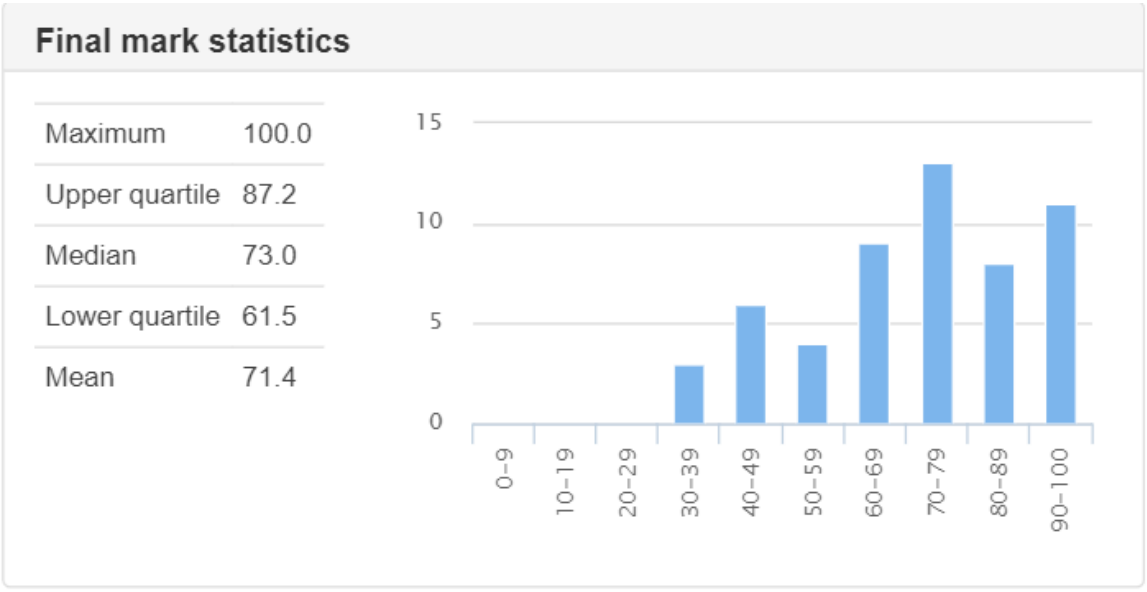
Comments on results of EEEN 202 Test 1

1. Generally very good results as shown below:



Congratulations on those students above 90 % - well done!

2. However, also a word of caution – the test was definitely on the easier side, particularly as Question 1 provided a "free" 10 marks. I would then suggest that you calculate your mark by ignoring Q1 and see what you get /55. This should be a far better reflection of your actual mastery of the work. This brings class average down from 71.4 % to 67.5%

Below some feedback on each question:

Q1: Avg. mark = 9/10.

As said a very easy intro question and most people got full marks as expected. However, several ignored the instruction to show your workings and got 5. A few should brush up on their BDC and hex.

Q2: Avg mark = 11.6/15

Generally well done, but some people not yet fully in control of MUXes. Note that where you put the input are important as the code on the select input will switch through a specific data input. Several people got the order of the data inputs wrong in (iv).

Also it is essential that you clearly label what the variables are that you are using as the select input and think about the code they provide. Several options possibilities for doing Q2 (v).

In Q2 (vi) I particularly said to use three 2:1 MUXes. Showing me how you could do it with a single MUX instead did not give you any marks for this question but did give a bonus mark.

Q3: Avg mark = 7.3/10

Most common mistake was not realising that every BCD input state after 1001 (9 decimal) should just be X = "don't care" as these states will not exist in the BCD code. It is essential to use these as X as you can then in the K-map change Xes to either 1 or 0 to give the most efficient simplification. In a

few cases people made a mess of simplification from the K-map. I would advise that you always clearly show(sketch) your groupings on the k-map and how that leads to simplification.

Q4: Avg mark = 8.1/15

The worst performing question of the test. Many people struggled with the timing diagrams and understanding the role of the Enable and CLK input. Essential stuff that you must make sure you can do !

In (b) many people did not see that the reset will put the code 100 on the counter. IT will then count DOWN from 100 to 000 with 111 the next state after 000. IT will then reset on 111 (not a counting state) and start at 100 again. Thus a down counter between 100 and 000 => MOD 5.

Also very few people got the full three marks for (c). What was needed was to say that it is due to the propagation delay and the total propagation delay will be 160 ns. (Note 8 FFs needed for 8 bit counter not 3 FFs as some stated). Then essential to calculate the absolute maximum counting frequency possible – 6.25 MHz.

Q5: Avg mark = 9.9/15

You had to realise that several values of the C-bit in the state diagram should be X = don't care as it will make this transition irrespective of the value of C (C=1 for MOD 4 and C=0 for MOD 3). However, most people did pretty well in completing the diagram.

Translating the diagram to the table should have been easy, but several unnecessary mistakes here. Of course there should be no X values here – it will always be going to a defined state !

You then had to provide the J_A and J_K inputs needed for the transition of A^n to A^{n+1}. Easiest is to produce your J-K excitation table and just work from that. Of course you will now find that one of the required input will always be X (don't care). It is essential that we use this fact as it will make simplification much more efficient. Many people produced JK values with no X states !

Some further comments:

1. Use of Circuitverse

A number of you decided to use Circuitverse to create your logic diagrams. Be very careful if you do that, because it can actually create more problems. One is that it does not automatically label I/Ps and O/P and if you forget to do these your diagram is not worth much. So my advice would to rather do a pen and paper sketch of your logic circuit and ensure that you have all I/Ps and O/Ps labelled.

In addition, if I already provide you with a sketch (e.g. the MUXes) just use these and add your labels and signals. Many of you made mistakes when translating these into your own sketches.

2. Following Instructions

I gave some instructions on handing in of the test – name format, file format etc which many of you completely ignored. Not a good way to start the test !

3. Other

Let me know if I have made a mistake with addition of marks etc and I will check. 4. For those people who have obtained < 50 % in the test the best advice is to ensure that you stay up to date with the second part of the work. Please come and see me if you have concerns about your progress.