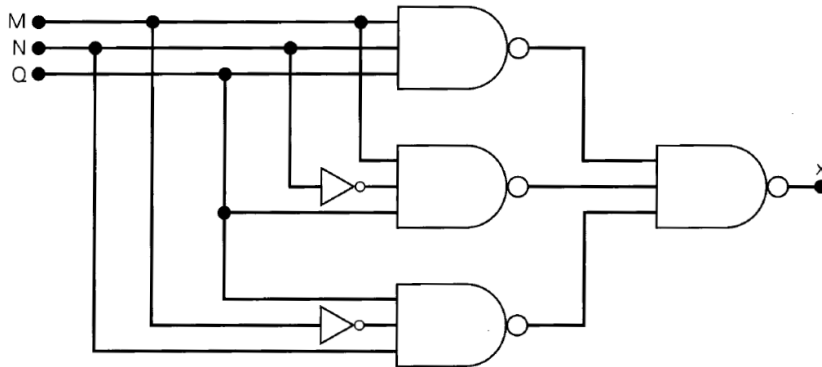**Due Monday 10 June 2024 before midnight.**

1. Simplify the circuit below using Boolean algebra

2. Determine the minimum expression for each K map below.

	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	1	1	1	1
$\bar{A}B$	1	1	0	0
AB	0	0	0	1
$A\bar{B}$	0	0	1	1

(a)

	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	1	0	1	1
$\bar{A}B$	1	0	0	1
AB	0	0	0	0
$A\bar{B}$	1	0	1	1

(b)

|	$\bar{C}$	C
$\bar{A}\bar{B}$	1	1
$\bar{A}B$	0	0
AB	1	0
$A\bar{B}$	1	X

(c)

3. Simplify the following expressions using Boolean algebra

(a) $x = \bar{A}\bar{B}\bar{C} + \bar{A}BC + ABC + A\bar{B}\bar{C} + A\bar{B}C$

(b) $x = \overline{C + D} + \bar{A}C\bar{D} + A\bar{B}\bar{C} + \bar{A}\bar{B}CD + AC\bar{D}$

4. You are to design a circuit that compares two 2-bit numbers, N1 and N2. Specifically, as shown, the circuit generates three outputs Feq, Flt and Fgt whose values are TRUE if N1 = N2, N1 < N2 and N1 > N2, respectively. The numbers N1 and N2 are denoted by single bit inputs A, B and C, D, respectively, where A and C are the most significant bits.
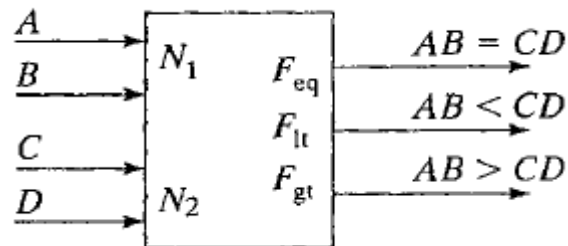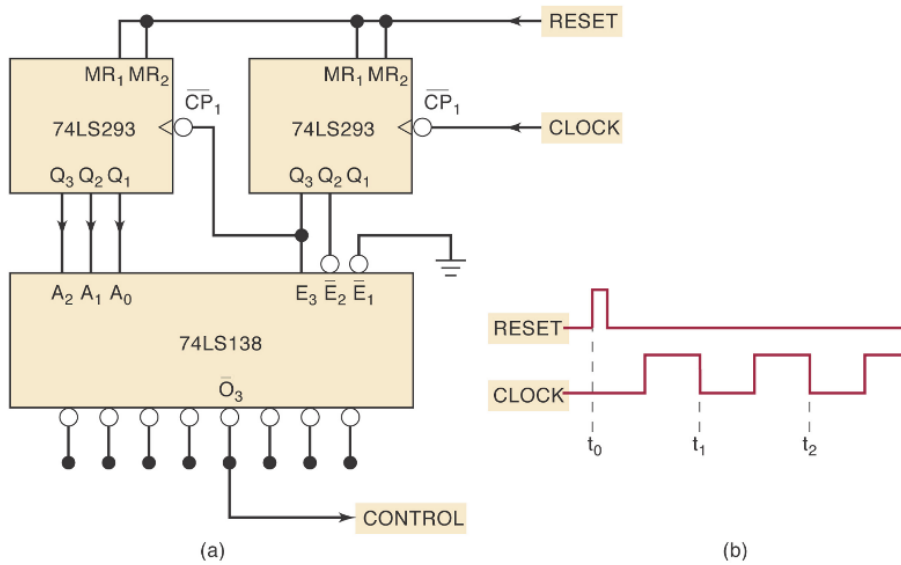

(a) Find the Boolean expressions for each of the outputs Feq, Flt and Fgt. Use K-maps to simplify them (if possible).
(b) Simplify Feq using Boolean algebra and express the final answer using XNOR operators.

5. Use J-K flip flops to design a **synchronous** counter that will go through the following sequence: **000, 010, 101, 110** and repeat. The undesired (unused) states must always go to 000 on the next clock pulse.

   Build the counter using the circuit simulator. Save your answer using the filename format: StudentIDNumberA2Q5 (Eg. 2012409101A2Q5.txt)

6. Redesign the counter of (Q5) without any requirement on the unused states, so that their next state can be a don't care state. Compare to the previous counter design.

   Build the counter using the circuit simulator. Save your answer using the filename format: StudentIDNumberA2Q6 (Eg. 2012409101A2Q6.txt)

7. Examine the circuit below, identify each of the ICs used and explain the operation of the circuit. Now modify the circuit so that it will produce a control signal that will remain LO from CLK t_{20} to t_{24}.

RESET

MR₁ MR₂ $\overline{CP}_1$

74LS293

$Q_3 Q_2 Q_1$

MR₁ MR₂ $\overline{CP}_1$

74LS293

$Q_3 Q_2 Q_1$

CLOCK

$A_2 A_1 A_0$

74LS138

$\overline{O}_3$

$E_3 \overline{E}_2 \overline{E}_1$

CONTROL

(a)

RESET

CLOCK

t_0 t_1 t_2

(b)