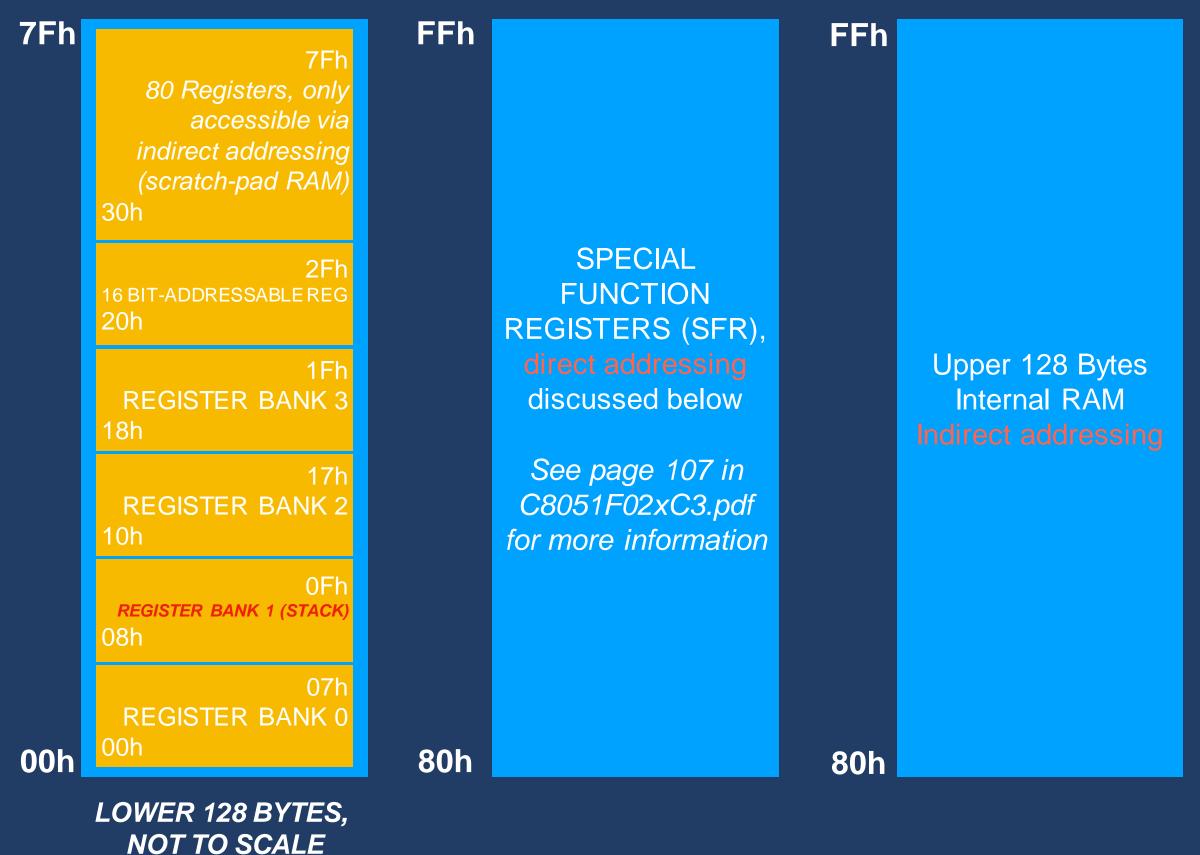
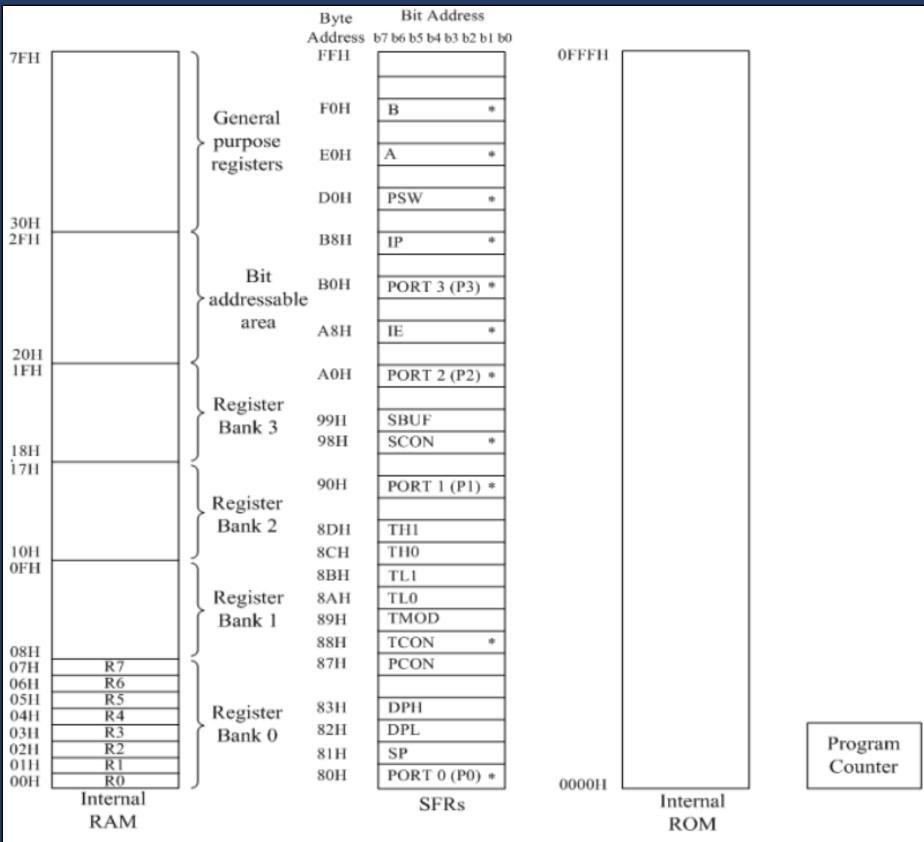
8051 DATA MEMORY MAP



8051 DATA MEMORY MAP



* Indicates the SFRs which are also bit addressable

8051 ADDRESSING MODES

 A key part of computer operation involves the accessing of memory; this may be done on the 8051 using five main approaches.

• IMMEDIATE ADDRESSING	 REGISTER ADDRESSING 	 DIRECT ADDRESSING 	 INDIRECT ADDRESSING 	 INDEXED ADDRESSING
MODE	MODE	MODE	MODE	MODE
The data is	The data	The address of	Slower: the	 Used to step
included in the	operand is in a	a location in	contents of a	through data
8051	specified	RAM is	location of the	(as in lookup
instruction.	register.	specified, and	address stored	tables).
• MOV A,#48H	 Only some 	its contents	in a register	 We won't be
The # shows	registers may	are operated	are fetched.	exploring this
that the data is	be used: R0	upon. Only	 MOV A,@R7 	in depth (and
'immediate'	through R7 of	works with	• The @	you won't be
In a sense, this	each of the	internal RAM &	indicates	tested on it!),
data is hard-	8051's banks.	SFR's	an address	but see details
coded into the	MOV A,R7	 MOV A,10H 	Upper 128	about the
instruction.	 Contents of 	 Contents of 	bytes of RAM	MOVC
Fast but less	R7 are	address	are accessible	instruction in
flexible.	copied to	are copied	this way.	C8051F02xC3.pdf
	ACC.	to ACC.		

8051 GENERAL PURPOSE REGISTERS

- The lowest addresses of the 8051's internal RAM are a number of General Purpose Registers.
 - There are four banks of these registers, with each bank having 8 registers (R0 through R7).
 - 32 Bytes total.
 - By default, Bank 0 is enabled.
 - As default, MOV A, R7 will move Bank 0's contents to accumulator.
 - We can switch register banks using bits 3 and 4 of the PSW flag register.

R7	R7	R7	R7		RS1	RS0
R6	R6	R6	R6			
R5	R5	R5	R5	BANK 0	0	0
R4	R4	R4	R4		0	1
R3	R3	R3	R3	BANK 1	0	1
R2	R2	R2	R2	BANK 2	1	0
R1	R1	R1	R1			
R0	R0	R0	R0	BANK 3	1	1
Bank 0	Bank 1	Bank 2	Bank 3			

8051 FLAGS

PSW.7 CY (Carry flag, raised when the processor needs to carry in addition)	PSW.6 AC (Aux. carry, used during BCD math)	PSW.5 F0 (User- assignable flag)	PSW.4 RS1 (Register bank selector, don't worry about for now)	PSW.3 RS2 (Register bank selector, don't worry about for now)	PWS.2 OV (Overflow, raised when a signed number overflows into the sign bit)	PSW.1 - (User assignable)	PSW.0 P (Parity: 0 if acc. holds even number of 1's)
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GENERAL PURPOSE REGISTER EXAMPLE CODE

MOV R0,#FFH ;Load R0 with 0xFF (immediate addressing) MOV R1,R0 ;Copy R0 contents to R1 (register addressing) MOV P0,R1 ;2 cycles! Direct move from R1 to P0 MOV 00,#FFH ;Address 00 is R0 (direct addressing)

;;Now, we'll switch reg. banks to bank 3 (PSW.4 HI, PSW.3 HI).

SETB PSW.4 ;Sets the register bank select bit RS1 high SETB PSW.3 ;Sets the register bank select bit RS2 high

;;R0-R7 now refer to bank 3 rather than bank 0 (default)
MOV R0,#FFH ;Same operation as top of code, different bank
MOV 00,#FFH ;However, this still refers to `bank 0, R0'