

ECEN202

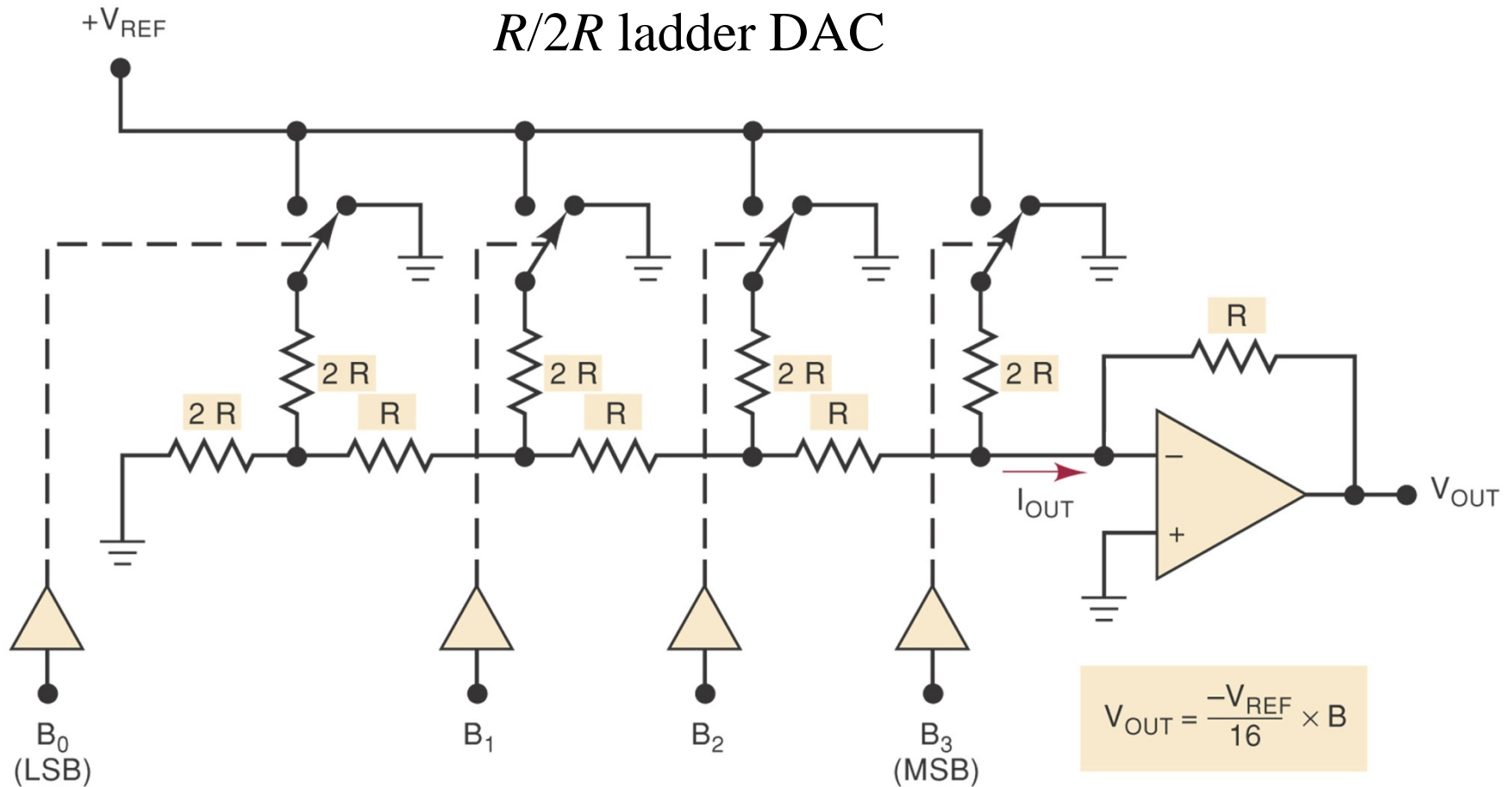
2024

Digital to Analog Conversion.

Lecture 2

Practical D/A Converter Circuitry

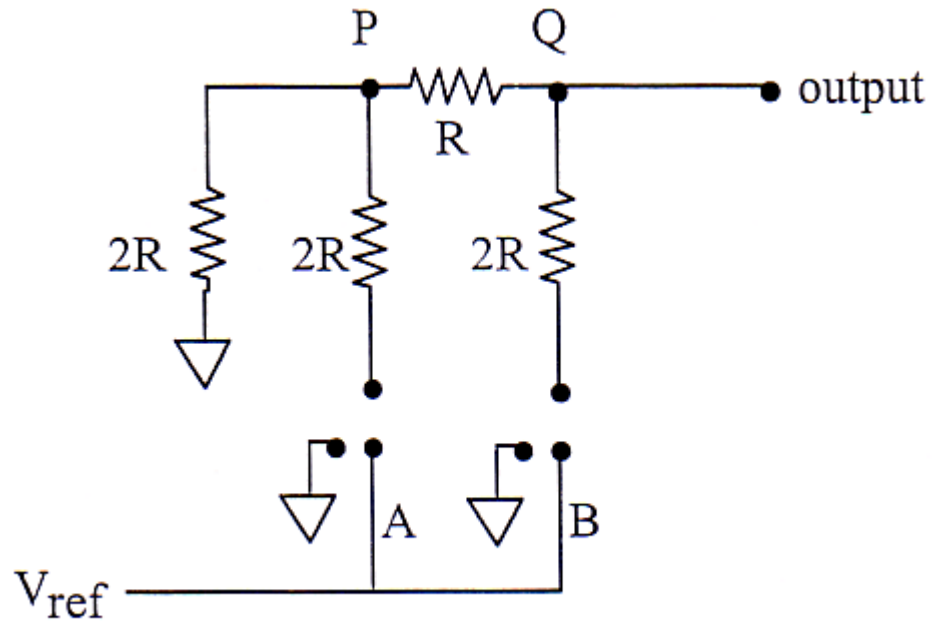
- R/2R ladder
 - Circuits with binary weighted resistors cause a problem due to the large difference in R values between LSB and MSB
 - e.g. for 12 bits can span from 1k (MSB) to >2M for LSB
 - Rather use R/2R ladder in practice
 - The R/2R ladder uses resistances that span only a 2 to 1 range



where B is the value of the binary I/P's from 0000 to 1111

$$V_{out} = \frac{V_{ref}}{2^4} (2^3 B_3 + 2^2 B_2 + 2^1 B_1 + 2^0 B_0)$$

Easier to consider a 2-bit converter



$$V_{\text{out}} = \frac{V_{\text{ref}}}{2^2} (2^1 B + 2^0 A)$$

Consider the cases: $B=0, A=0$

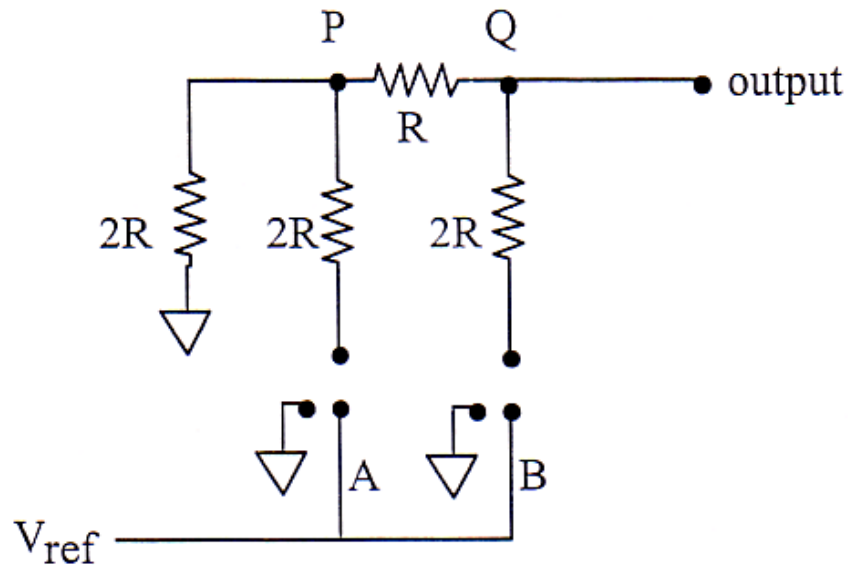
$B=1, A=0$

$B=0, A=1$

$B=1, A=1$

and prove that the relationship
holds for all.

$$V_{\text{out}} = \frac{V_{\text{ref}}}{2^2} (2^1 B + 2^0 A)$$



So for an n-bit R-2R ladder ADC we have the output given by:

$$V_{\text{out}} = \frac{V_{\text{ref}}}{2^n} \left(2^{n-1} S_{n-1} + 2^{n-2} S_{n-1} + \dots + 2^0 S_0 \right)$$

where S_n represents the state (0 or 1) of the n^{th} bit in the system.

Problem: Assume that $V_{REF} = 10\text{ V}$ for the 4 bit DAC. What are the resolution and full-scale output of this converter?

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Answer:

The resolution is equal to the weight of the LSB, which we can determine by setting $B = 0001 = 1$

$$\text{resolution} = -10\text{ V} * 1/16 = -0.625\text{ V}$$

The full-scale output occurs for $B = 1111 = 15_{10}$.

$$\text{full scale} = -10\text{ V} * 15/16 = -9.375\text{ V}$$

Questions ?

- A. What is the advantage of R/2R ladder DACs over those that use binary weighted resistors?
- B. A certain six-bit DAC uses binary-weighted resistors. If the MSB resistor is $20 \text{ k } \Omega$ what is the LSB resistor?
- C. What will happen to both resolution and full-scale output when V_{REF} is increased by 20 percent?

Questions ?

A. What is the advantage of R/2R ladder DACs over those that use binary weighted resistors?

Ans: It uses only two different sizes of resistors.

B. A certain six-bit DAC uses binary-weighted resistors. If the MSB resistor is $20\text{ k}\Omega$ what is the LSB resistor?

Ans: $640\text{ k}\Omega$.

C. What will happen to both resolution and full-scale output when V_{REF} is increased by 20 percent?

Ans: Increases by 20 percent.

DAC Specification

- A wide variety of DACs are available as ICs or as self-contained, encapsulate packages.
- One should be familiar with the more important manufacturers' specifications in order to evaluate a DAC for a particular application.
 - Resolution: the percentage resolution of a DAC depends solely on the number of bits.
 - Accuracy: The two most common are called *full-scale error* and *linearity error*, which are normally expressed as a percentage of the converter's full-scale output (% F.S.). It is important to understand that accuracy and resolution of a DAC must be compatible.
 - Offset error: Ideally, the output of a DAC will be zero volts when the binary input is all 0s. In practice, however, there will be a very small output voltage for this situation; this is called offset error.

Output examples showing an offset of 2mv

Input Code	Ideal Output (mV)	Actual Output (mV)
0000	0	2
0001	100	102
1000	800	802
1111	1500	1502

- Settling Time: The operating speed of a DAC is usually specified by giving its settling time, which is the time required for the DAC output to go from zero to full scale as the binary input is changed from all 0s to all 1s.

Problem: A certain eight-bit DAC has a full-scale output of 2 mA and a full-scale error of $\pm 0.5\%$ F.S. What is the range of possible outputs for an input of 10000000?

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Answer:

The step size is $2 \text{ mA} / 255 = 7.84 \mu \text{ A}$.

Since $10000000 = 128_{10}$, the ideal output should be $128 * 7.84 \mu \text{ A} = 1004 \mu \text{ A}$.

The error can be as much as

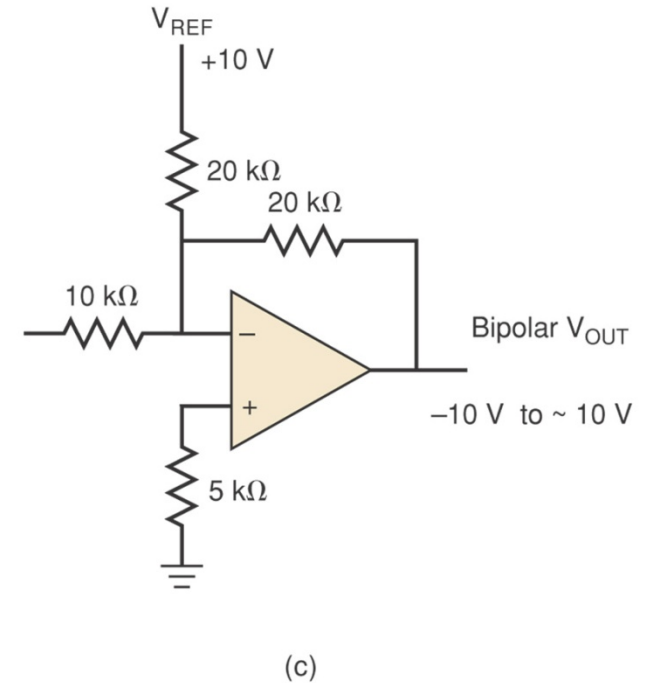
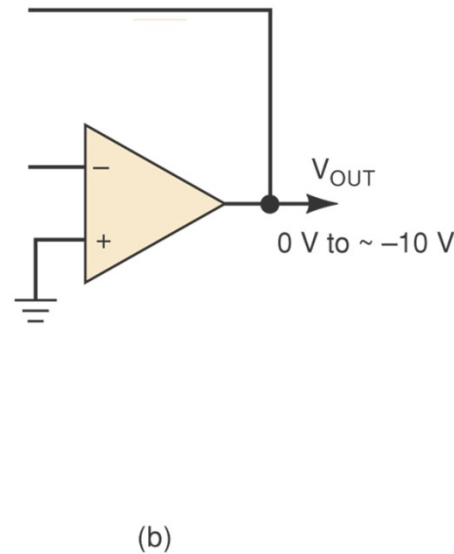
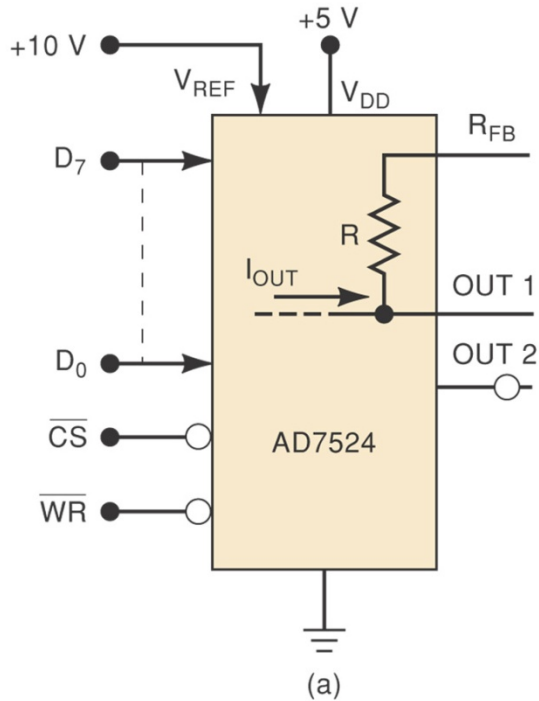
$$\pm 0.5\% * 2 \text{ mA} = \pm 10 \mu \text{ A}$$

Thus, the actual output can deviate by this amount from the ideal $1004 \mu \text{ A}$, so the actual output can be anywhere from 994 to $1014 \mu \text{ A}$.

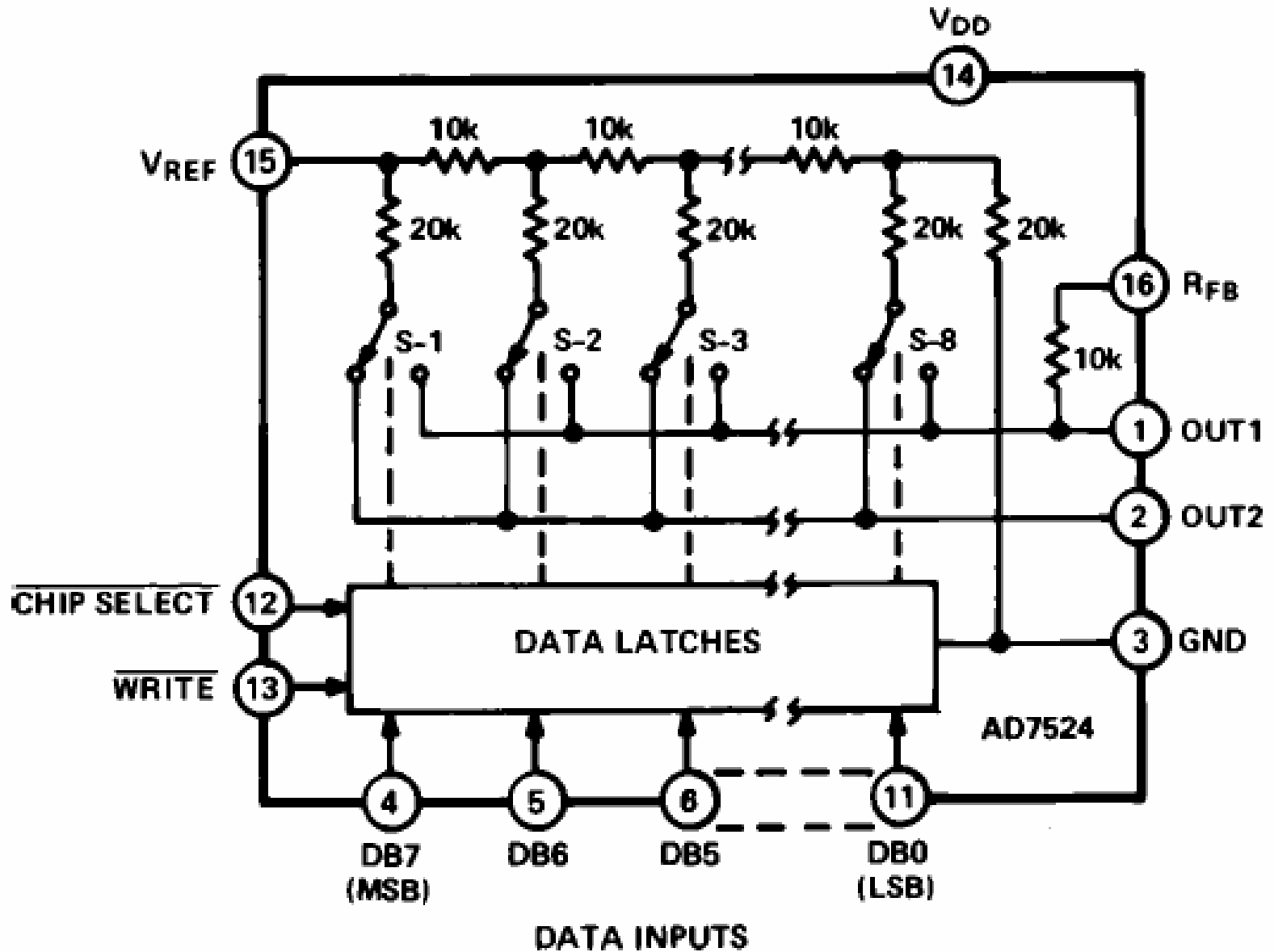
An IC DAC

- AD7524
 - CMOS IC
 - 8 bit D/A
 - Uses R/2R ladder network
 - Max settling time is 100 ns
 - Full range accuracy is +/- 0.2% F.S.
 - Reference voltage can be negative and positive from 0 to 25 V.

(a) AD7524 8-bit DAC with latched inputs; (b) op-amp current-to-voltage converter provides 0 to approximately -10 V out; (c) op-amp circuit to produce bipolar output from -10 V to approximately +10 V.



FUNCTIONAL BLOCK DIAGRAM



DAC Applications

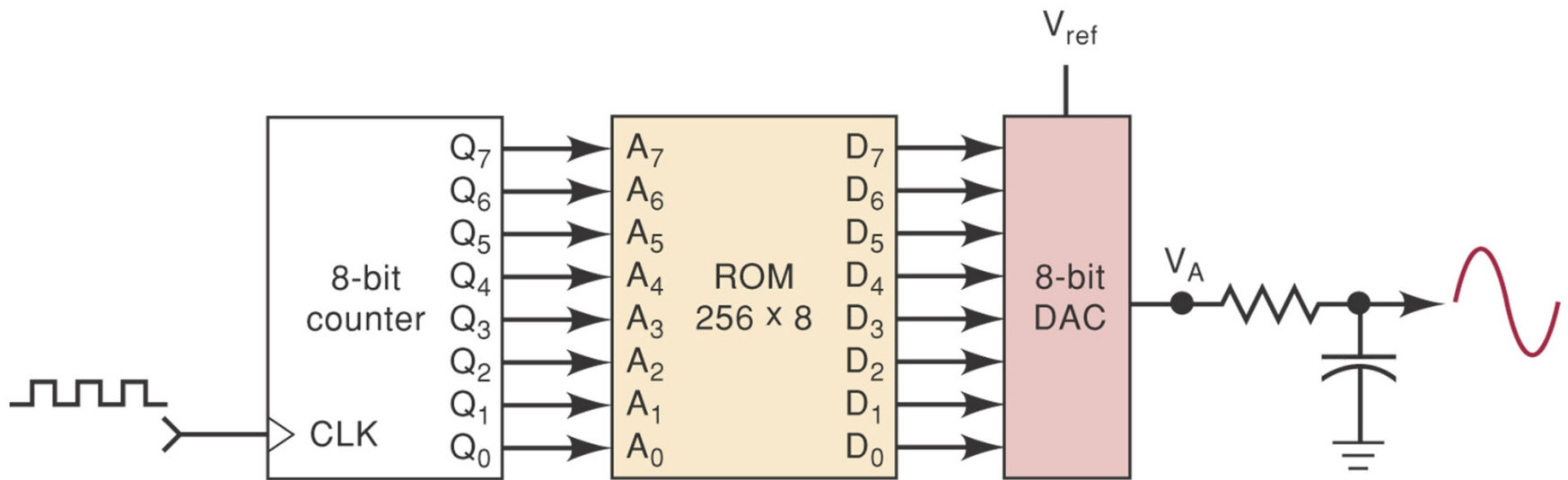
- Used when a digital circuit output must provide an analog voltage or current
 - Control
 - Use a digital computer output to adjust motor speed or furnace temperature
 - Automatic testing
 - Computer generated signals to test analog circuitry
 - Signal reconstruction
 - Restoring an analog signal after it has been converted to digital. Audio CD systems, and audio/video recording
 - A/D conversion
 - Direct Digital Synthesis

Generating a sinusoidal waveform.

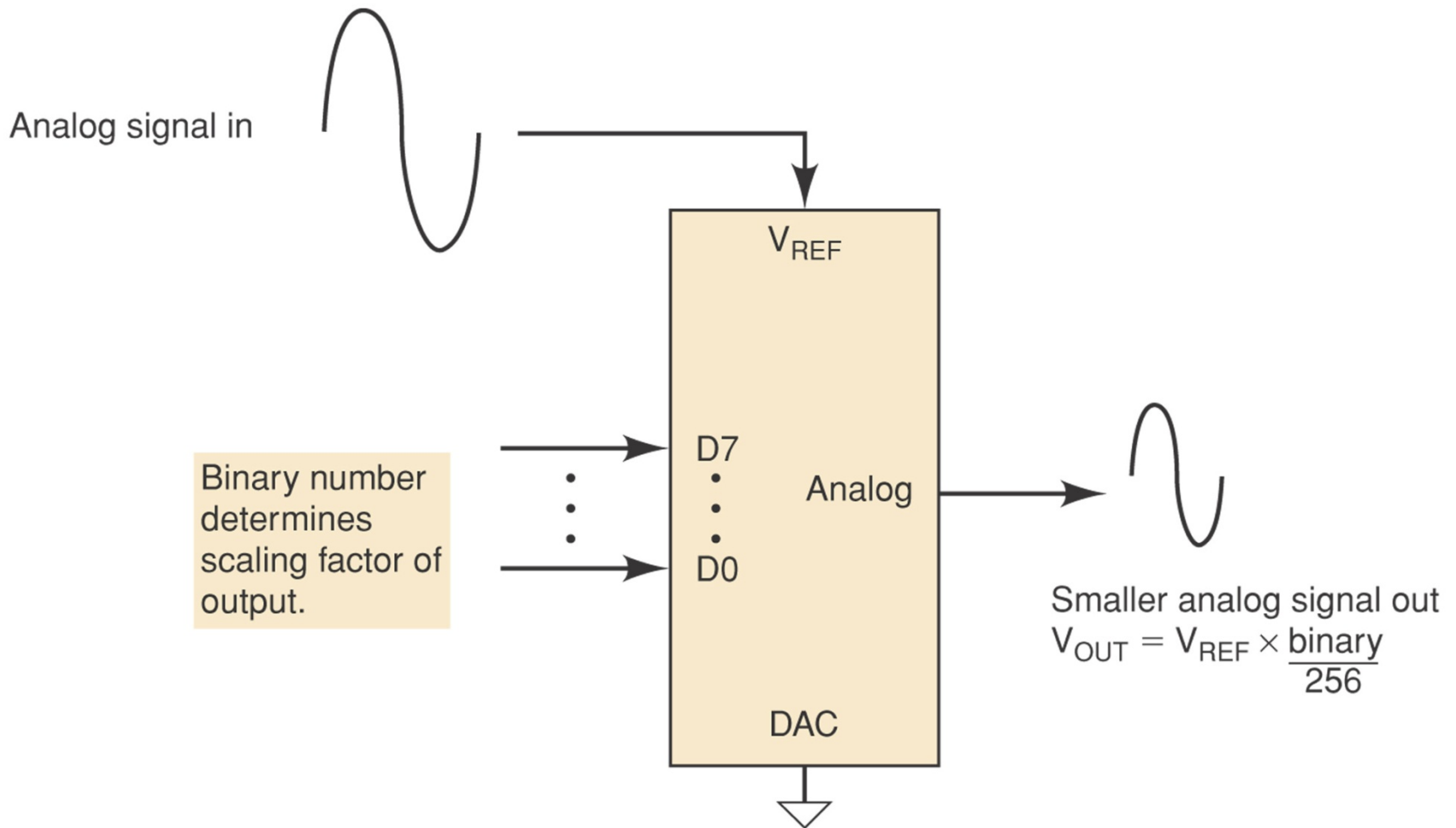
Generating a sinusoidal waveform is a common D/A application. This will typically use the following parts:

- A clock for pulse generation
- A counter driven by the clock
- A sine (or waveform coded) ROM
- An DAC driven by the ROM O/P
- A low pass filter to reduce distortion or other signal shaping circuitry

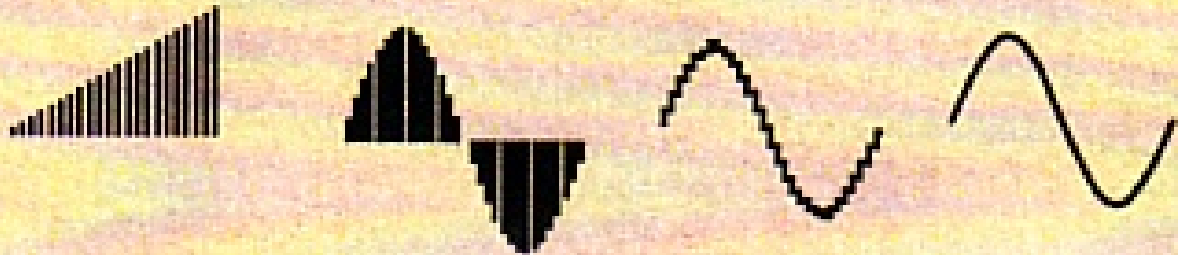
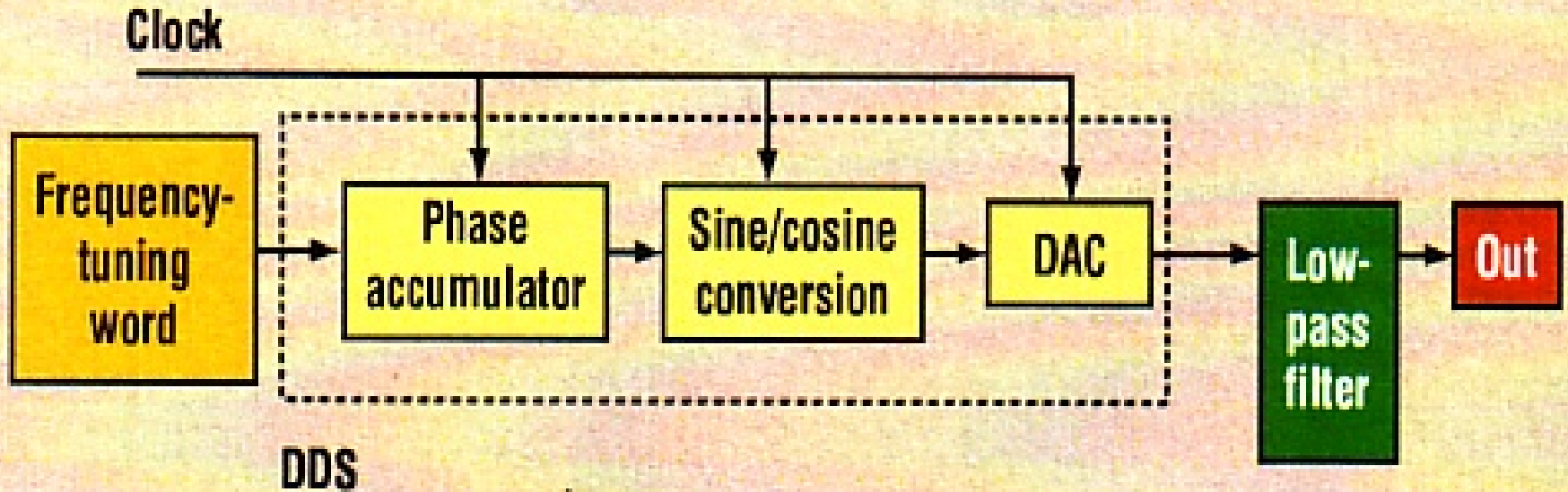
Creating a waveform by using a ROM and a DAC



A DAC used to control the amplitude of an analog signal.

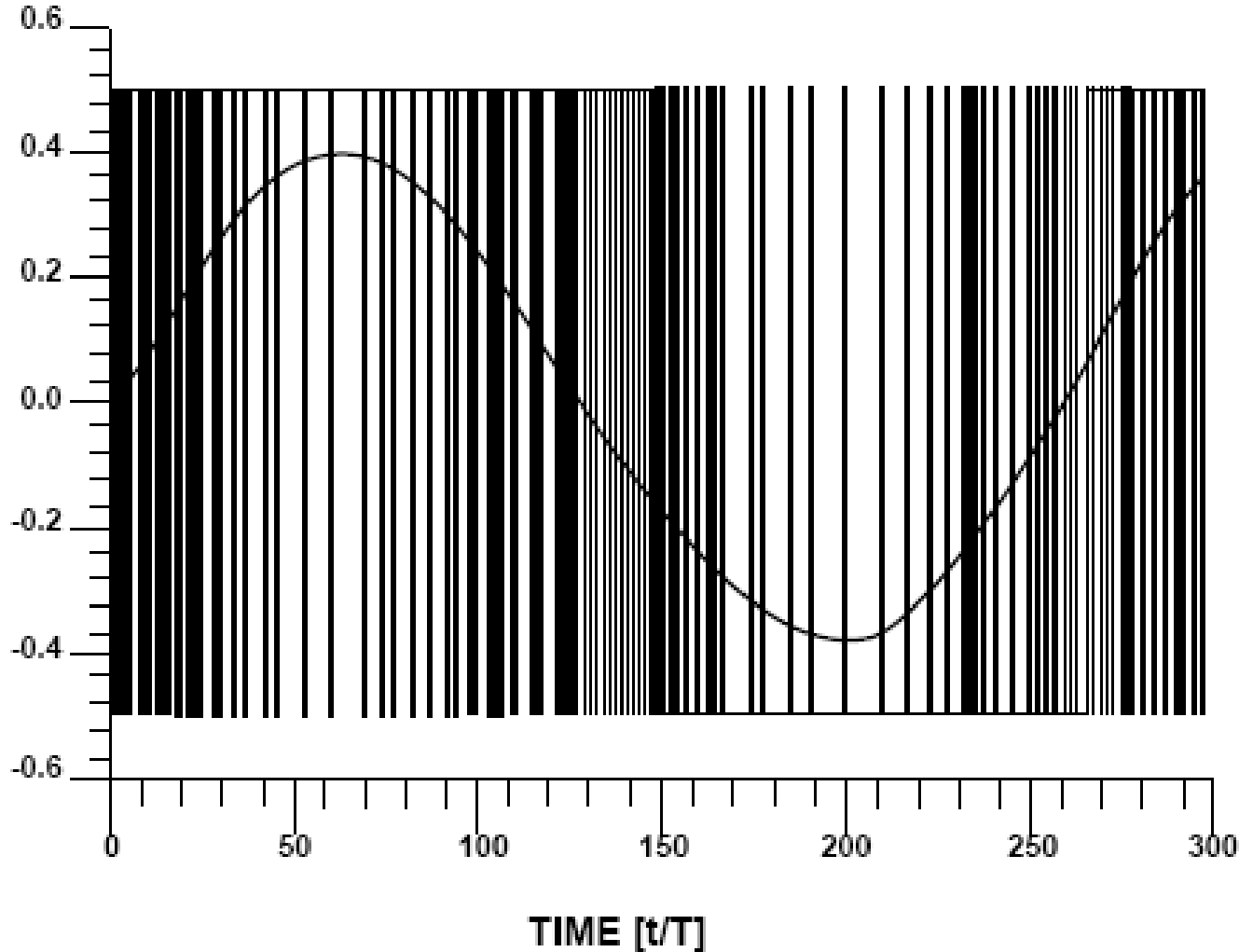


DAC forms an integral part of DDS systems.



Pulse Width Modulation (PWM) DAC

A single digital output can be used to generate a waveform!
This is done by low pass filtering a PWM output.



This method
is used in high
power sub
woofer
amplifiers!!

Called
"class D"