

Family Name: Other Names:

Student ID: Signature

ECEN 202: Final exam

2019, Dec 23 ** WITH SOLUTIONS **

Instructions

- Time allowed: **120 minutes**
- Attempt **all** the questions. There are 45 marks in total.
- Write your answers in this exam paper and hand in all sheets.
- If you think some question is unclear, ask for clarification.
- You may use dictionaries.
- You may write notes and working on this paper, but make sure your answers are clear.

Questions

Marks

1. Microprocessors

[30]

2. ADC and DAC

[15]

TOTAL:

December 21, 2019

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Cross out rough working that you do not want marked.
Specify the question number for work that you do want marked.

Question 1. Microprocessors**[25 marks]**

(a) [1 mark] What high-level computer architecture makes use of separate data and program memories?

Harvard

(b) [1 mark] In a standard 8051, how many clock cycles result in one machine cycle?

12

(c) [2 marks] Given a 40 MHz crystal, find the time (in μs) required for one machine cycle

$1/(40/12) = 0.3 \mu s$

(d) [2 marks] Given a 12 MHz crystal, find the time (in μs) required for one machine cycle

$12\text{MHz}/12 = 1 \text{ MHz frequency of machine, } 1/1\text{MHz} = 1 \mu s$

(e) [1 mark] How many bits is Register A?

8-bit (1 byte)

(f) [1 mark] What register holds the address of the next instruction to be executed?

Program Counter (PC)

(Question 1 continued on next page)

(Question 1 continued)

(g) [1 mark] What is 0d16 in hexadecimal?

0d16 dec to hex = 0x10 hex

(h) [1 mark] On the 8051, what does the NOP instruction do?

Causes no operation that cycle

(i) [1 mark] What instruction is used to add data to the stack?

Push: data is added to the stack

(j) [1 mark] What instruction is used to remove data from the stack?

Pop: the most recently added data is removed from the stack

(k) [1 mark] What addressing mode is used by the following instruction? MOV A, R7

Register addressing mode

(Question 1 continued)

(l) [1 mark] Multiple choice (circle one of 1-4): On the 8051, when MOV A,B is called, which of the following occurs?

1. The contents of B are moved to A, with B's contents being cleared after this operation
2. The contents of a A are moved to B, with A's contents being cleared after this operation.
3. The contents of B are moved to A, with B's contents being retained after this operation.
4. The contents of a A are moved to B, with A's contents being retained after this operation.

3

(m) [1 mark] Multiple choice (circle one of 1-4): On the 8051, which of the following instructions is directly associated with a subroutine call?

1. LJMP
2. SJMP
3. ACALL
4. INC

ACALL

(n) [3 marks] Briefly describe the role, function, and use of a **watchdog** timer

Role: prevents the system from hanging.
Function: resets the system if the timer is not reset in a timely manner.
Use: In a regularly-accessed region of code, the timer is reset in software. If this reset isn't reached (code is hanging), the system will reset

(o) [2 marks] Briefly describe the advantages of an interrupt-driven approach compared to a blocking/ polling approach.

In polling method, the microcontroller is checking continuously whether the device is ready or not. It makes the CPU busy.
In interrupt, however, the device notifies the CPU that it needs servicing.

(Question 1 continued on next page)

(Question 1 continued)

(p) [2 marks] The initial contents of Register A are 0b11001100. What are the contents of Register A after the execution of an ORL instruction against A with an operand of 0b00110011?

0b11111111

(q) [2 marks] The initial contents of Register A are 0b11111111. What are the contents of Register A after the execution of an ANL instruction against A with an operand of 0b00100000?

0b00100000

(r) [2 marks] The A register has an initial value of 0b00000100
What are the register's contents after executing the following code?

```
RR A
RR A
ANL A, #10000011B
```

0000001B

(Question 1 continued)

(s) [4 marks] Timer mode information and details about the TMOD register are provided. Write code that sets Timer 0 to Mode 1 and Timer 1 to Mode 3. Assume that TMOD holds other values that must not be overwritten.

	Mode name
MODE 0	13-bit timer mode: 8 bits of THx and 5 bits of TLx
MODE 1	16-bit timer mode. TLx counts 0-255; on overflow, this adds 1 to THx
MODE 2	8-bit timer mode. TLx auto-reloads with THx value
MODE 3	“Split timer” mode: THx is one 8-bit timer, and TLx is another

TMOD.7 GATE When 1, timer only counts when TR1 bit is high and there is an external interrupt at INT0	TMOD.6 C/T When 0, Timer1 serves as XTAL-driven delay generator (timer); When 1, Timer1 counts external events	TMOD.5 M1 Timer 1 Mode bit 1 (see figure below for timer mode info.)	TMOD.4 M0 Timer 1 Mode bit 0 (see figure below for timer mode info.)	TMOD.3 GATE When 1, timer only counts when TR0 bit is high and there is an external interrupt at INT1	TMOD.2 C/T When 0, Timer0 serves as XTAL-driven delay generator (timer); When 1, Timer0 counts external events	TMOD.1 M1 Timer 0 Mode bit 1 (see figure below for timer mode info.)	TMOD.0 M0 Timer 0 Mode bit 0 (see figure below for timer mode info.)
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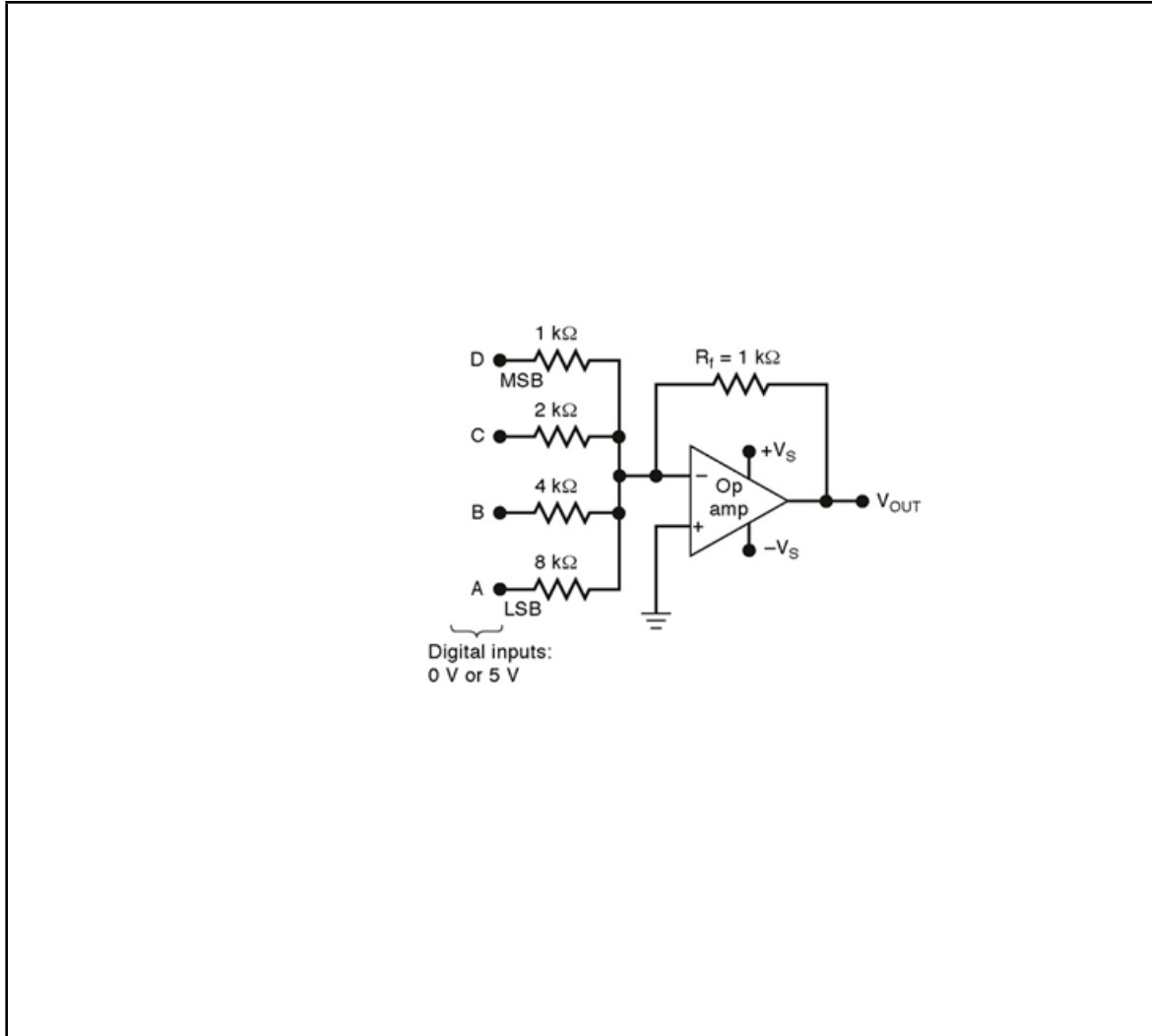
Timer 0 Mode Select Bit

<u>M10</u>	<u>M00</u>	<u>Operating mode</u>
0	0	Mode 0: 8-bit Timer/Counter (TH0) with 5-bit prescaler (TL0).
0	1	Mode 1: 16-bit Timer/Counter.
1	0	Mode 2: 8-bit auto-reload Timer/Counter (TL0) ⁽²⁾
1	1	Mode 3: TL0 is an 8-bit Timer/Counter TH0 is an 8-bit Timer using Timer 1's TR0 and TF0 bits.

```
ORL TMOD, #00110001B
```

Question 2. ADC and DAC**[15 marks]**

(a) **[4 marks]** Sketch a circuit diagram of a four-bit binary-weighted Digital to Analogue Converter (DAC)



(b) **[2 marks]** Briefly describe the major advantage and disadvantage of a flash converter.

Major advantage is its conversion speed;
Disadvantage is the number of required circuit components for a practical resolution.

(c) **[1 mark]** A certain eight-bit successive-approximation converter has 2.55 V full scale. The conversion time for $V_A = 1$ V is $80 \mu\text{s}$. What will be the conversion time for $V_A = 1.5$ V?

$80 \mu\text{s}$

(Question 2 continued on next page)

(Question 2 continued)

(d) [8 marks] For the following analogue to digital converters cases, calculate both the binary and decimal output code. Show your calculations.

i. [4 marks] An input voltage of 4.261 V into a 8-bit ADC with a 0 – 8 V input range.

The number of total possible steps is $2^8 - 1 = 255$
 the step size or resolution of A/D is $8 \text{ V}/255 = 31.4 \text{ mV}$
 To what code level (step) does the I/P voltage corresponding:
 $4.261 \text{ V}/31.4 \text{ mV} = 135.7 \approx 136 \text{ steps}$
 The analogue I/P voltage will be converted in 8-bit binary by A/D:
 1000 1000
 The decimal output will be: $136 \times 31.4 \text{ mV} = 4.270 \text{ V}$

ii. [4 marks] (ii) An input voltage of 2.295 V into a 10-bit ADC with a 0 – 4 V input range.

The number of total possible steps is $2^{10} - 1 = 1023$
 the step size or resolution of A/D is $4 \text{ V}/1023 = 3.91 \text{ mV}$
 To what code level (step) does the I/P voltage corresponding:
 $2.295 \text{ V}/3.91 \text{ mV} = 586.9 \approx 587 \text{ steps}$
 The analogue I/P voltage will be converted in 10-bit binary by A/D:
 10 0100 1011
 The decimal output will be: $587 \times 3.91 \text{ mV} = 2.295 \text{ V}$

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