XMUT 202
Digital Electronics

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UNIVERSITY OF WELLINGTON
Te Whare Wānanga
o te Ūpoko o te Ika a Māui
CAPITAL CITY UNIVERSITY

Review Exercise 2 (Gates and Latches)

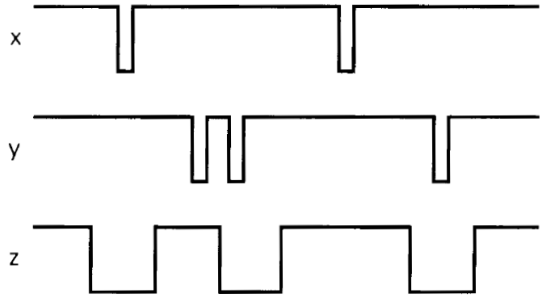


FIGURE 5-61

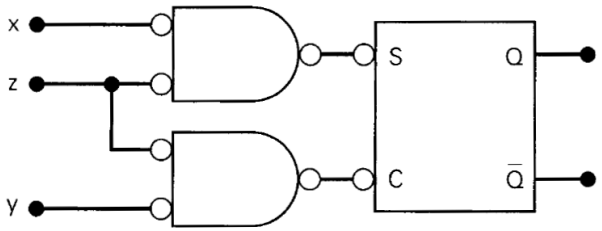
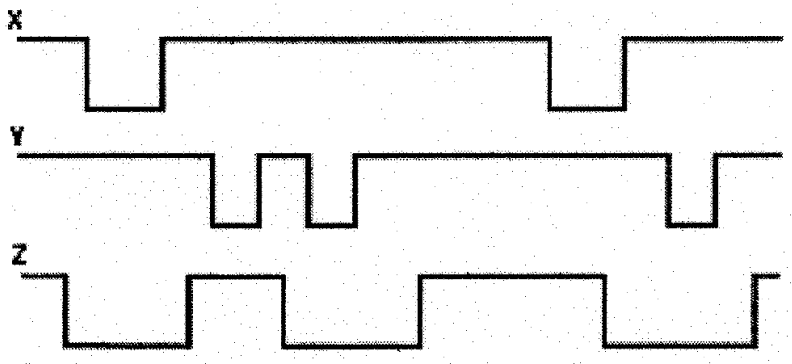
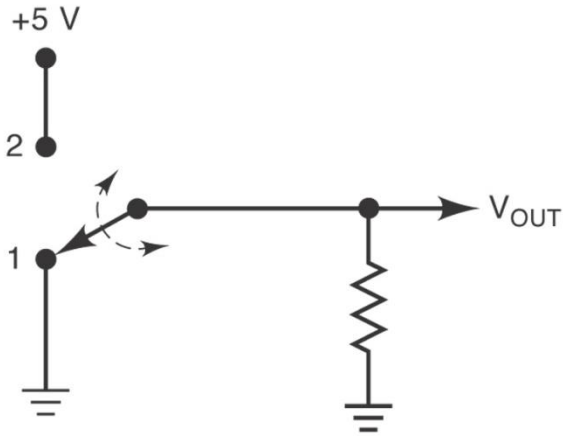


FIGURE 5-62

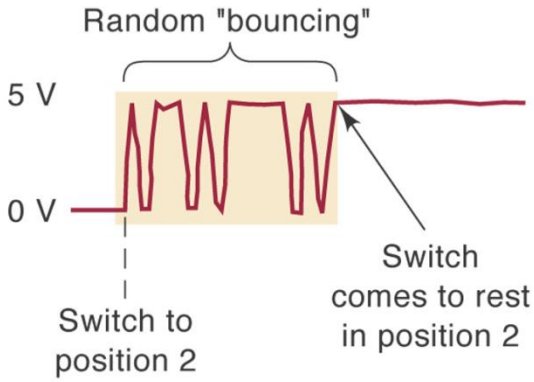
5-3. The waveforms of Figure 5-61 are connected to the circuit of Figure 5-62. Assume that $Q = 0$ initially, and determine the Q waveform.



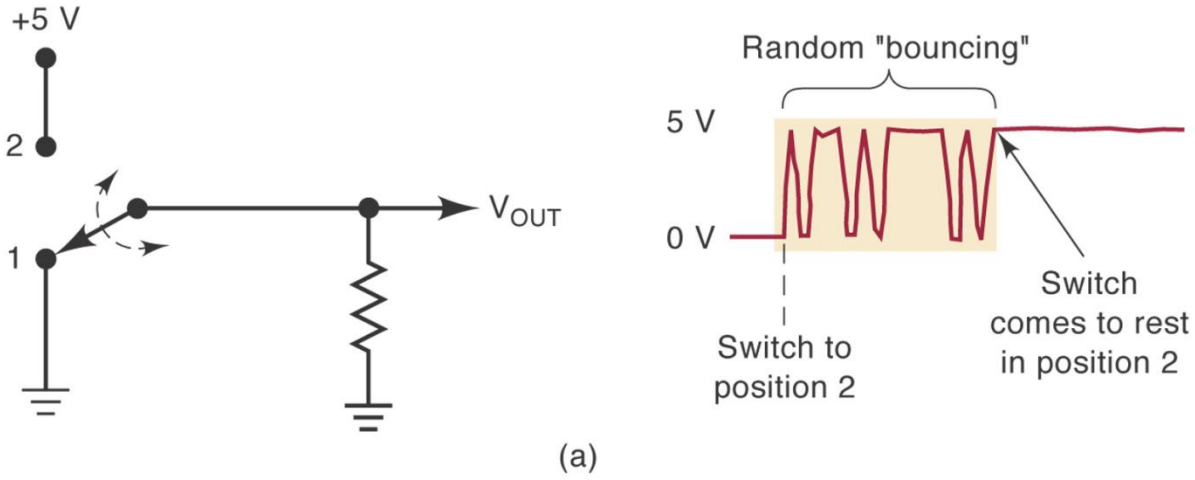
Interesting application of a latch – Eliminating mechanical switch bounce



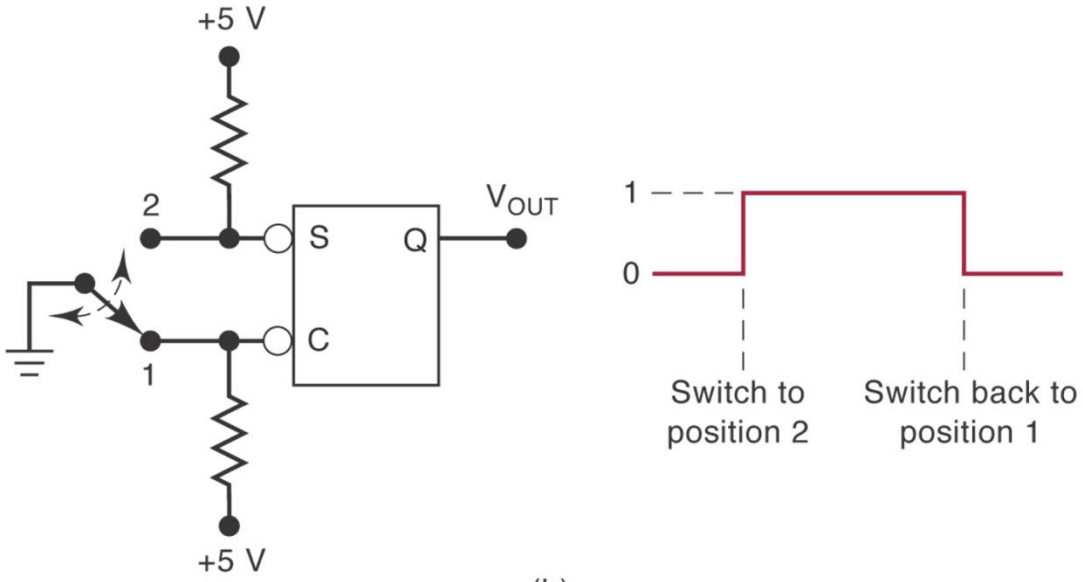
(a)



Interesting application of a latch – Eliminating mechanical switch bounce



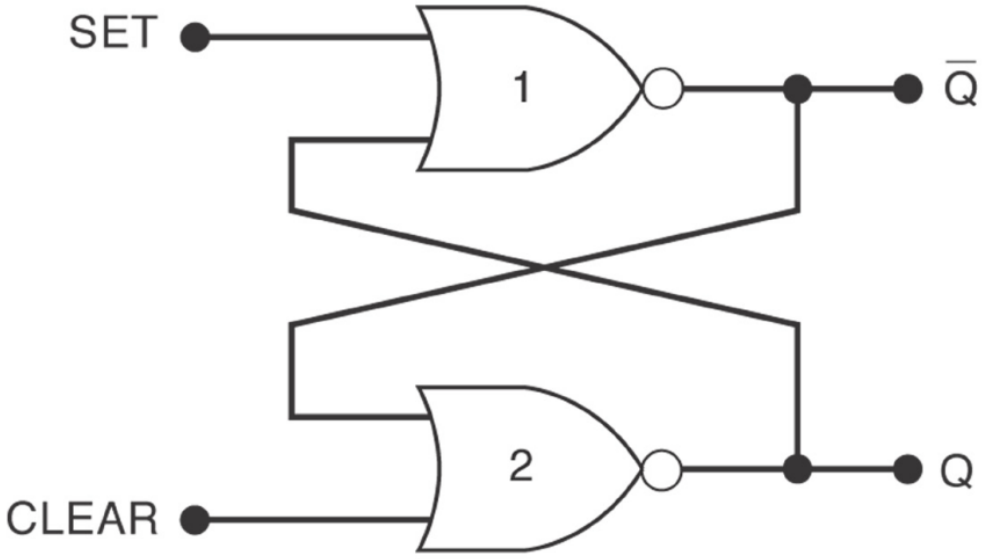
(a)



(b)

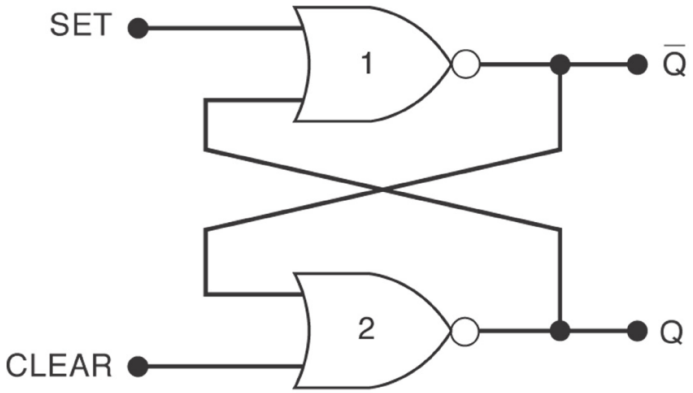
The NOR Gate Latch

- The **NOR** latch is similar to the NAND latch except that the Q and $\overline{Q}$ outputs are reversed.



The NOR Gate Latch

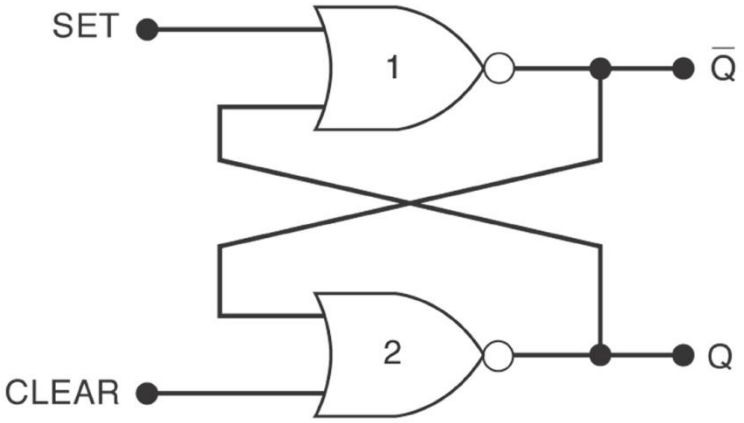
- The **NOR** latch is similar to the NAND latch except that the Q and $\overline{Q}$ outputs are reversed.
- The Set and Clear inputs are **active high**, that is, the output will change when the input is pulsed high.



The NOR Gate Latch

- The **NOR** latch is similar to the NAND latch except that the Q and $\overline{Q}$ outputs are reversed.
- The Set and Clear inputs are **active high**, that is, the output will change when the input is pulsed high.
- In order to ensure that a latch/FF begins operation at a known level, a pulse may be applied to the Set or Clear inputs when a device is powered up.

The NOR gate latch



(a)

Set	Clear	Output
0	0	No change
1	0	Q = 1
0	1	Q = 0
1	1	Invalid*

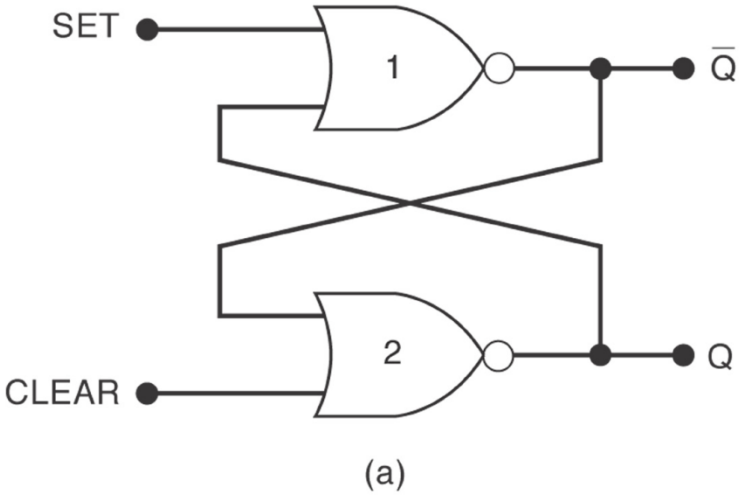
*Produces $Q = \overline{Q} = 0$.

(b)

The NOR gate latch

NOR Gate

A	B	X
0	0	1
0	1	0
1	0	0
1	1	0



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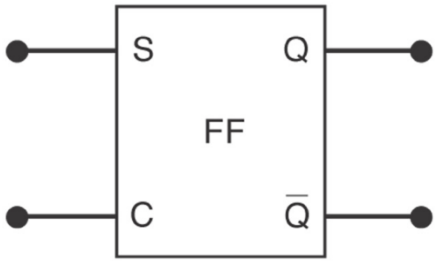
*Produces $Q = \overline{Q} = 0$.

(b)



(c)

- SET = CLEAR = 0: Normal resting state – no effect on O/P state.
- SET = 1, CLEAR = 0: gets Q = 1, will remain when SET goes LO.
- SET = 0, CLEAR = 1: Clear to Q = 0, remain when CLEAR goes LO.
- SET = 1 = CLEAR, Tries to set and clear simultaneously, not allowed.

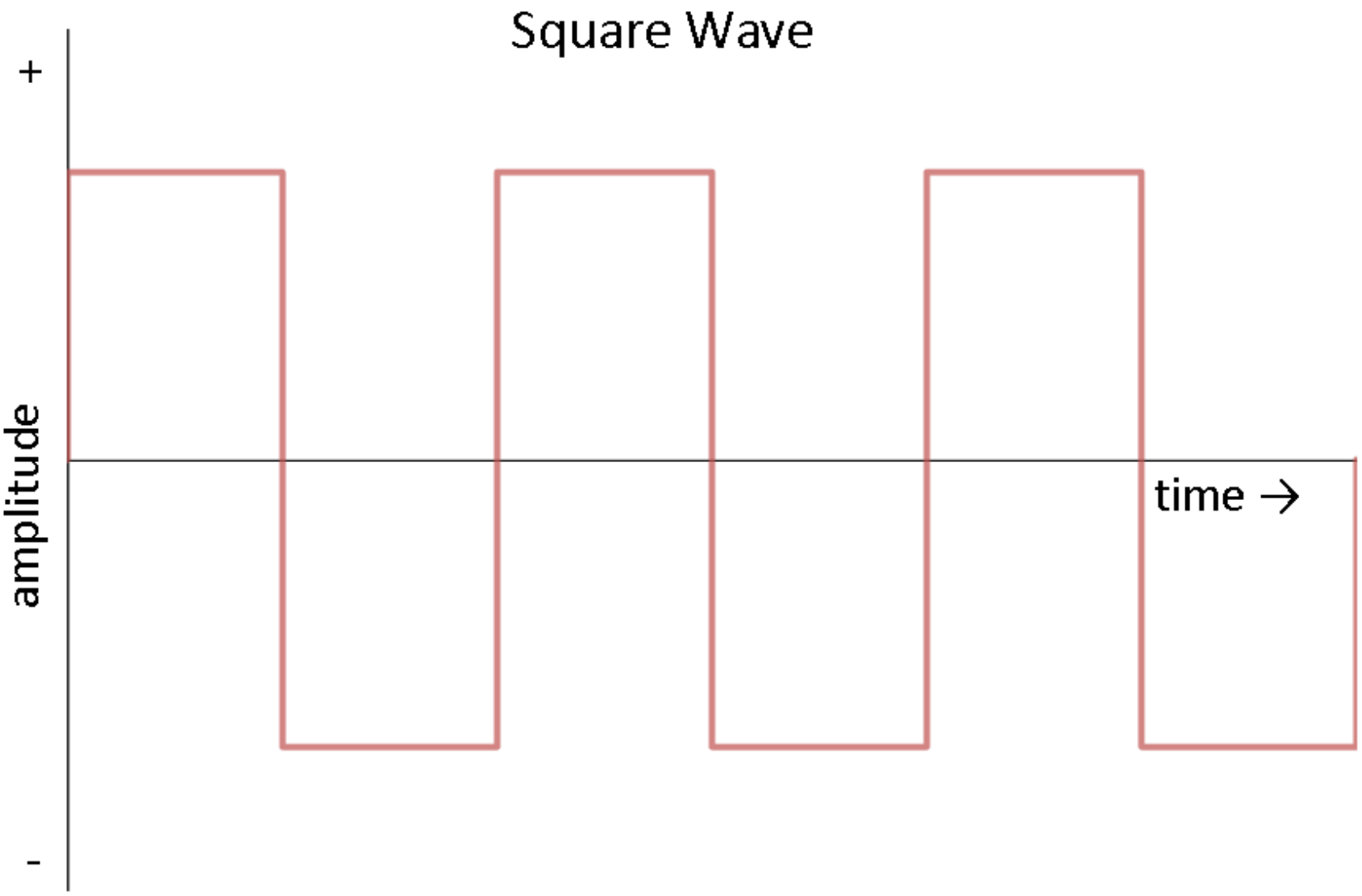
Clock Signals and Flip-Flops

Now add a **clock signal** (another input to a latch) in order to synchronise the change in output.

- Asynchronous system – outputs can change state at any time the input(s) change = latch as we have seen.

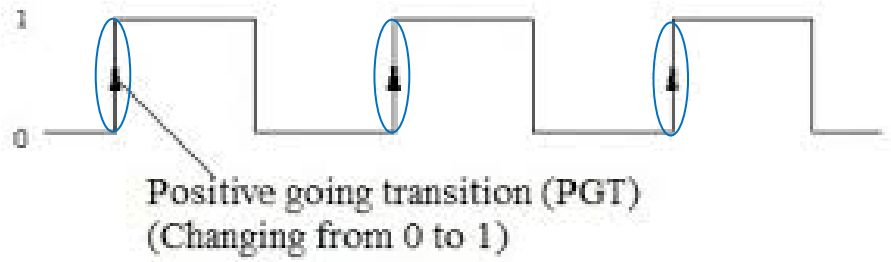
- Synchronous system – output can change state only at a specific time. This timing is determined by a clock input – change in output will be synchonized with the clock cycle = flip-flop. Inputs will then only have effect at the clock event.

• The clock signal is a rectangular pulse train or square wave.

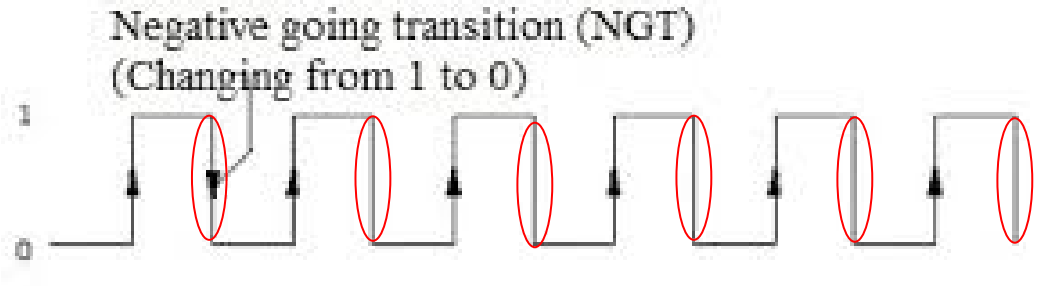


- The clock signal is a rectangular pulse train or square wave.

- Positive Going Transition (PGT) – when clock pulse goes from 0 to 1.



- Negative Going Transition (NGT) – when clock pulse goes from 1 to 0.



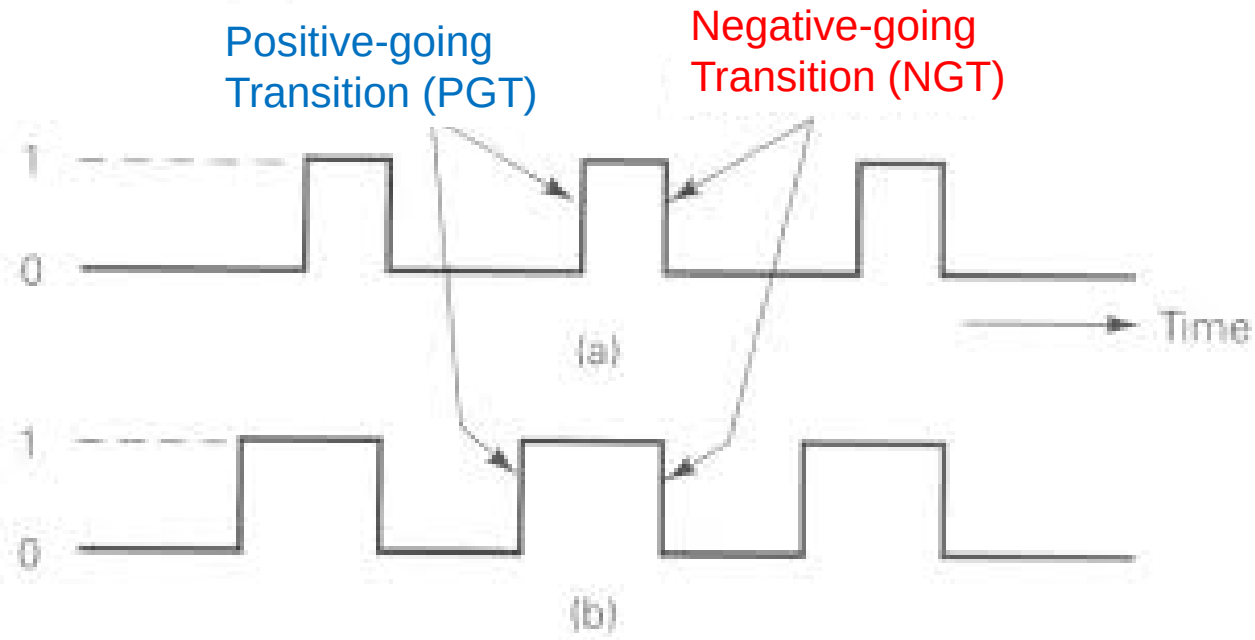
- The clock signal is a rectangular pulse train or square wave.

- Positive Going Transition (PGT) – when clock pulse goes from 0 to 1.

- Negative Going Transition (NGT) – when clock pulse goes from 1 to 0.

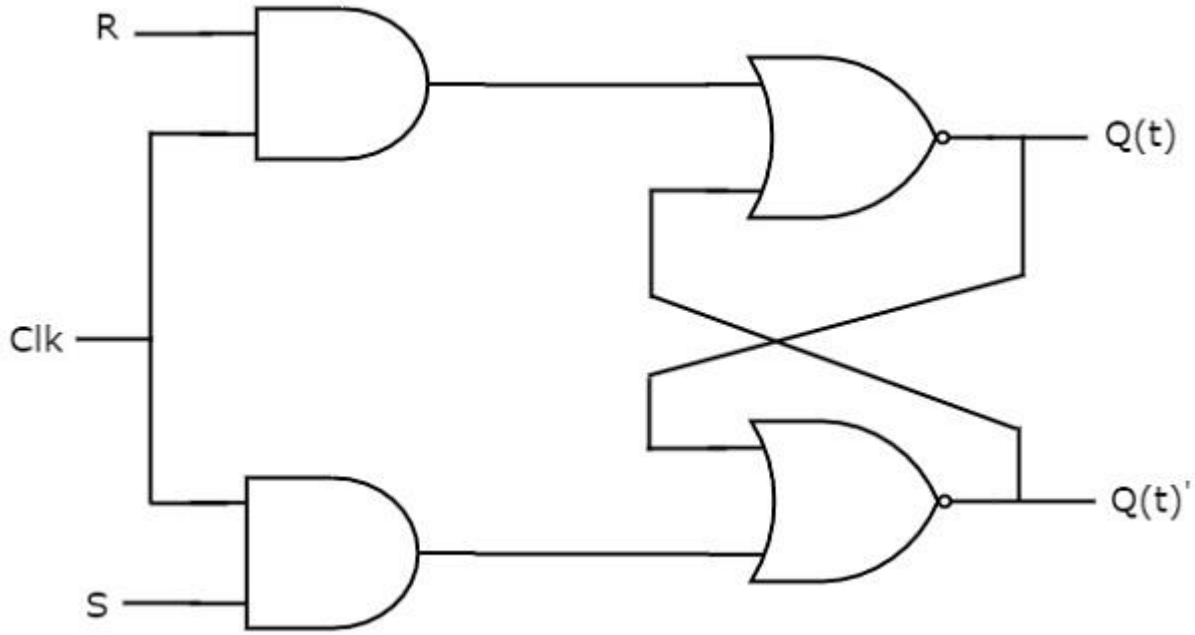
- **Transitions** are also called **edges**.

- It is the **edges** that are <u>important</u>, not the HI or LO portions.



Clock Signals and Clocked Flip-Flops

- Clocked FFs change state on one or the other clock transitions. Some common characteristics:
  1. Clock inputs are labeled CLK, CK, or CP.



Clock Signals and Clocked Flip-Flops

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  1. Clock inputs are labeled CLK, CK, or CP.
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  3. A bubble and a triangle indicates that the CLK input is activated with a NGT.

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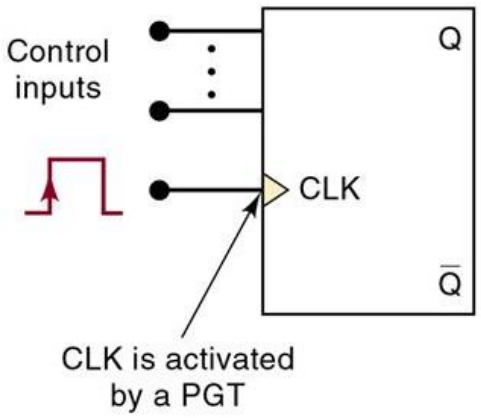
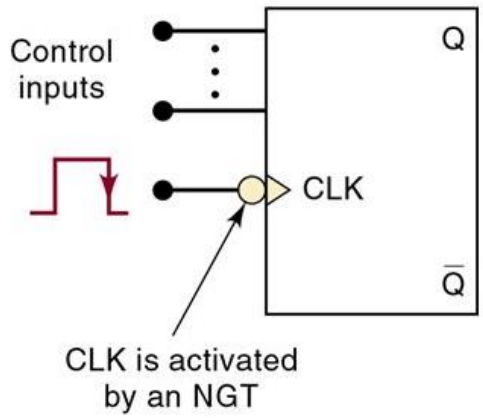


A bubble and a triangle indicates that the CLK input is activated with a NGT.



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  4. Control inputs have an effect on the output only at the active clock transition (NGT or PGT). These are also called synchronous control inputs.

Clock Signals and Clocked Flip-Flops

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  1. Clock inputs are labeled CLK, CK, or CP.
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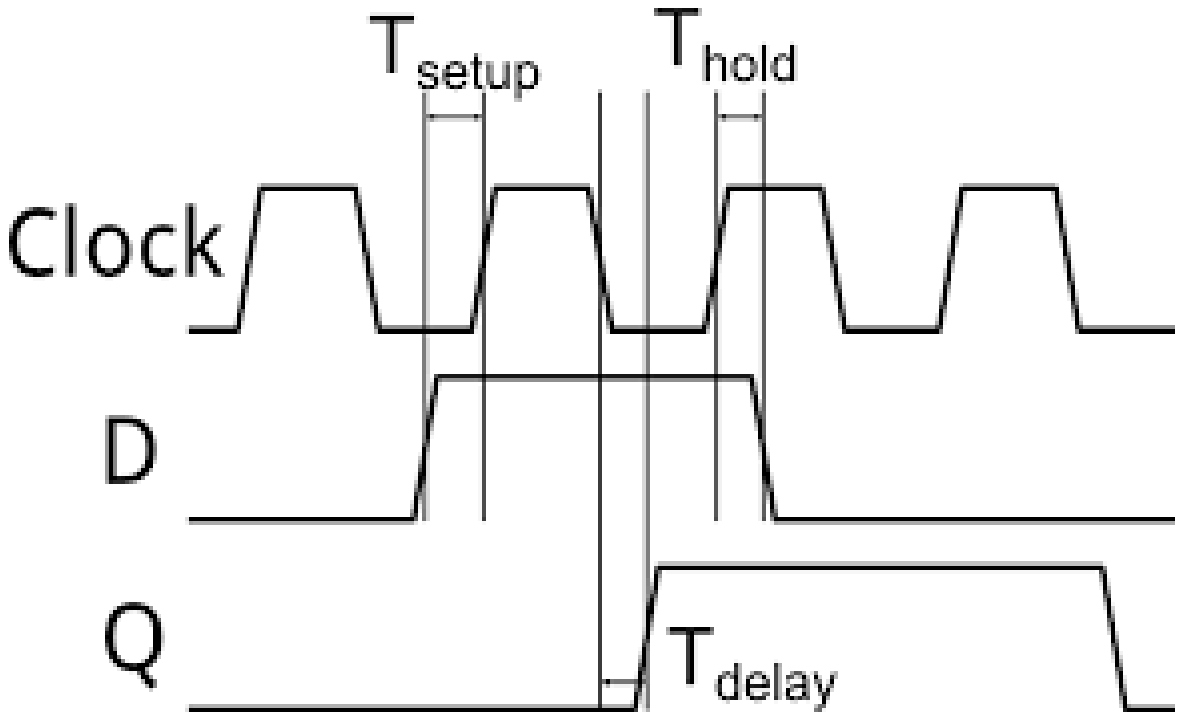
  3. A bubble and a triangle indicates that the CLK input is activated with a NGT.
  4. Control inputs have an effect on the output only at the active clock transition (NGT or PGT). These are also called synchronous control inputs.
  5. The control inputs get the FF outputs ready to change, but the change is not triggered until the CLK edge.

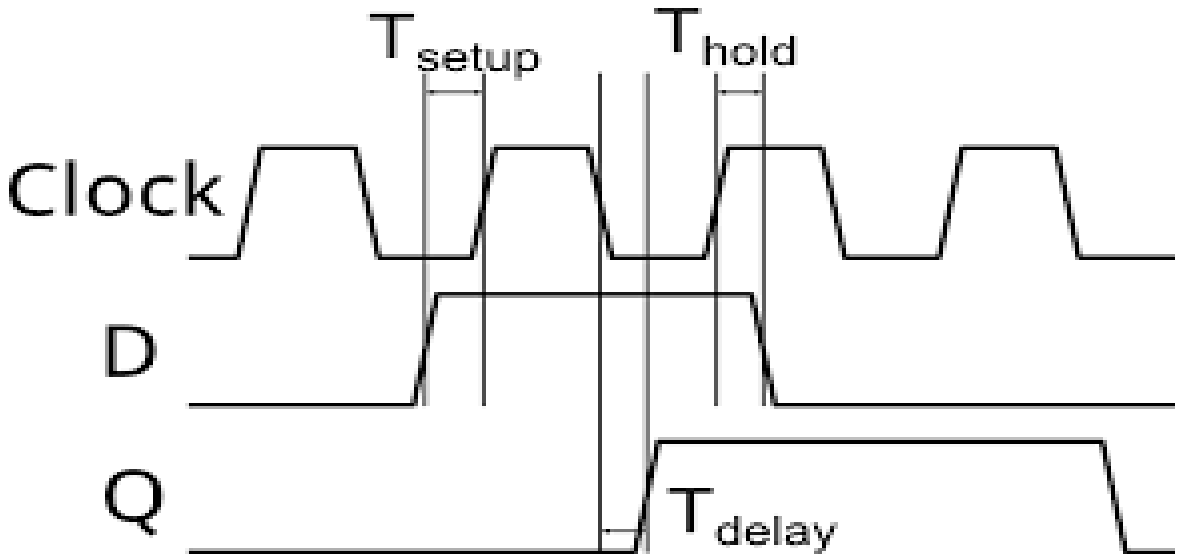
Clock Signals and Clocked Flip-Flops

- Setup time, T_S is the minimum time interval before the active CLK transition that the control input must be kept at the proper level.

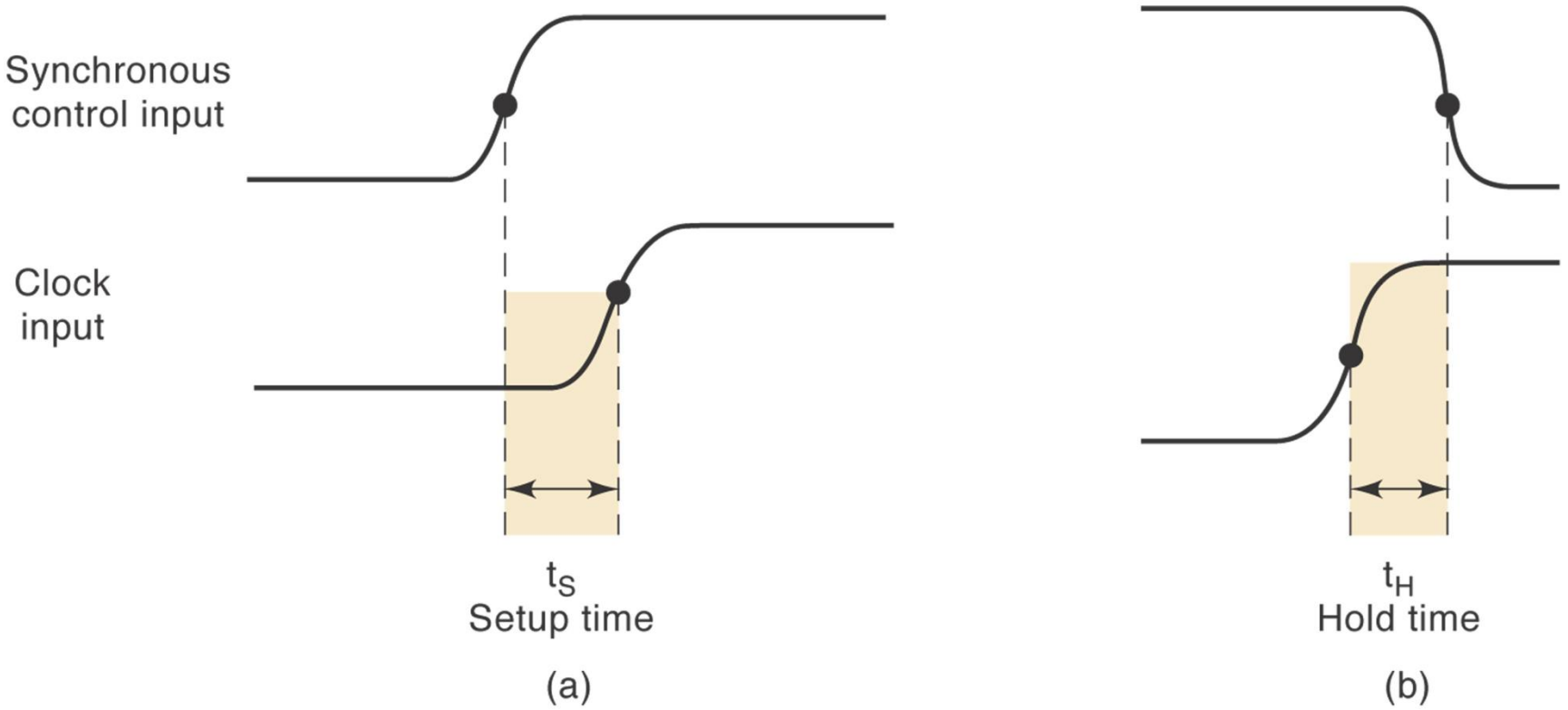


Clock Signals and Clocked Flip-Flops

- Setup time, T_S is the minimum time interval before the active CLK transition that the control input must be kept at the proper level.
- Hold time, T_H is the time following the active transition of the CLK during which the control input must kept at the proper level.

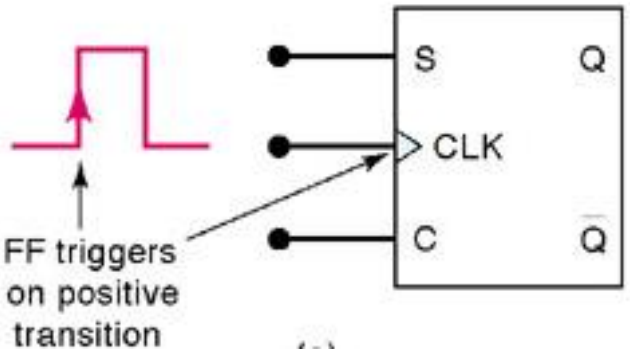


Setup and hold time



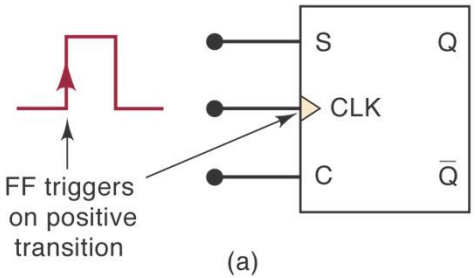
Clocked S-C Flip-Flop

- The set-clear (or set-reset) FF will change states at the positive going or negative going clock edge.
- (note: NOR implementation, active high)



Inputs			Output
S	C	CLK	Q
0	0	↑	Q_0 (no change)
1	0	↑	1
0	1	↑	0
1	1	↑	Ambiguous

Q_0 is output level prior to ↑ of CLK.
↓ of CLK produces no change in Q.

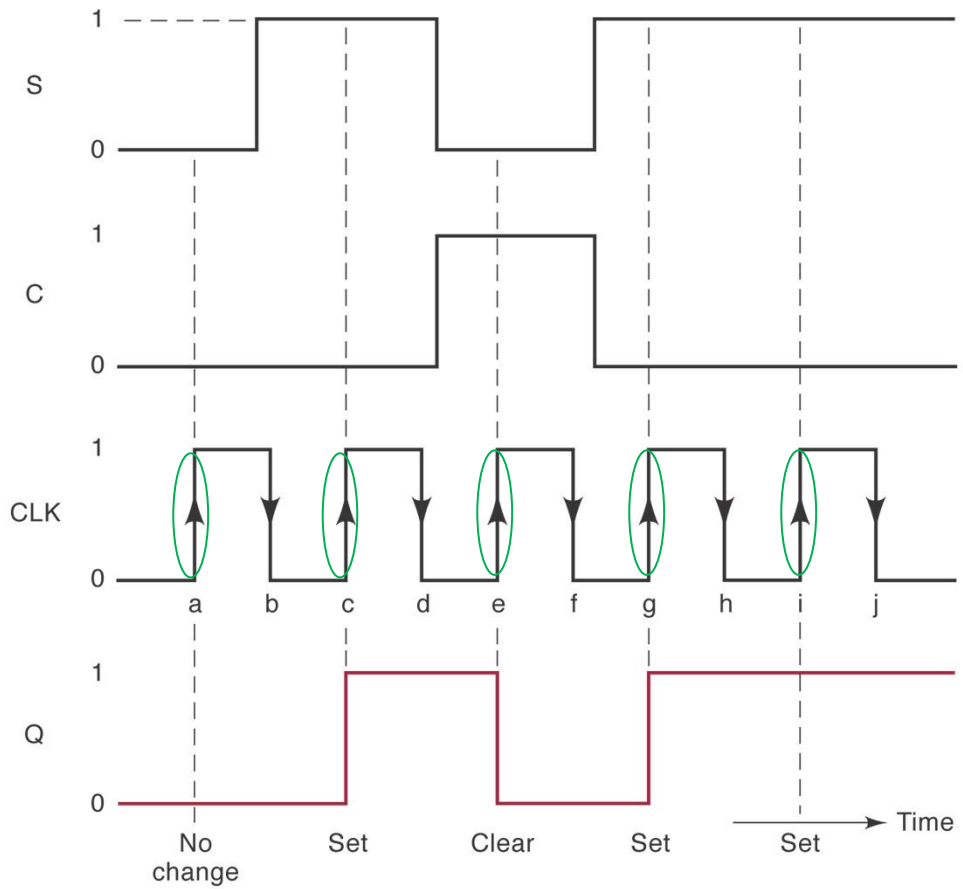


(a)

Inputs			Output
S	C	CLK	Q
0	0	↑	Q_0 (no change)
1	0	↑	1
0	1	↑	0
1	1	↑	Ambiguous

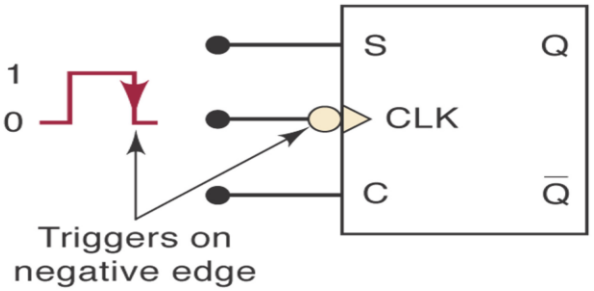
Q_0 is output level prior to ↑ of CLK.
↓ of CLK produces no change in Q.

(b)

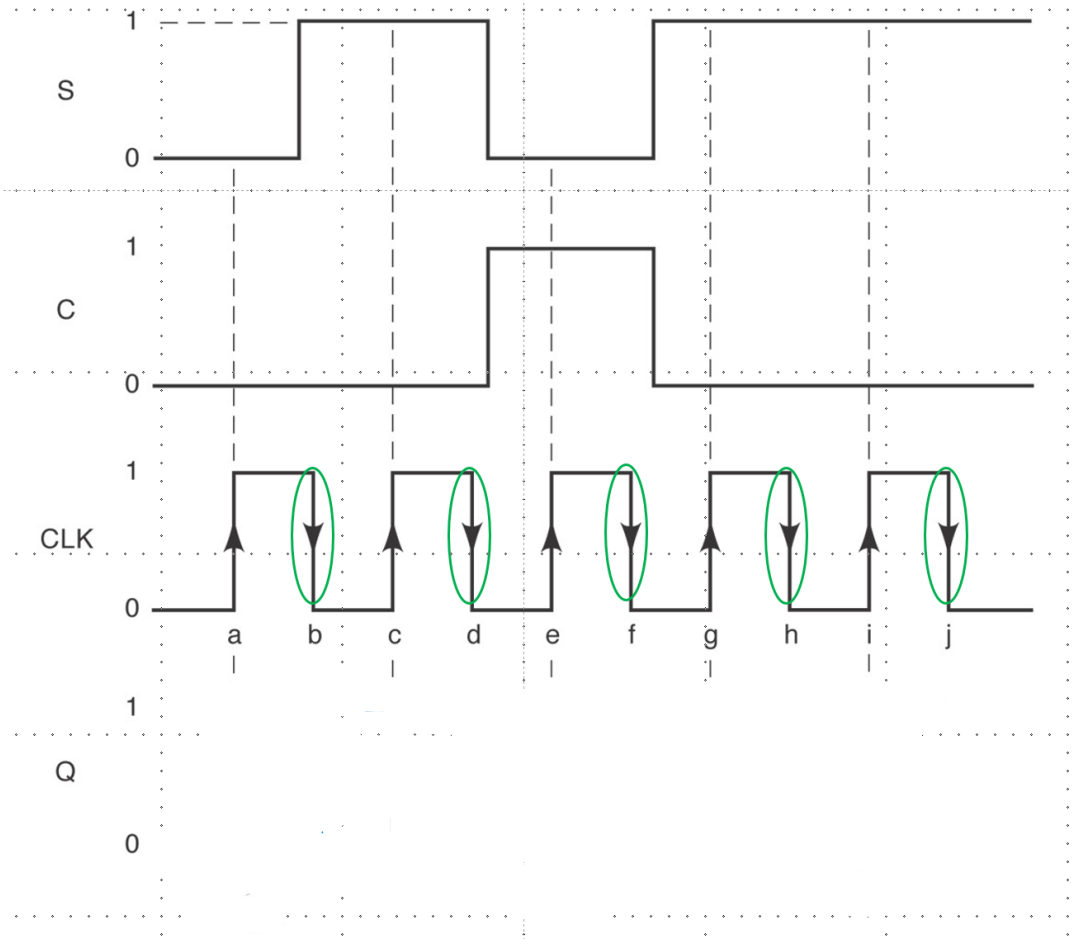


(c)

Negative –edge clocked S-C flip-flop.



Inputs			Output
S	C	CLK	Q
0	0	↓	Q_0 (no change)
1	0	↓	1
0	1	↓	0
1	1	↓	Ambiguous



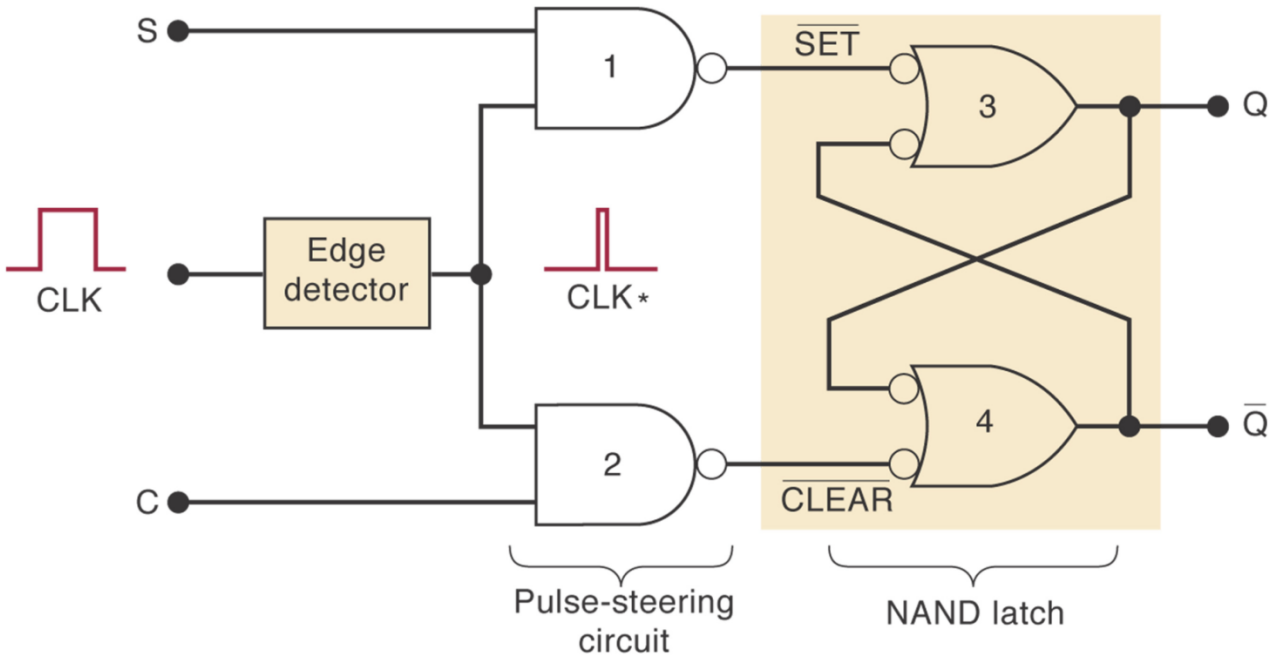
Internal circuitry of the edge triggered S-C FF

Consists of three different sections:

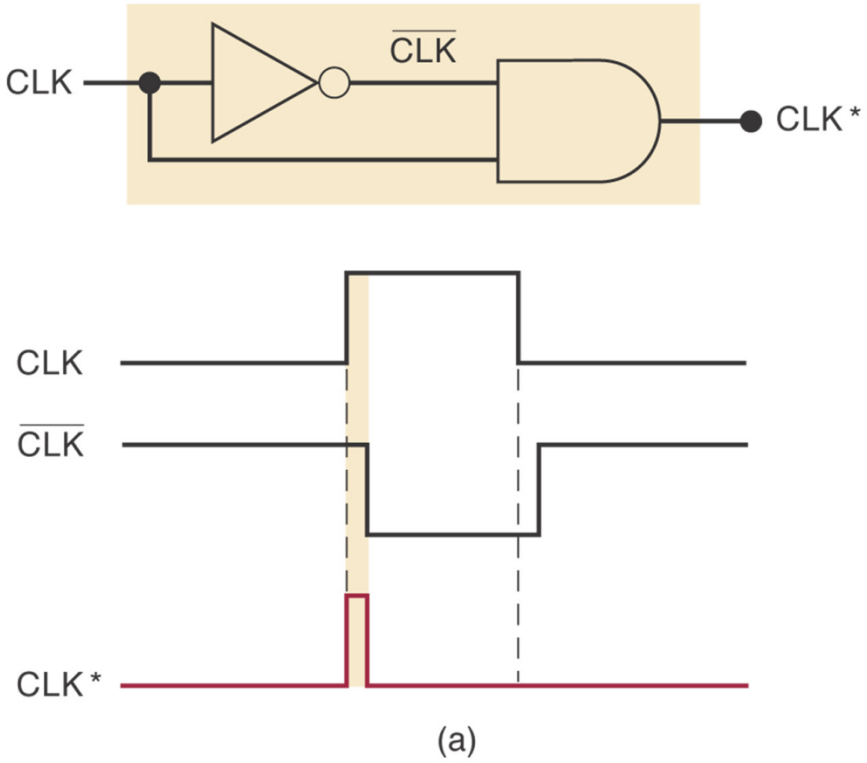
1. A basic NAND gate latch (NAND 3 and NAND 4)

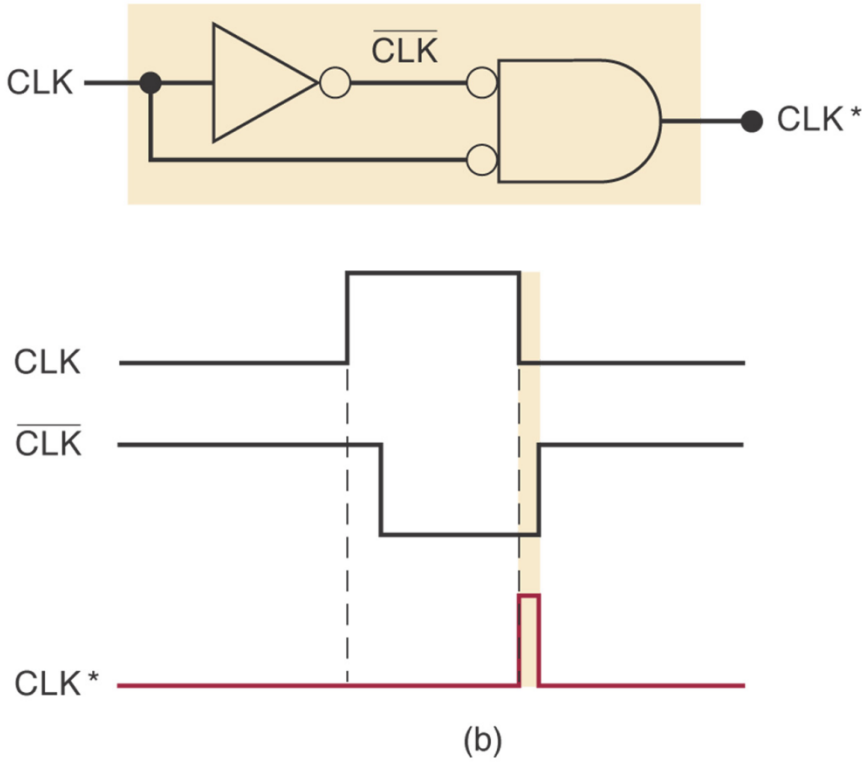
2. Pulse steering circuit (NAND 1 and NAND 2)

3. Edge detector circuit



Edge detector circuits.





PGT

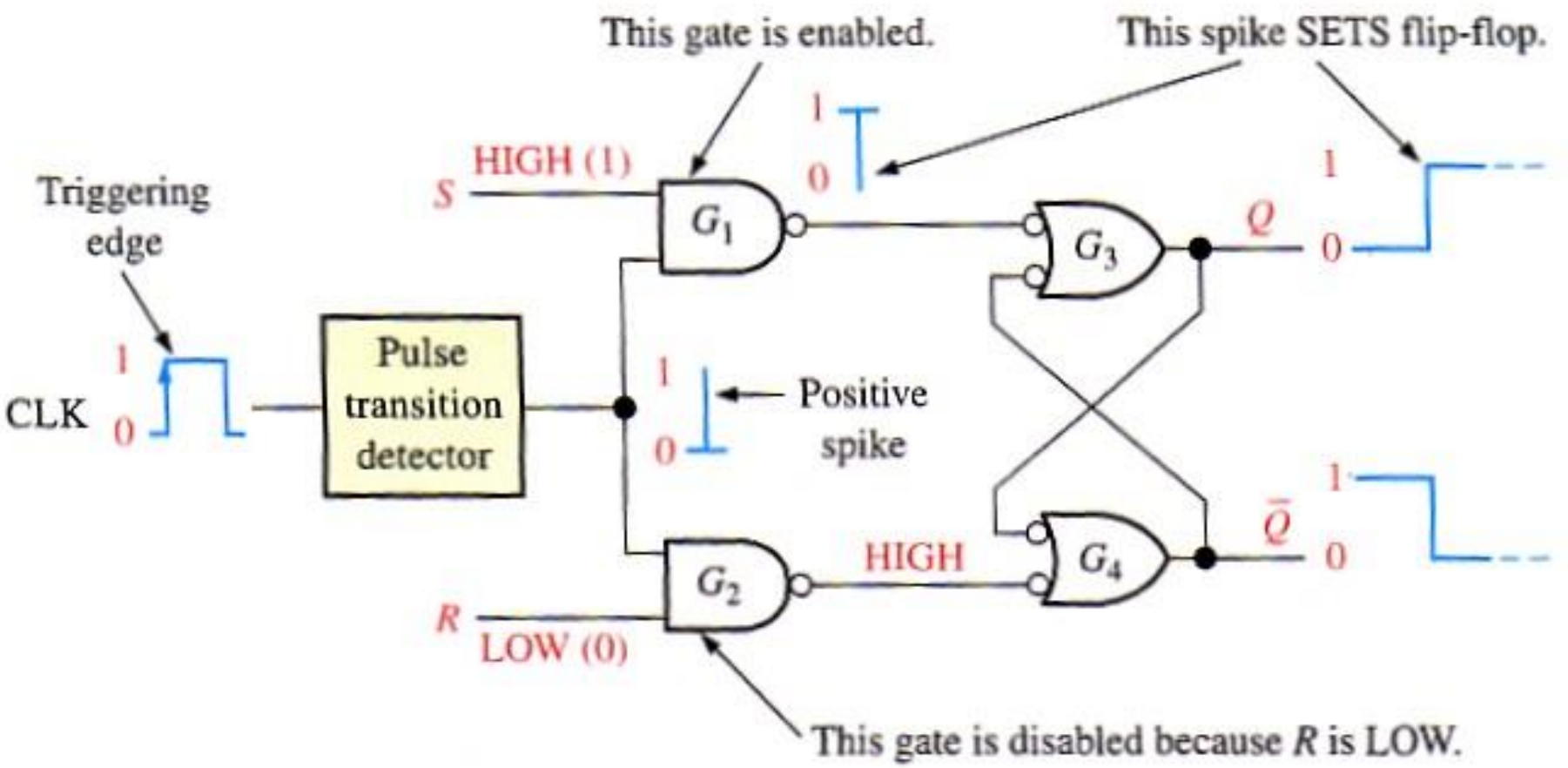
Positive Going Transition

NGT

Negative Going Transition

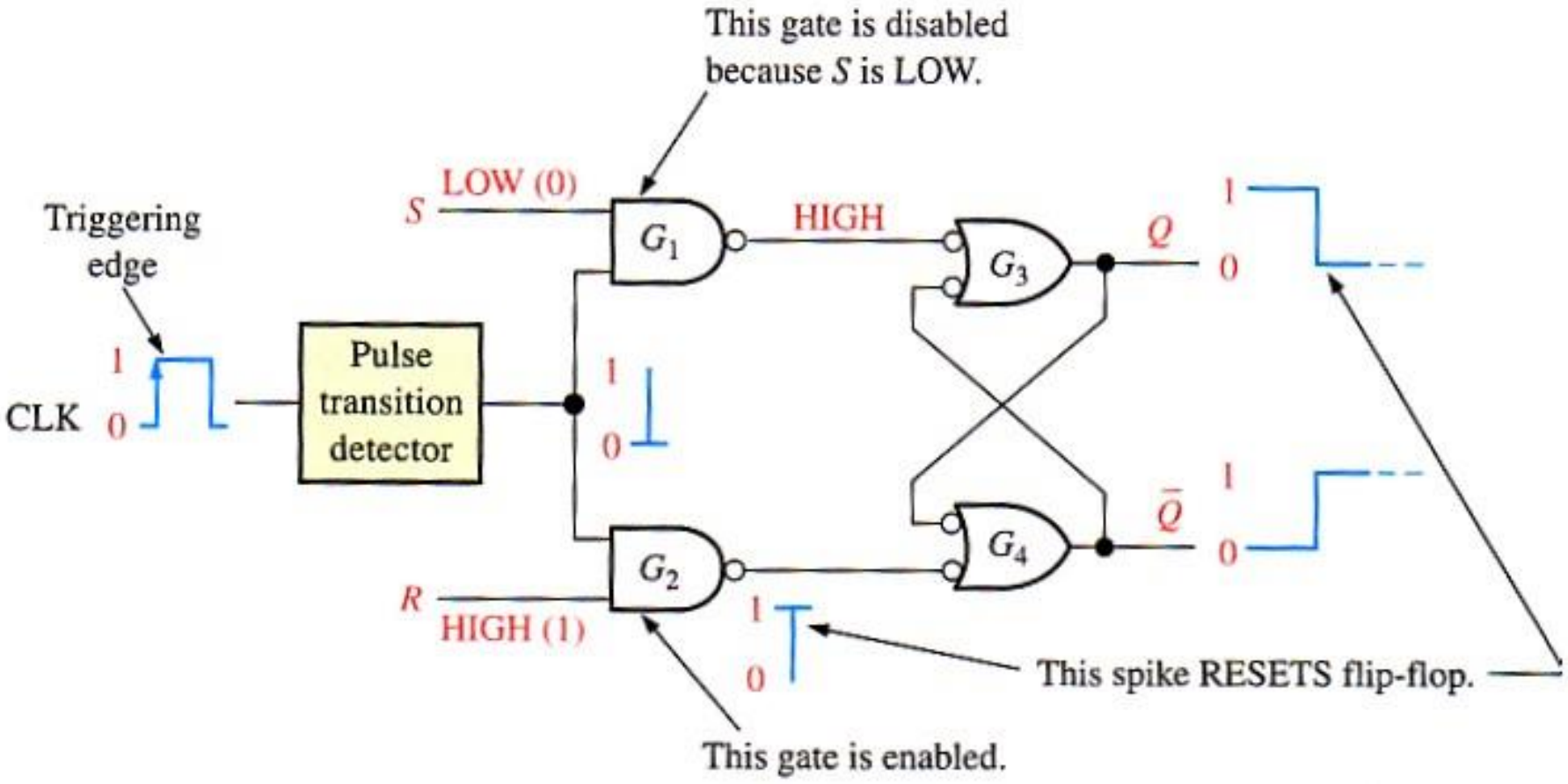
FF making transition from RESET to SET on PGT of clock

The S and R (another label for Clear) inputs to the FF below is active HI – **The inputs to the NAND latch is still active LO**.



FF making transition from SET to RESET on the PGT of clock.

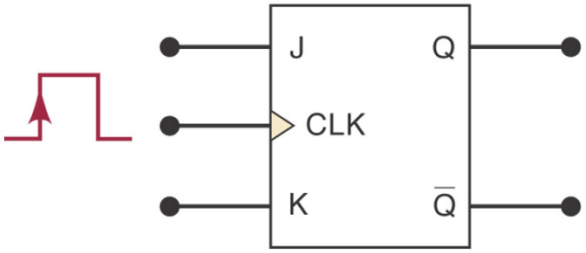
The S and R (another label for Clear) inputs to the FF below is active HI – **The inputs to the NAND latch is still active LO**.



Clocked J-K Flip-Flop

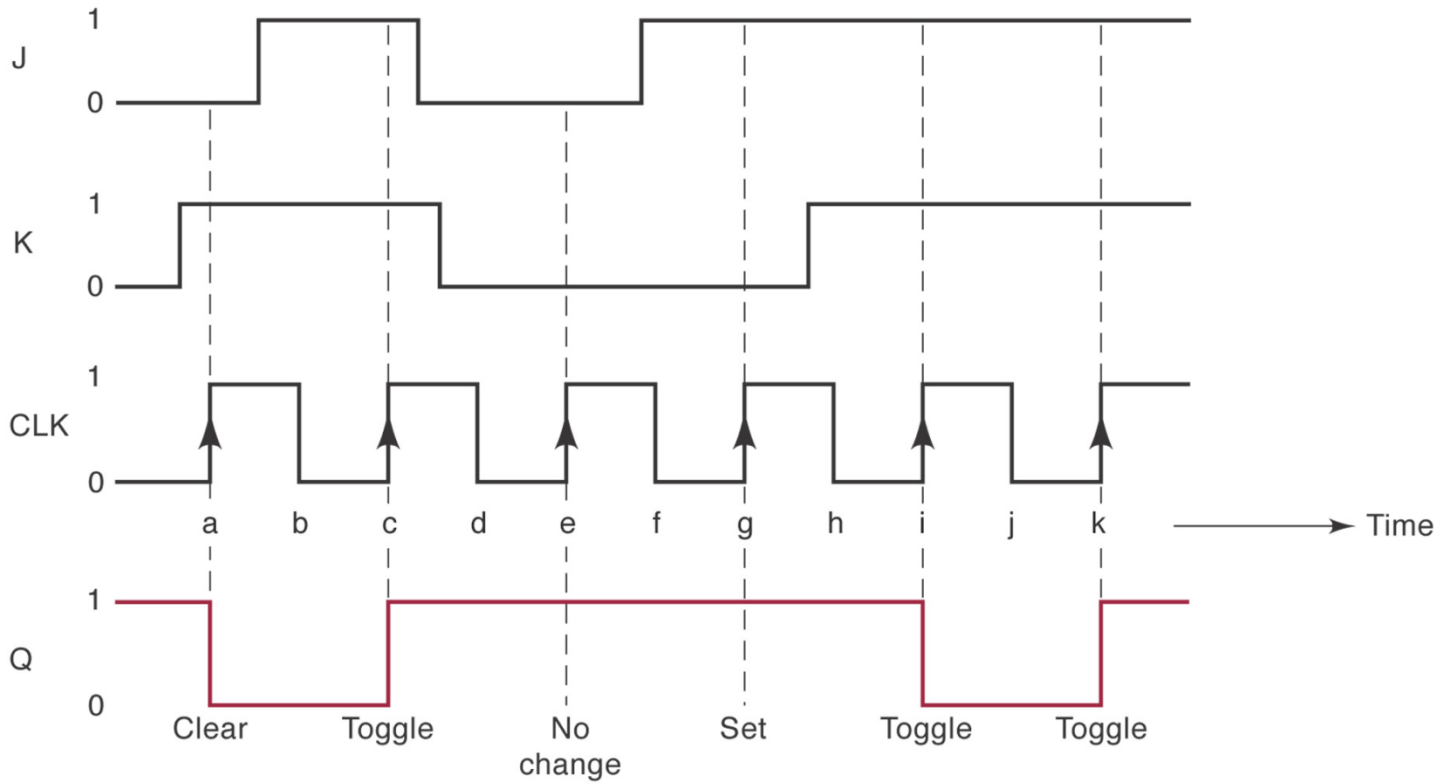
- Overcomes the disallowed state of S-C FF.
- Operates like S-C FF, but with J = set and K= clear.
- When J and K are both HI, the output is toggled from whatever state it is in to the opposite state.
- May be positive or negative going clock trigger.
- Has the ability to do everything the S-C FF does, plus operate in toggle mode.

Clocked J-K Flip Flop (triggers on PGT)



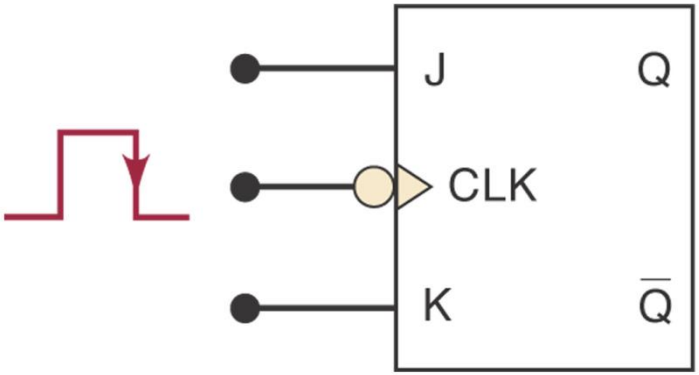
J	K	CLK	Q
0	0	↑	Q_0 (no change)
1	0	↑	1
0	1	↑	0
1	1	↑	$\overline{Q}_0$ (toggles)

(a)

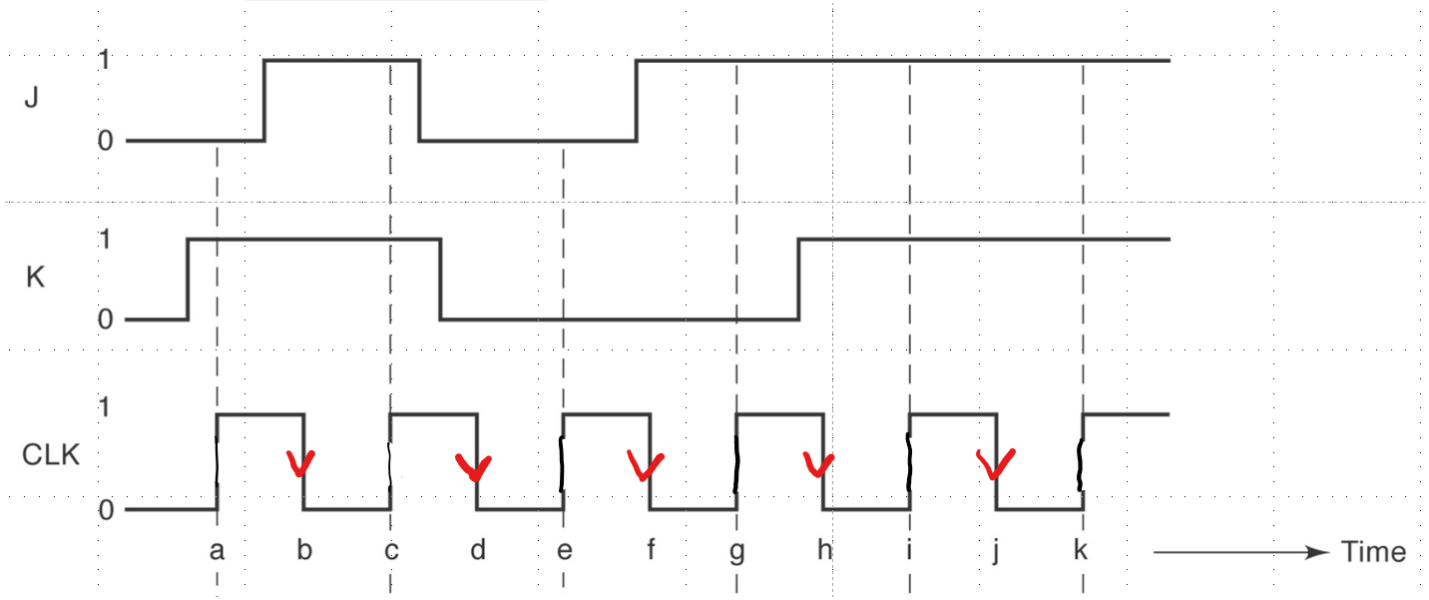


(b)

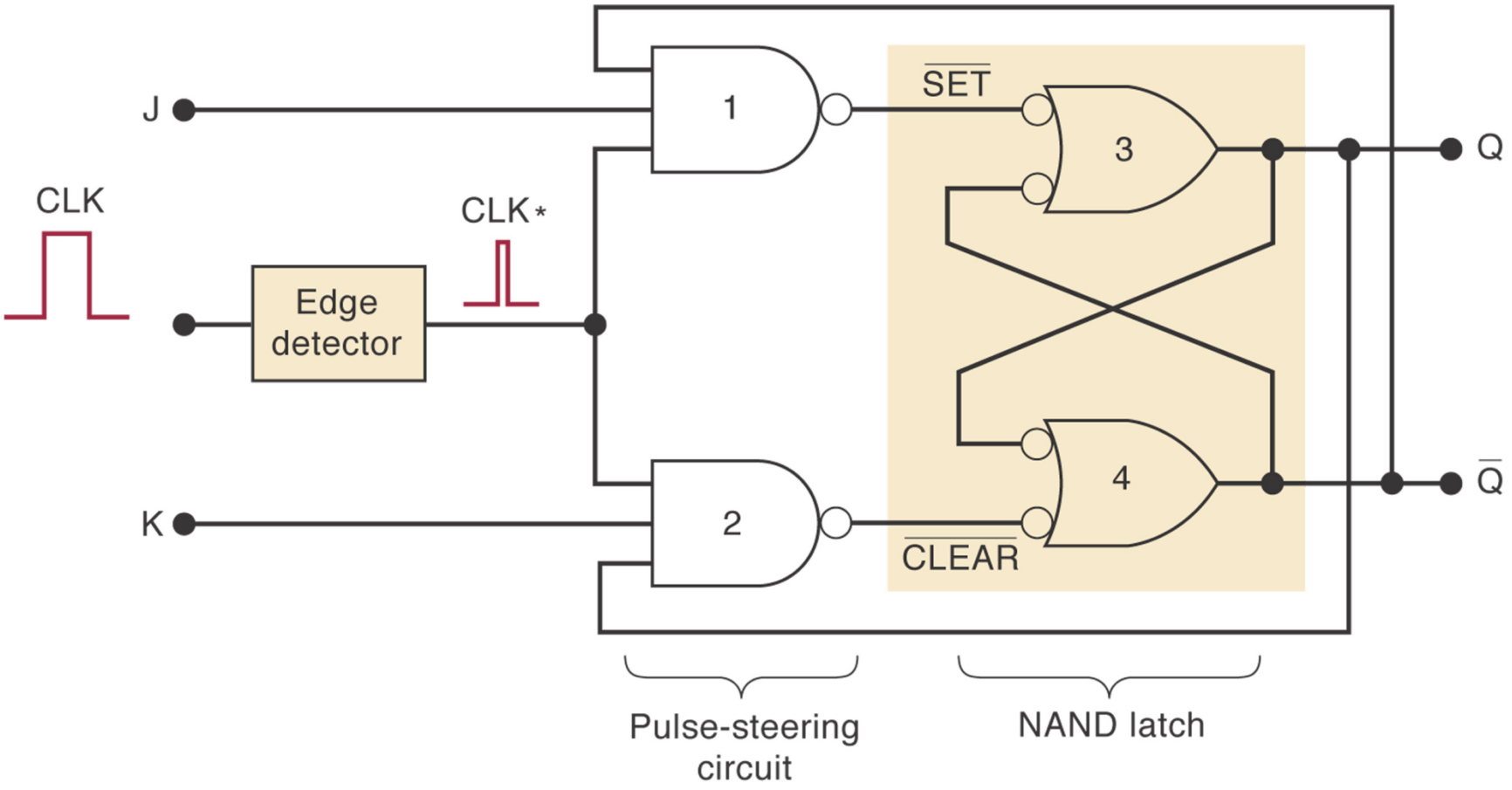
J-K flip flop triggering on NGT



J	K	CLK	Q
0	0	↓	Q_0 (no change)
1	0	↓	1
0	1	↓	0
1	1	↓	$\overline{Q_0}$ (toggles)



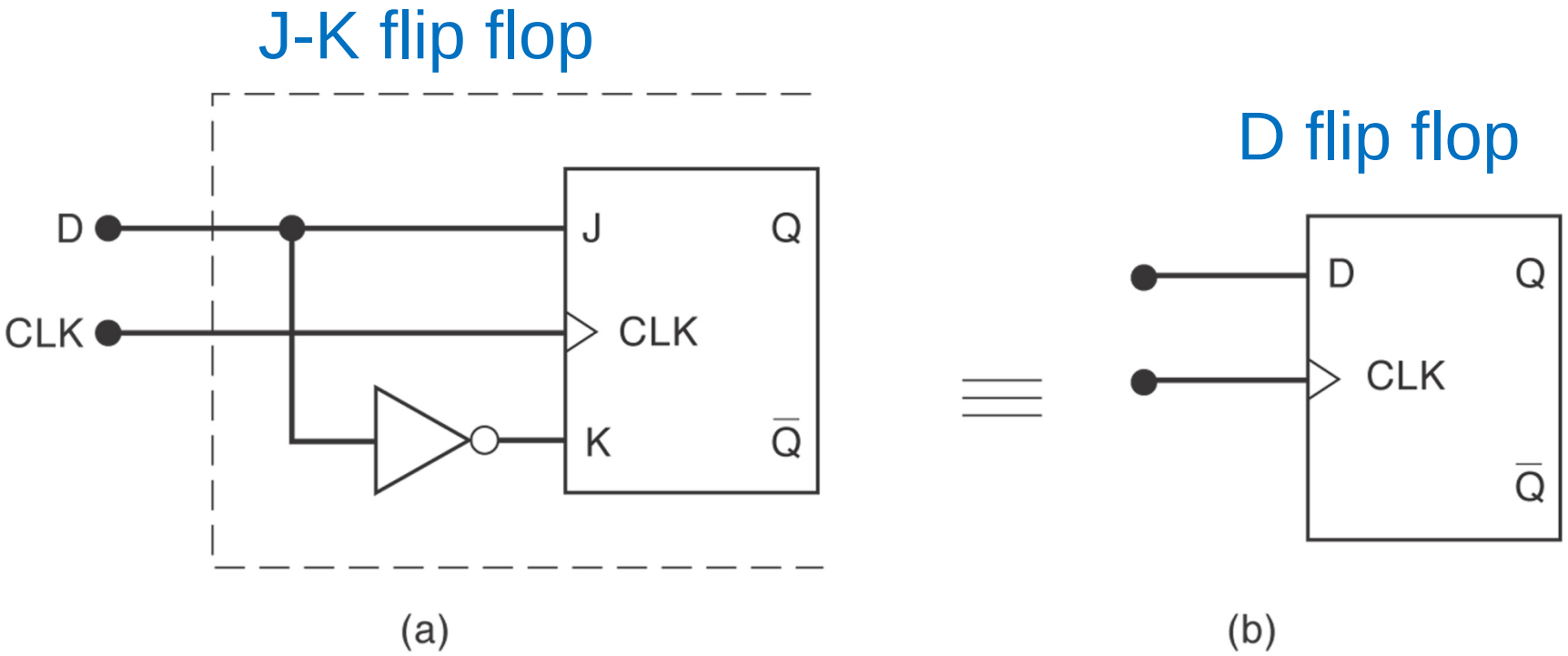
Internal circuitry of edge triggered J-K flip flop.



Clocked D Flip-Flop

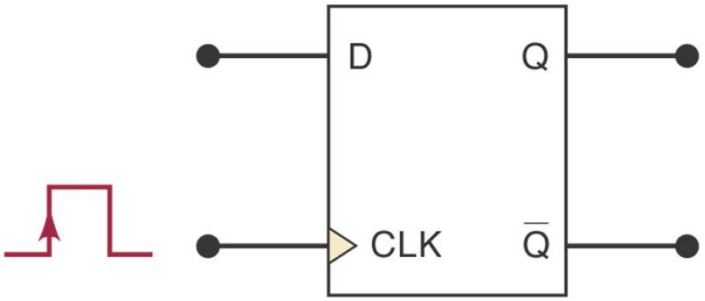
- One data input.
- The output changes to the value of the input at either the positive going or negative going clock trigger (device dependent) .
- May be implemented with a J-K FF by tying the J input to the K input through an inverter.
- Useful for parallel data transfer.

D FF implementation from a J-K FF



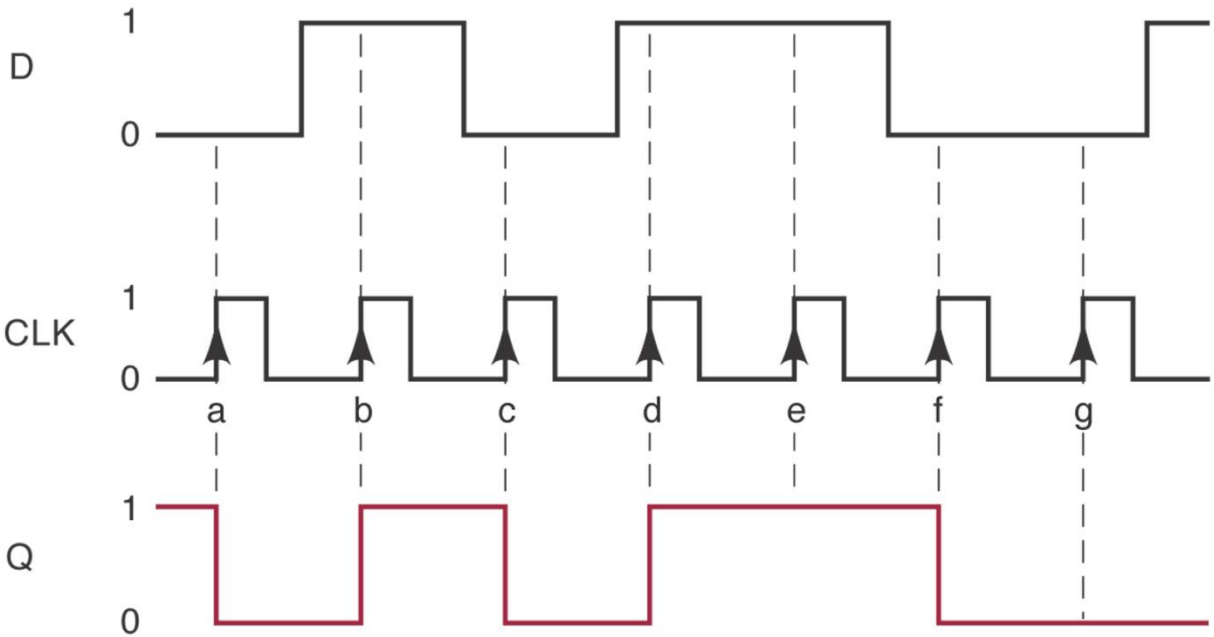
D flip flop triggering on PGT's

Q is always the same as D
but updates on PGT only



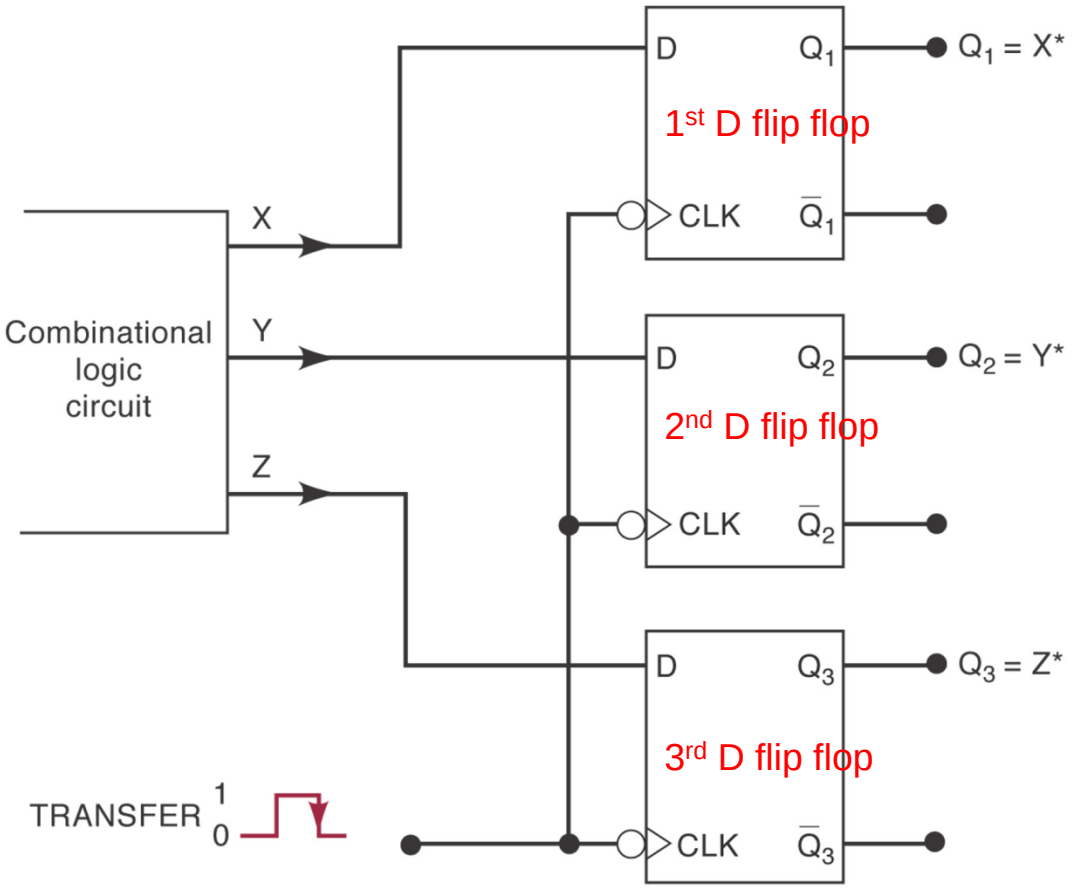
(a)

D	CLK	Q
0	↑	0
1	↑	1



(b)

Parallel data transfer using D flip flops.

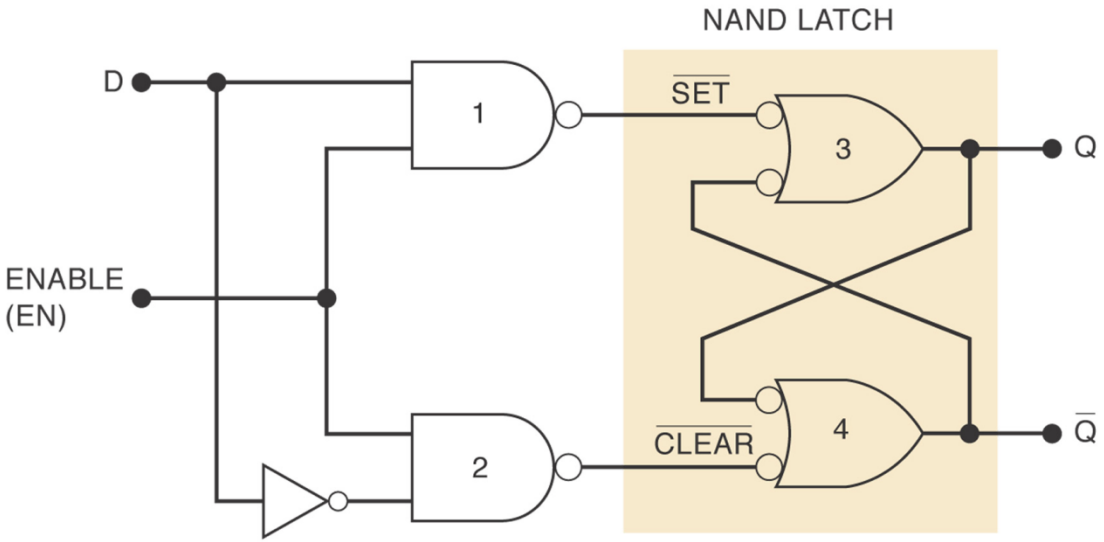


*After occurrence of NGT

D Latch (Transparent Latch)

- One data input.
- The clock has been replaced by an enable (EN) line.
- The device is NOT edge triggered.
- The output follows the input only when EN is active.

Structure of the D latch

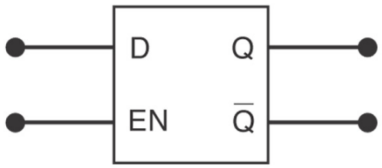


(a)

Inputs		Output
EN	D	Q
0	X	Q_0 (no change)
1	0	0
1	1	1

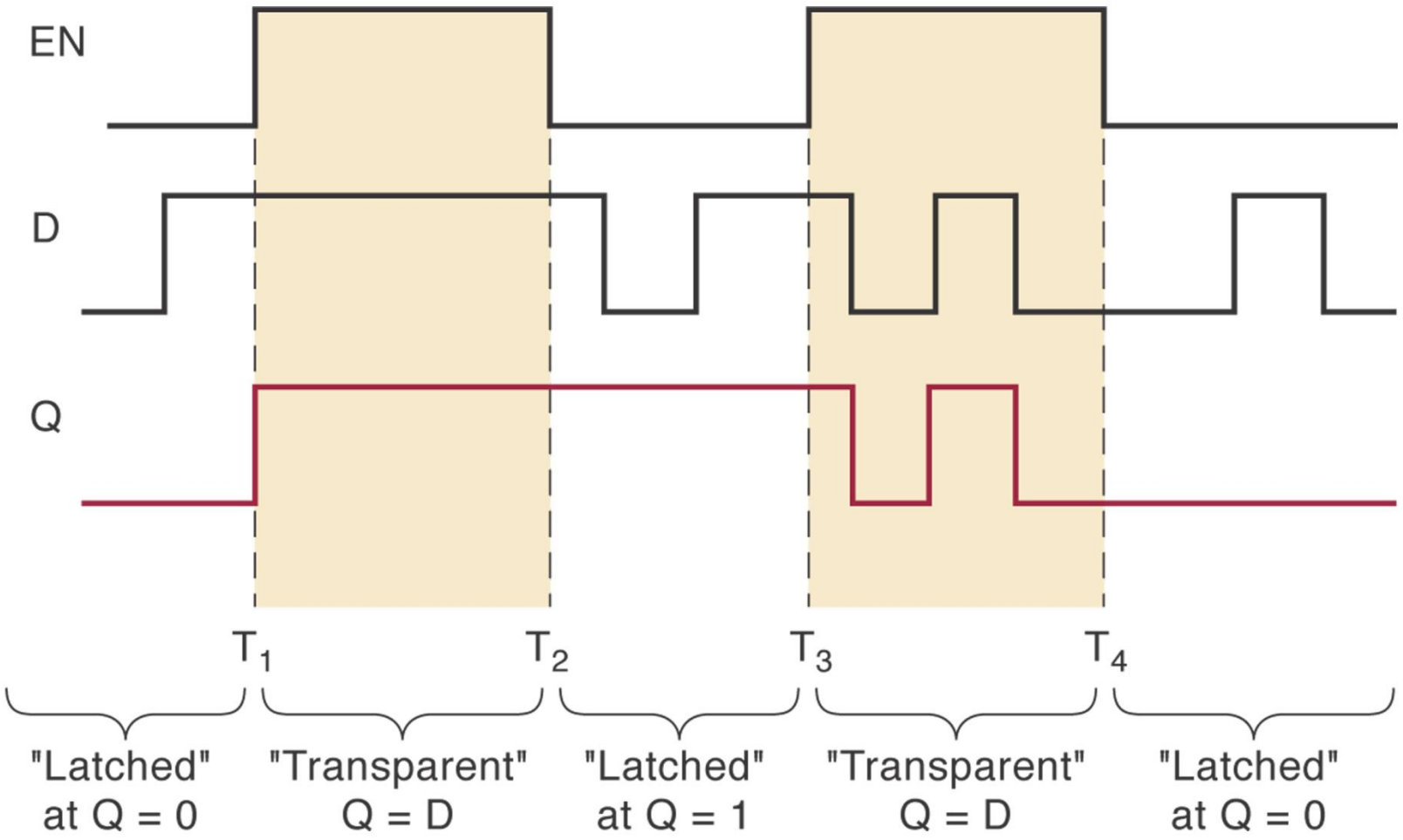
"X" indicates "don't care."
Q_0 is state Q just prior to EN going LOW.

(b)



(c)

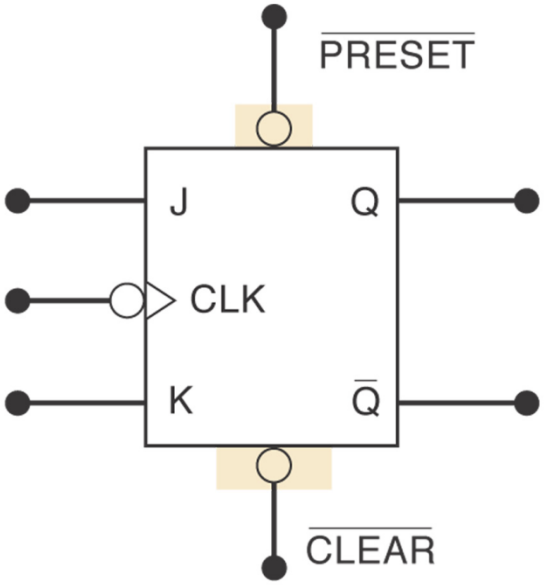
Operation of the D latch



Asynchronous Inputs

- Inputs that depend on the clock are synchronous.
- Most clocked FFs have additional asynchronous inputs that do not depend on the clock.
- These I/P's are used to preset (Q = 1) or clear (Q = 0) the FF – Active regardless of the state of the other I/P's.
- Also called override inputs.
- If the asynchronous inputs are not used they will be tied to their inactive state.

Clocked J-K FF with asynchronous inputs.

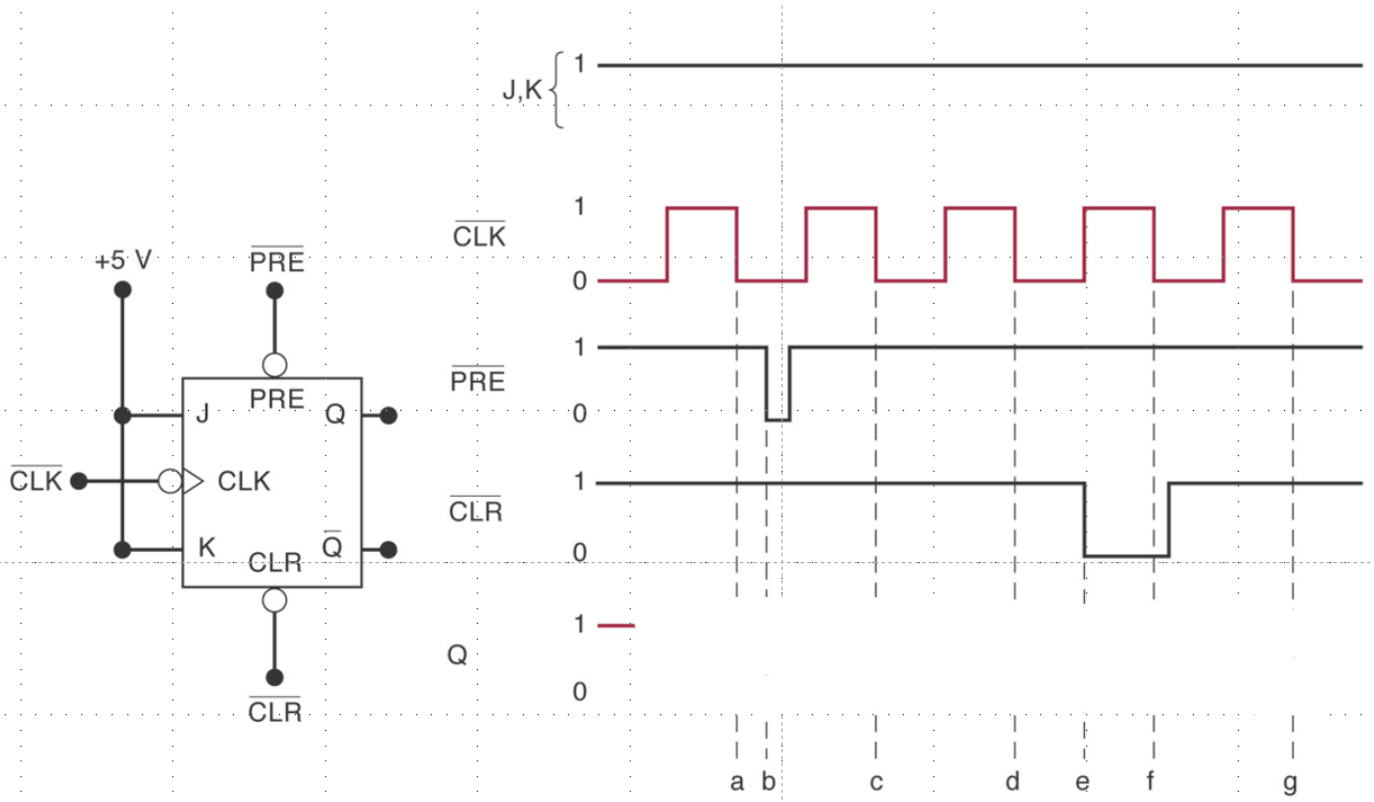


PRESET	CLEAR	FF response
1	1	Clocked operation*
0	1	Q = 1 (regardless of CLK)
1	0	Q = 0 (regardless of CLK)
0	0	Not used

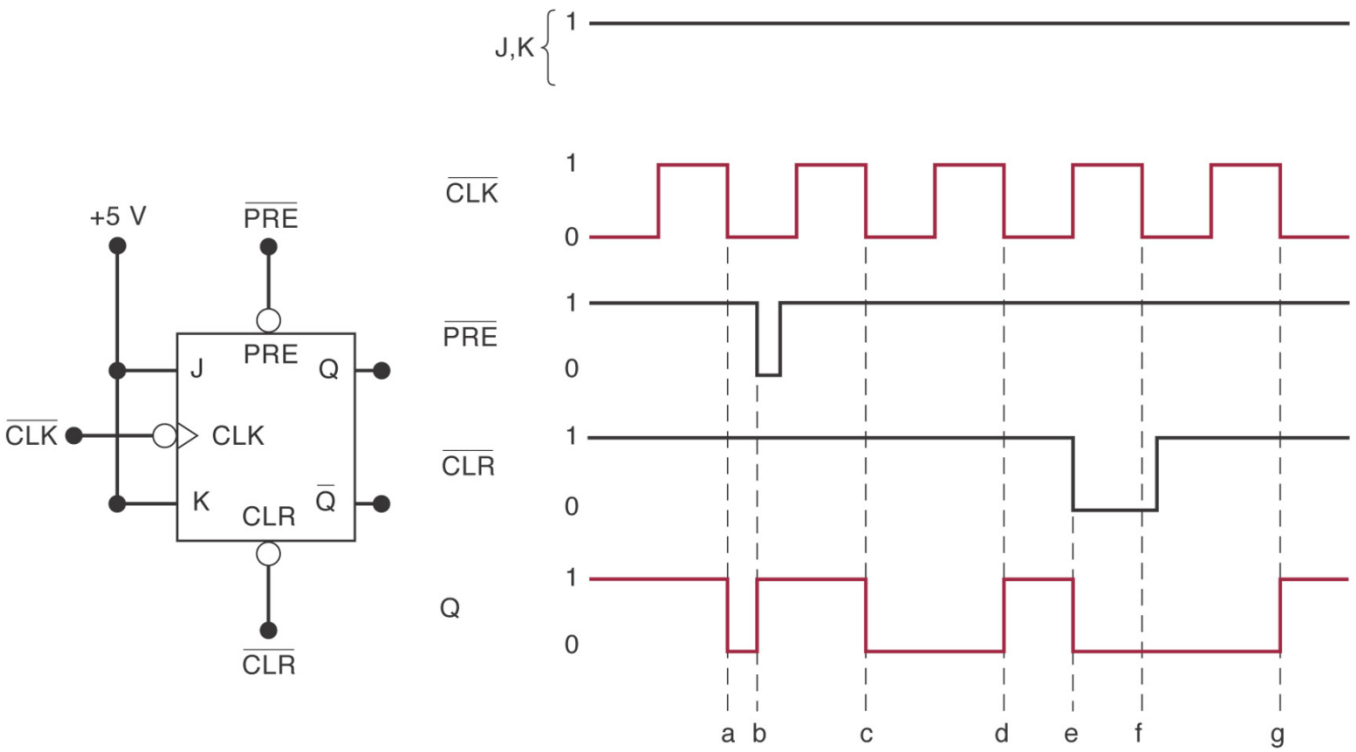
*Q will respond to J, K, and CLK.

- The labels PRE and CLR are used for asynchronous inputs.
- Active low asynchronous inputs will have a bar over the labels and inversion bubbles.

Clocked FF responding to asynchronous inputs



Clocked FF responding to asynchronous inputs



Point	Operation
a	Synchronous toggle on NGT of $\overline{CLK}$
b	Asynchronous set on $\overline{PRE}$ = 0
c	Synchronous toggle
d	Synchronous toggle
e	Asynchronous clear on $\overline{CLR}$ = 0
f	$\overline{CLR}$ overrides the NGT of $\overline{CLK}$
g	Synchronous toggle

(b)

IEEE/ANSI Symbols

- Note the differences in the representations below.