XMUT 202
Digital Electronics

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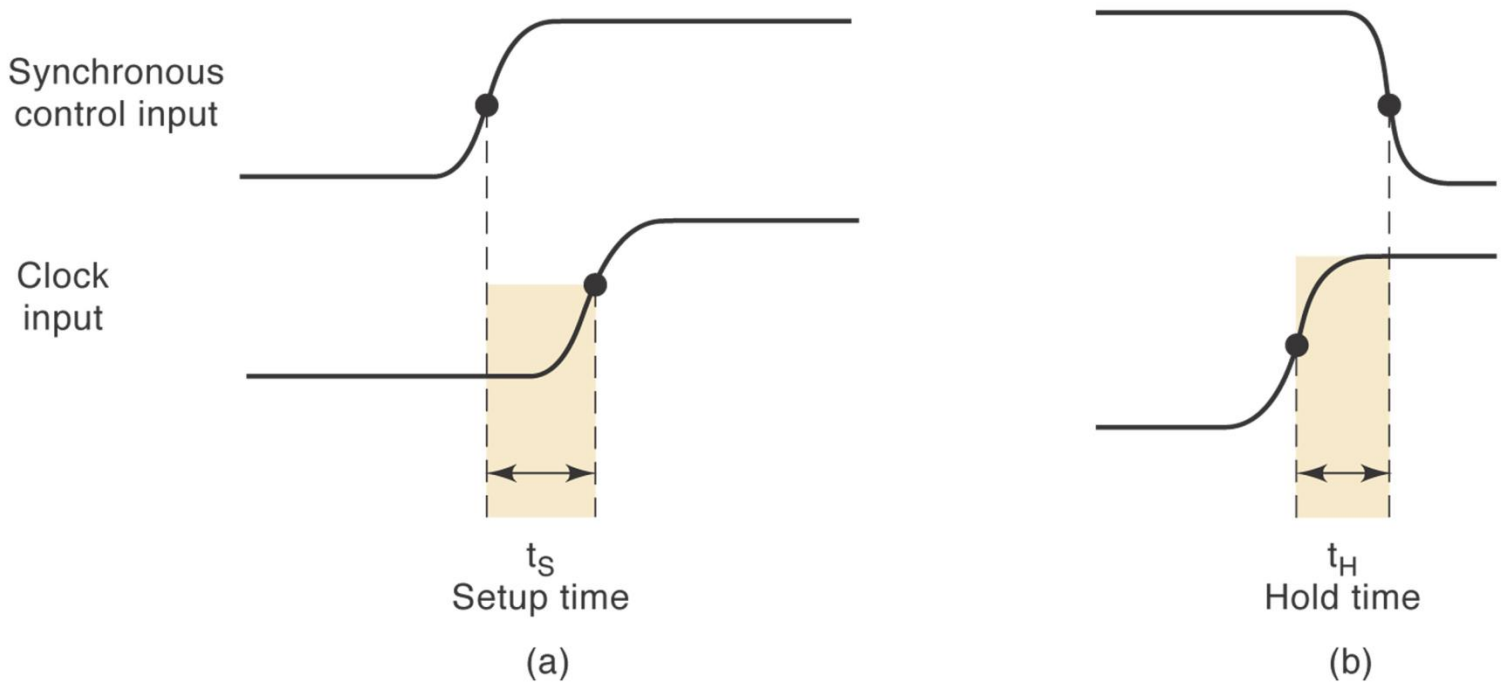
Week 12 Lecture 1

1. A bit more on Flip Flops
    1. Timing considerations
    2. Applications
2. Schmitt-Trigger Devices
3. Multivibrators
    1. Bistable
    2. Monostable
    3. Astable

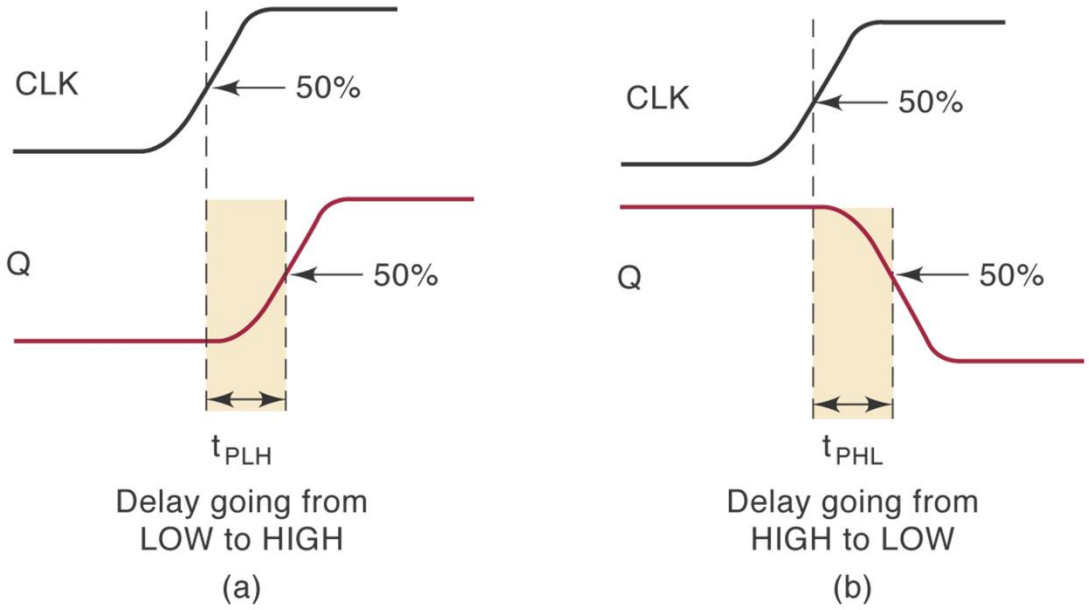
Flip-Flop Timing Considerations

- Important timing parameters:
  1. Setup and hold times (already discussed)



Flip-Flop Timing Considerations

2. Propagation delay – the time for a signal at the input to be shown at the output.



- Specifies maximum value
- Typically 5 – 100 ns

Flip-Flop Timing Considerations

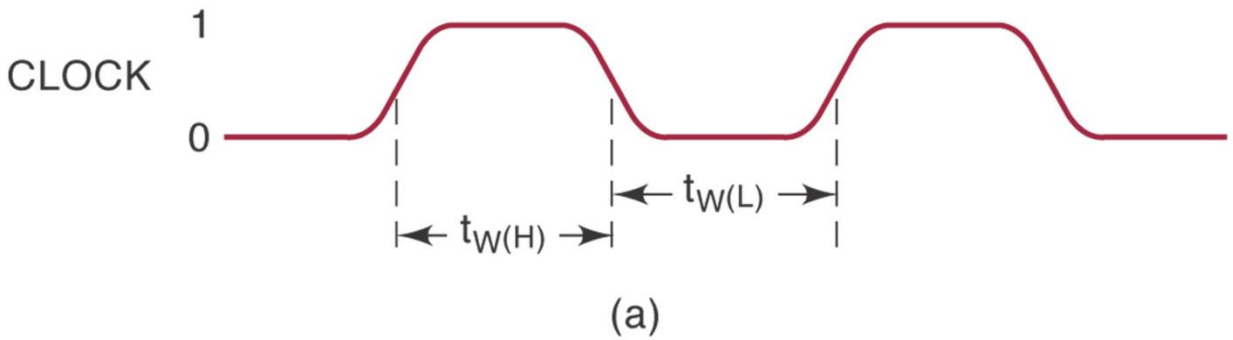
3. Maximum clocking frequency – highest clock frequency that will give a reliable output.

May vary considerably between similar devices

Manufacturer will specify lowest frequency that will give reliable operation.

Flip-Flop Timing Considerations

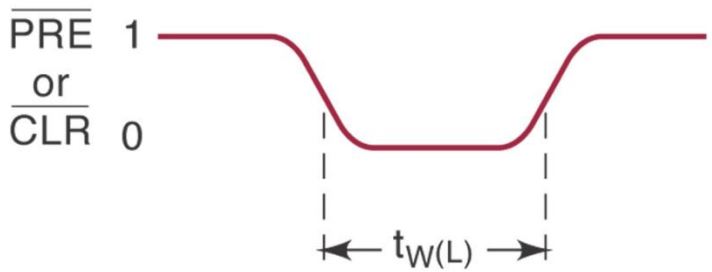
4. Clock pulse high and low times – minimum time that clock must high before going low, and low before going high.



(a)

Flip-Flop Timing Considerations

5. Asynchronous active pulse width – the minimum time PRESET or CLEAR must be held for the FF to set or clear reliably.



(b)

Flip-Flop Timing Considerations

6. Clock transition times – maximum time for the clock transitions, generally less than 50 ns for TTL or 200 ns for CMOS devices.

		TTL		CMOS	
		7474	74LS112	74C74	74HC112
t_S		20	20	60	25
t_H		5	0	0	0
t_{PHL}	from *CLK* to *Q*	40	24	200	31
t_{PLH}	from *CLK* to *Q*	25	16	200	31
t_{PHL}	from $\overline{CLR}$ to *Q*	40	24	225	41
t_{PLH}	from $\overline{PRE}$ to *Q*	25	16	225	41
$t_W(L)$	*CLK* LOW time	37	15	100	25
$t_W(H)$	*CLK* HIGH time	30	20	100	25
$t_W(L)$	at $\overline{PRE}$ or $\overline{CLR}$	30	15	60	25
f_{MAX}	in MHz	15	30	5	20

(a) Assume that $Q = 0$. How long can it take for Q to go HIGH when a PGT occurs at the *CLK* input of a 7474?

(b) Assume that $Q = 1$. How long can it take for Q to go LOW in response to the $\overline{CLR}$ input of a 74HC112?

(c) What is the narrowest pulse that should be applied to the $\overline{CLR}$ input of the 74LS112 FF to clear Q reliably?

(d) Which FF in Table 5-2 requires that the control inputs remain stable *after* the occurrence of the active clock transition?

(e) For which FFs must the control inputs be held stable for a minimum time prior to the active clock transition?

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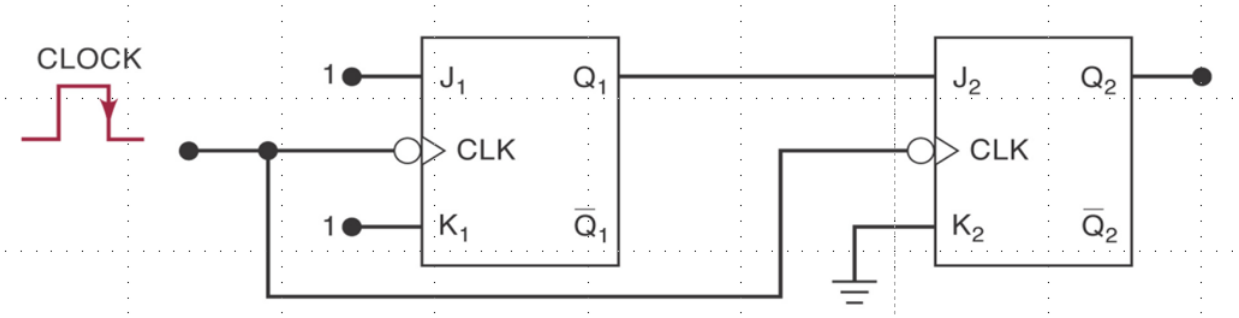
Potential Timing Problems in FF Circuits

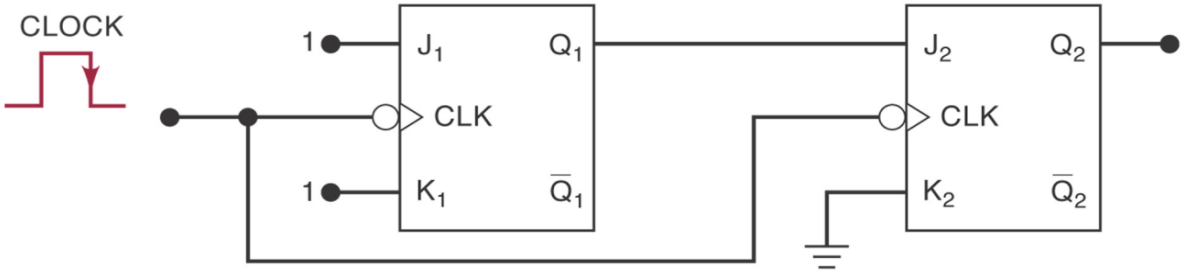
- When the output of one FF is connected to the input of another FF and both devices are triggered by the same clock, there is a potential timing problem.
- Propagation delay may cause unpredictable outputs.
- The low hold time parameter of most FFs mean this won’t normally be a problem.

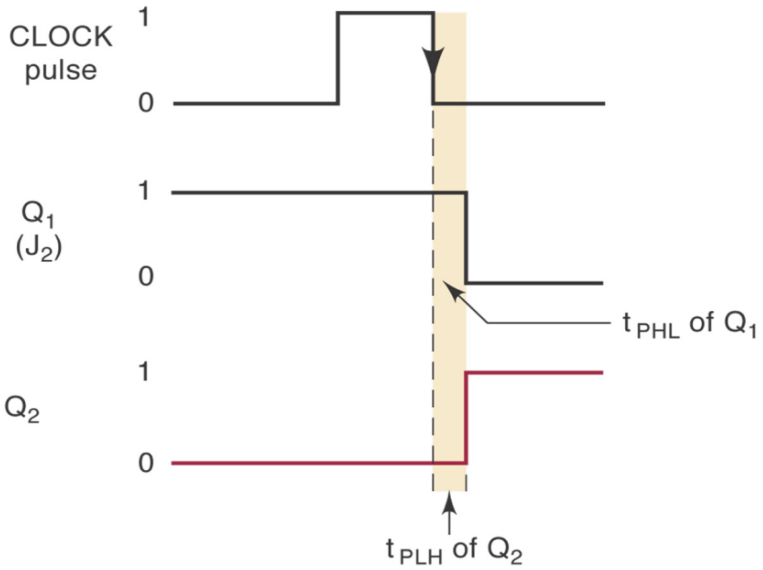
Potential timing problems



Assume Q_1=1, Q_2=0 initially

Potential timing problems





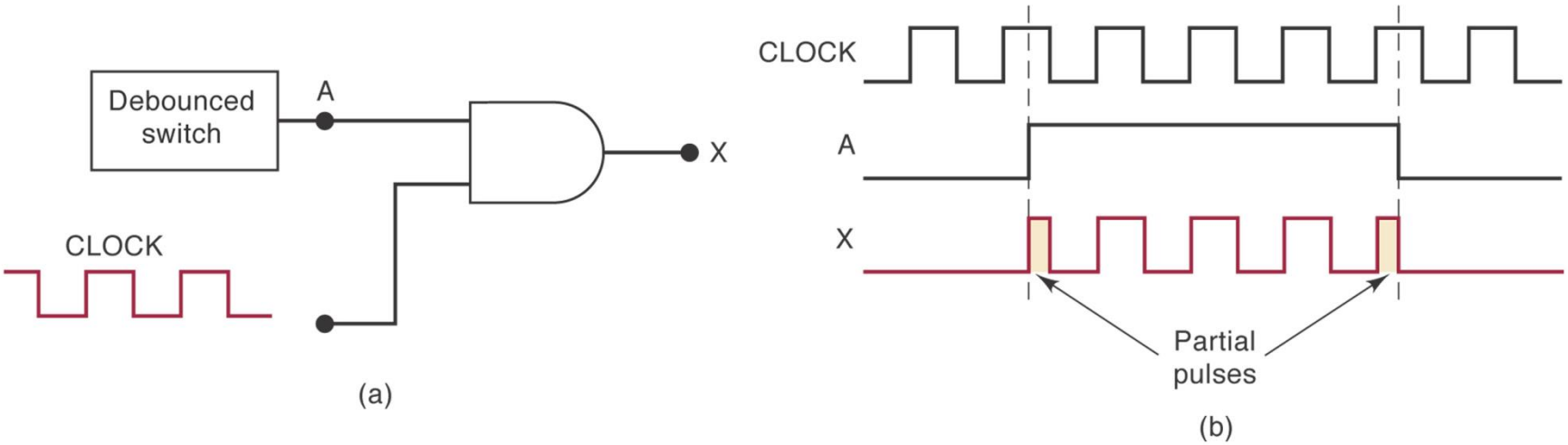
Assume Q_1=1, Q_2=0 initially

Q_2 will go HI, provided that the high->low delay t_{PHL} of FF_1 is greater than the **hold time** t_H of FF_2.

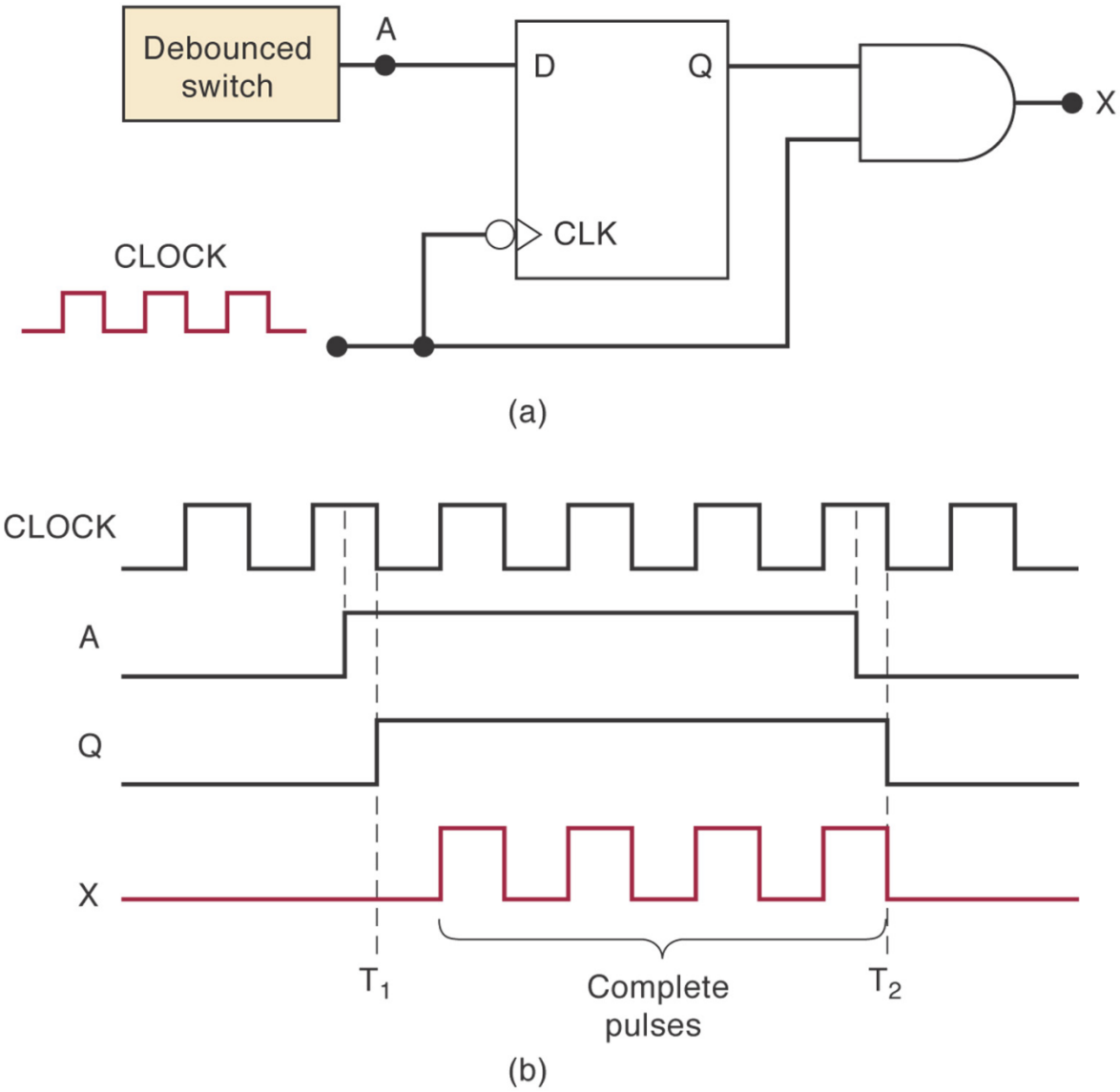
(1) Flip-Flop Synchronization

FF's can be used to synchronize an external signal with the system clock

Example: Partial pulses produced by the asynchronous signal

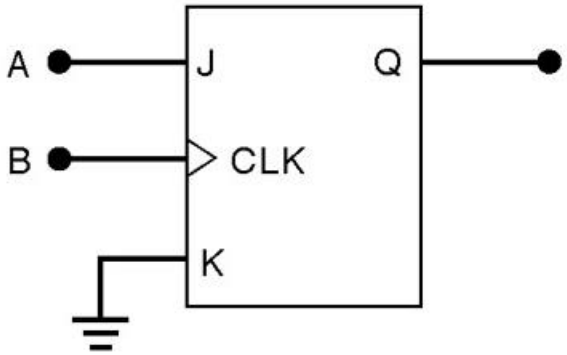


Solution with a D FF

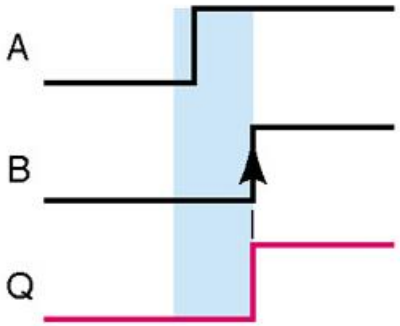


(2) Detecting an Input Sequence

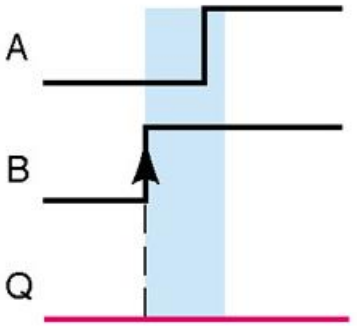
- FFs provide features that pure combinational logic gates do not.
- If an output is desired only when inputs change state in sequence, an arrangement similar to below can be used.
- Here, I/P A needs to go HI before B



(a)



(b) A goes HIGH before B

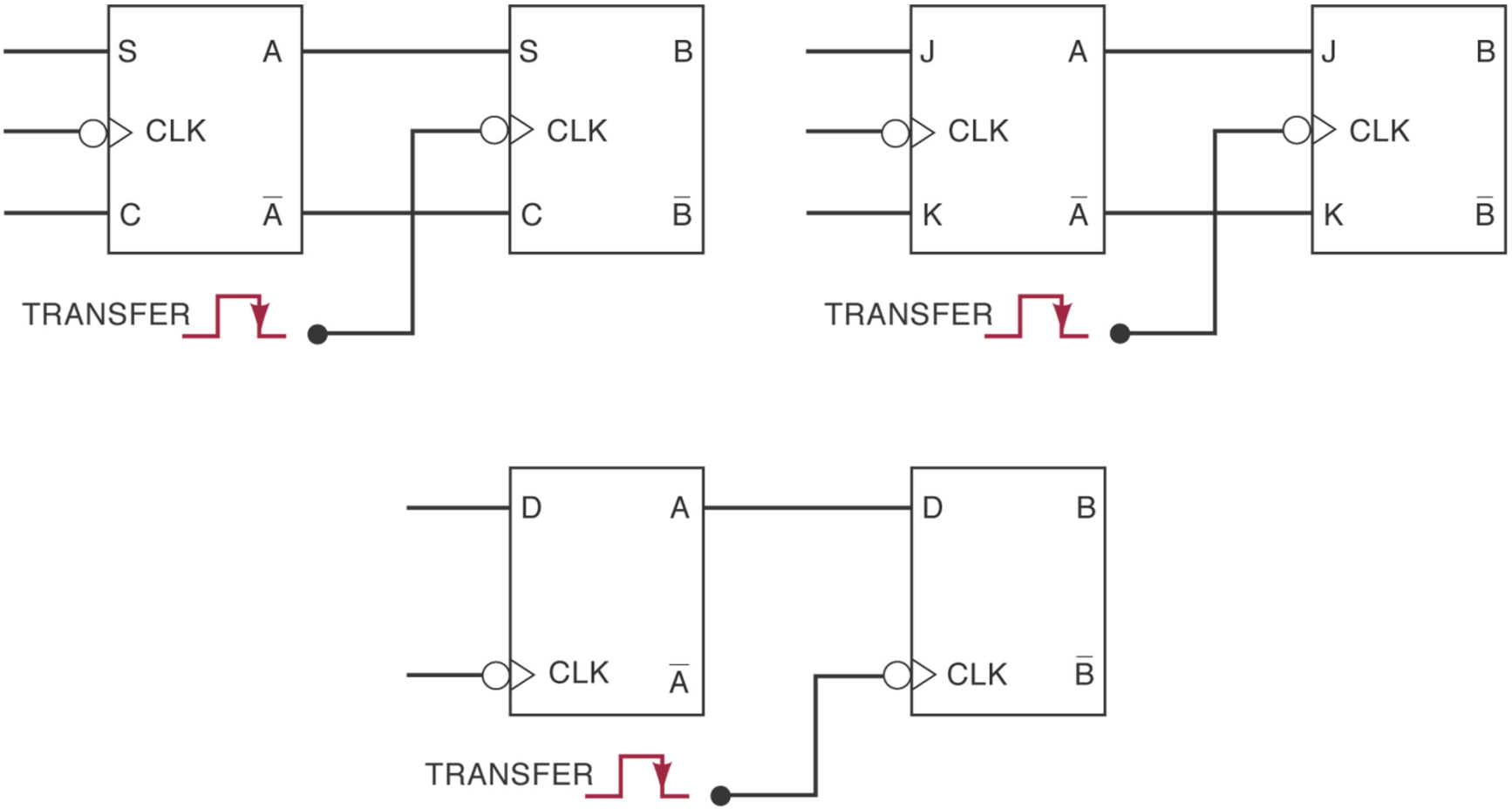


(c) B goes HIGH before A

(3) Data Storage and Transfer

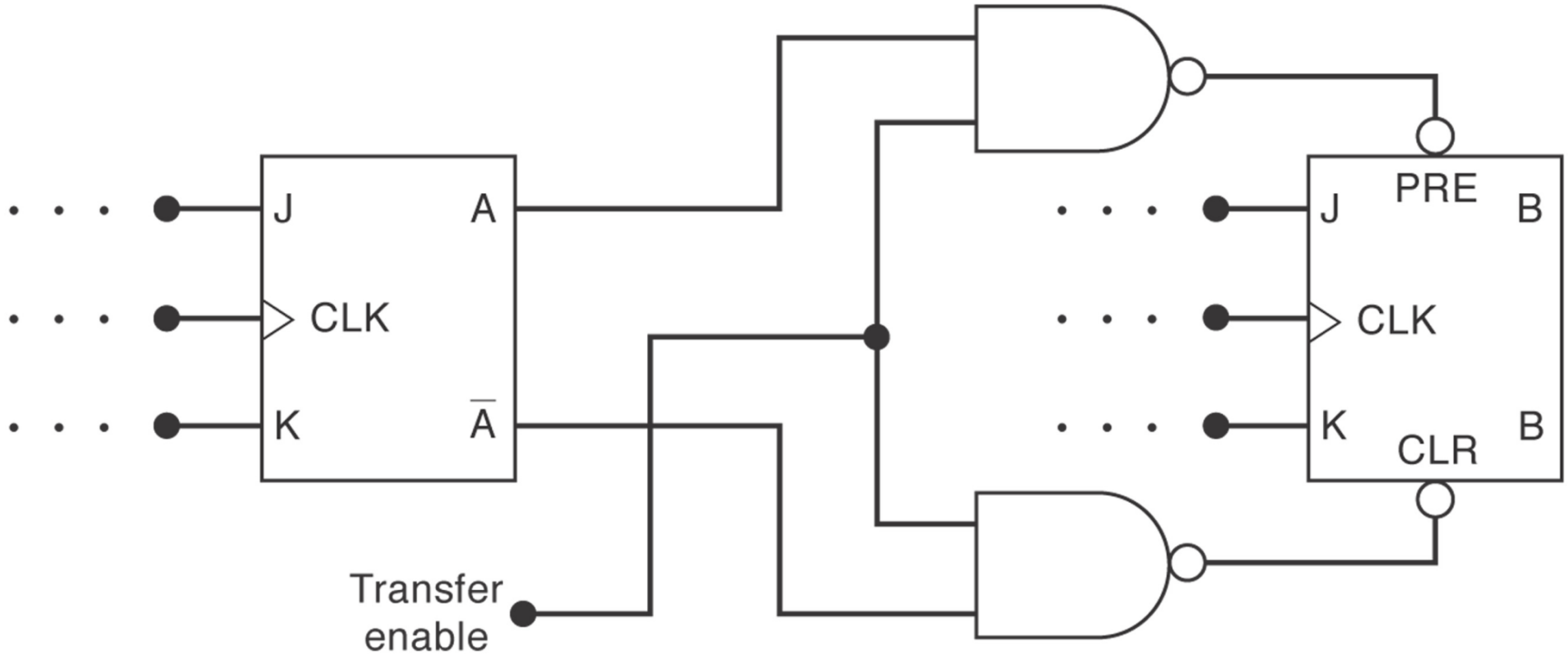
- FFs are commonly used for storage and transfer of binary data.
- Groups of FFs used for storage are called registers.
- Data transfers take place when data is moved between registers or FFs.
- Synchronous transfers take place at PGT or NGT of clock.

Synchronous data transfer by various types of clocked FF's.



Asynchronous data transfer operation.

- Controlled by PRE and CLR inputs.
- Also called a "jam" transfer.



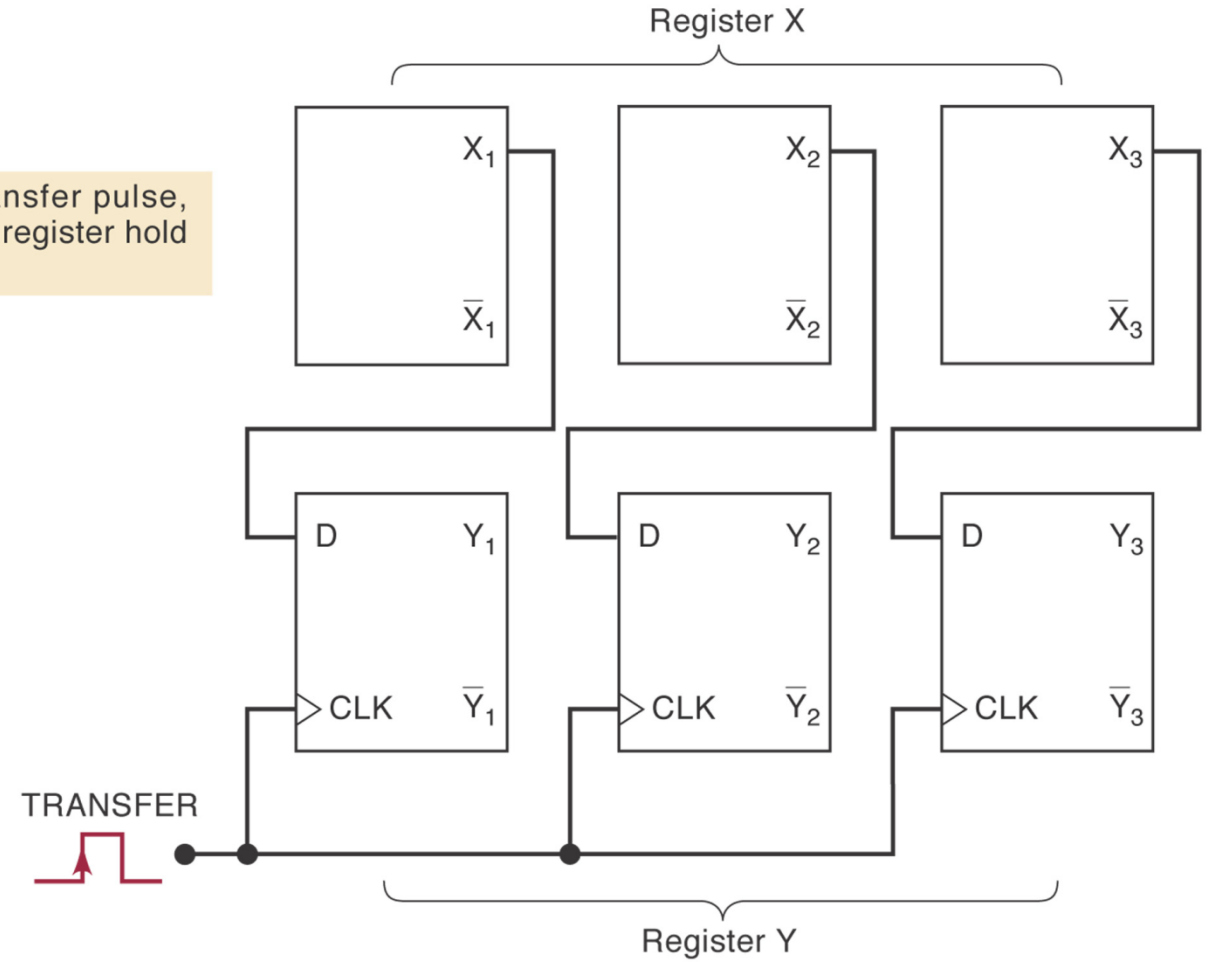
Data Transfer: Parallel or serial transfer

- Parallel transfers – register contents are transferred simultaneously with a single clock cycle.
- Serial transfers – register contents are transferred one bit at a time, with a clock pulse for each bit.
- Serial transfers are slower, but the circuitry is simpler. Parallel transfers are faster, but circuitry is more complex.
- Serial and parallel are often combined to exploit the benefits of each.

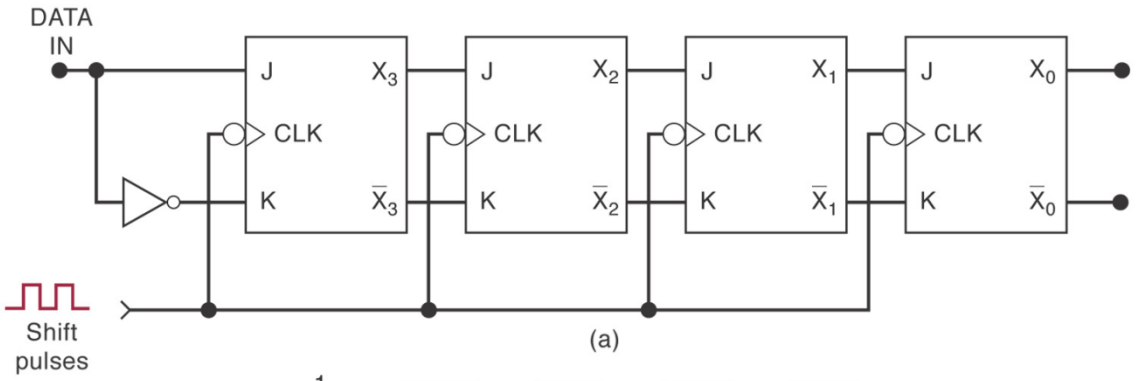
Parallel data transfer from register X to register Y.

Transferring the bits of a register simultaneously is a parallel transfer.

Note: After PGT of transfer pulse, Y register and X register hold same data.



Four serial bit shift register.

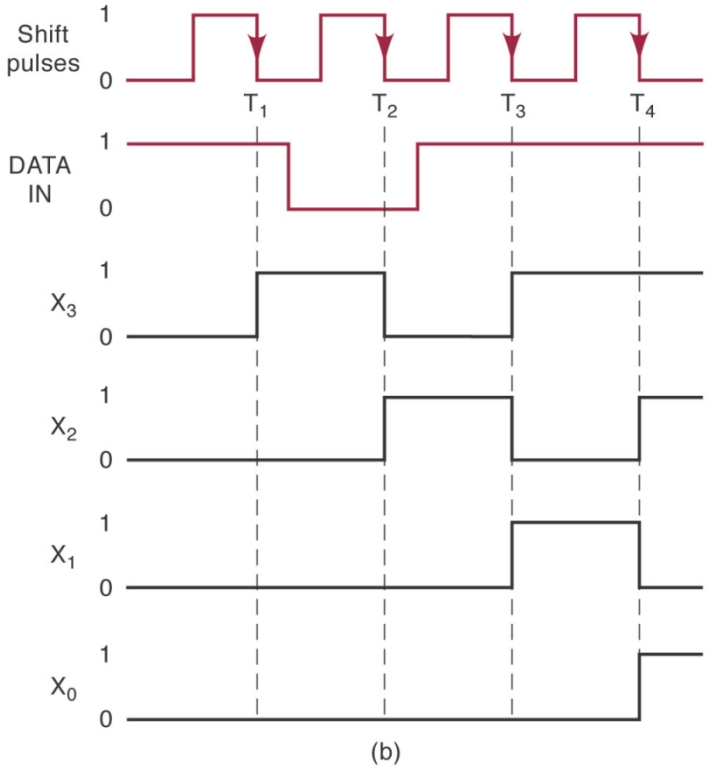


We want to move 1101

into the register.

(assume all X=0 initially)

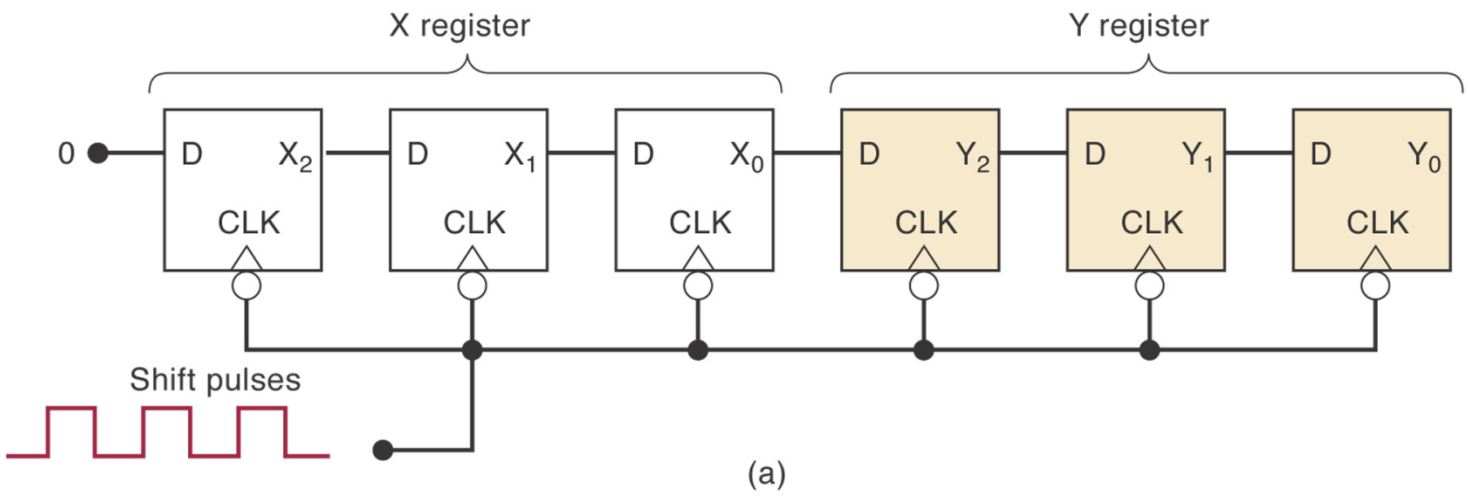
LSB



Requires small t_H

(recall t_H vs t_{PHL}, t_{PLH})

Serial transfer from register X to register Y.



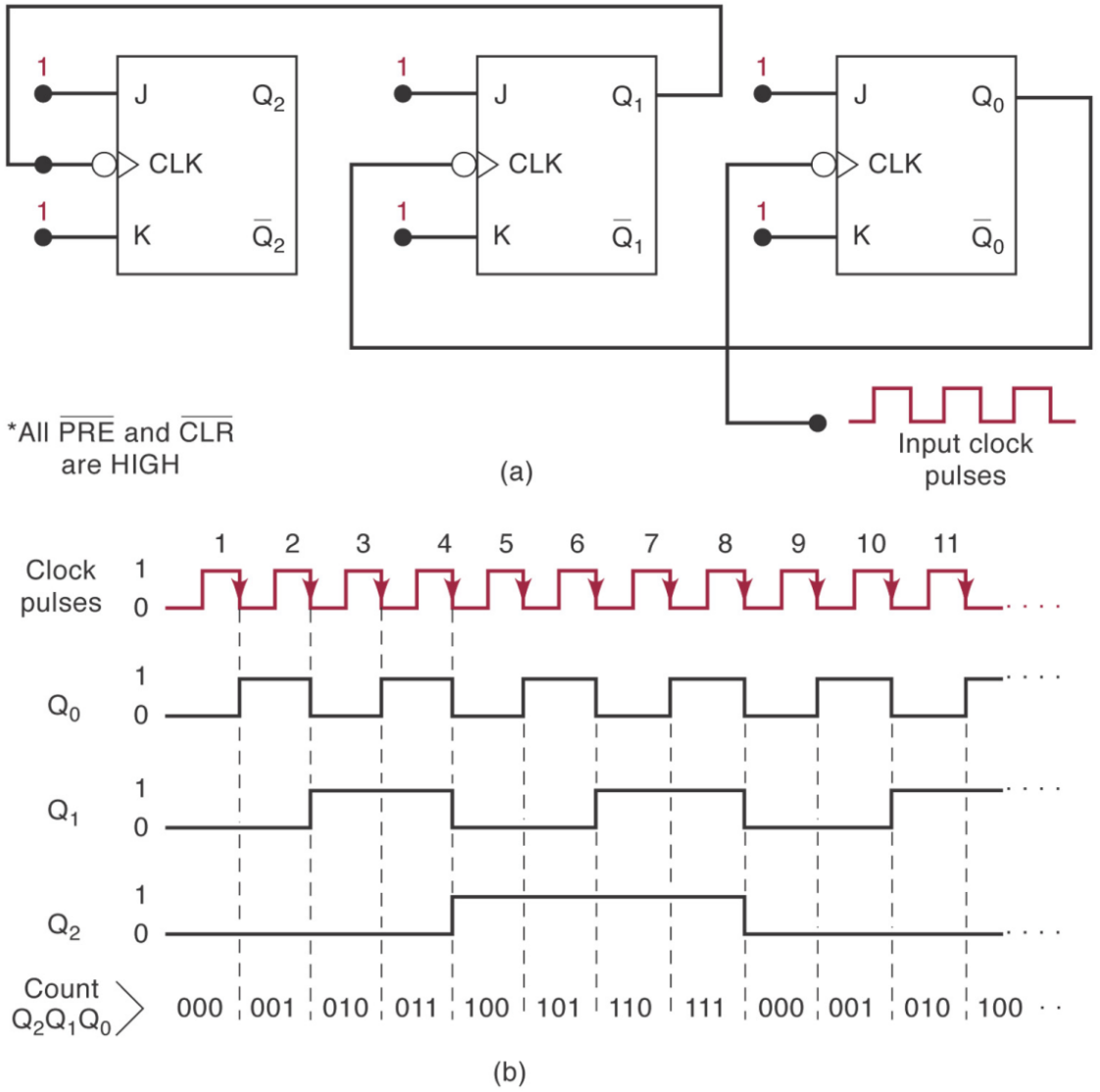
(a)

X_2	X_1	X_0	Y_2	Y_1	Y_0	
1	0	1	0	0	0	← Before pulses applied
0	1	0	1	0	0	← After first pulse
0	0	1	0	1	0	← After second pulse
0	0	0	1	0	1	← After third pulse

(b)

(4) Frequency Division and Counting

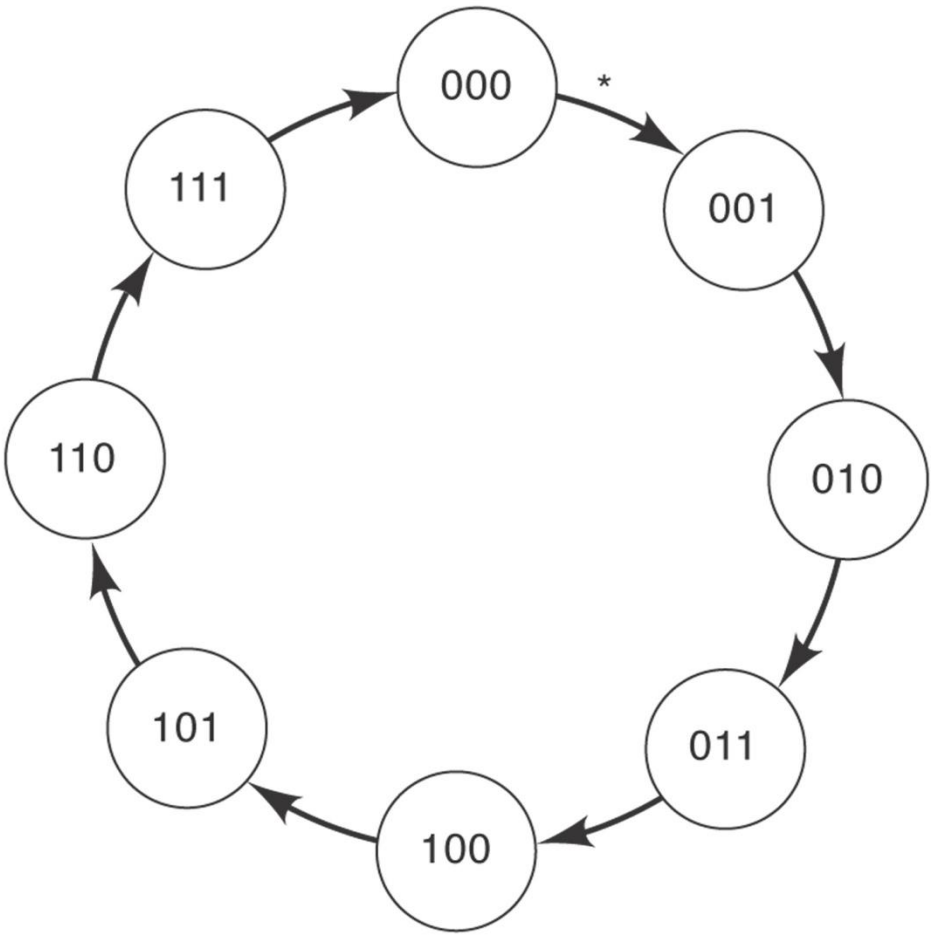
- FFs are often used to divide a frequency as illustrated.



Flip Flop states showing binary counting sequence MOD-8 Counter

2^2 Q_2	2^1 Q_1	2^0 Q_0	
0	0	0	Before applying clock pulses
0	0	1	After pulse #1
0	1	0	After pulse #2
0	1	1	After pulse #3
1	0	0	After pulse #4
1	0	1	After pulse #5
1	1	0	After pulse #6
1	1	1	After pulse #7
0	0	0	After pulse #8 recycles to 000
0	0	1	After pulse #9
0	1	0	After pulse #10
0	1	1	After pulse #11
.	.	.	. . .
.	.	.	. . .
.	.	.	. . .

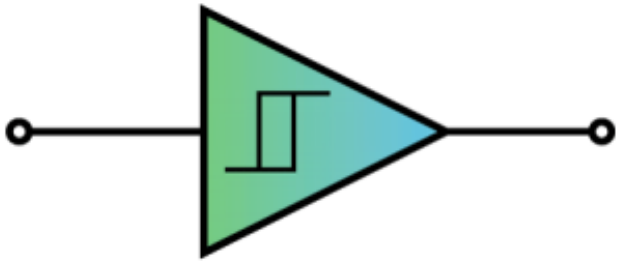
State transition diagram for the counter with each applied pulse.



* **Note:** each arrow represents the occurrence of a clock pulse

Related: Schmitt-Trigger Devices

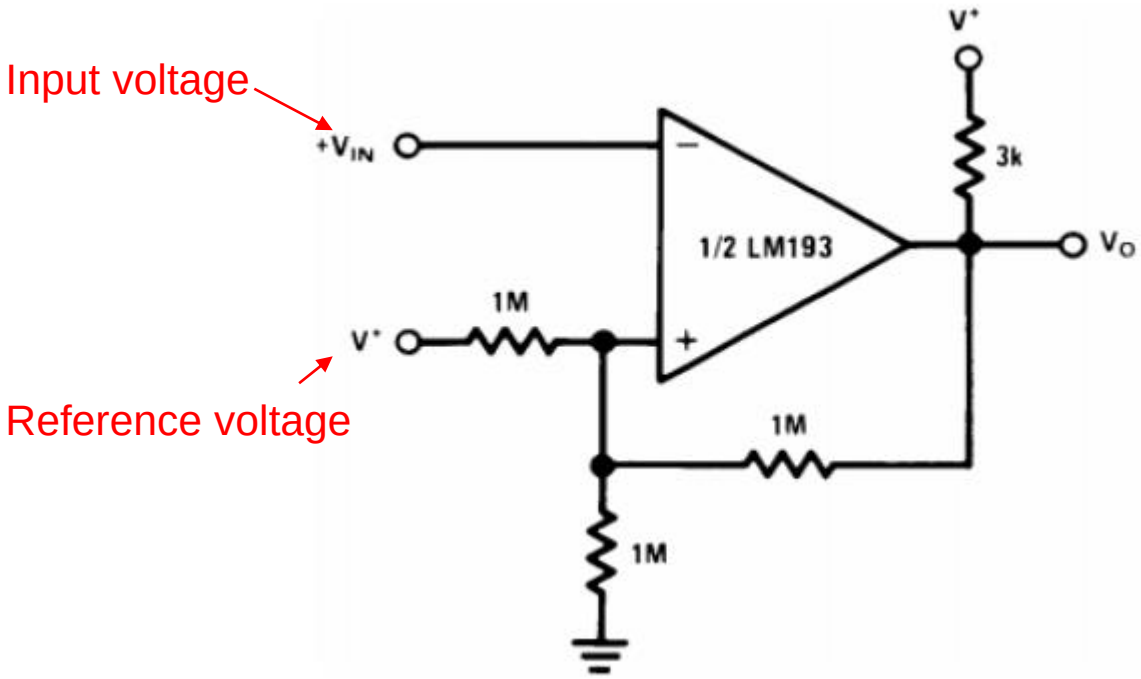
- A comparator circuit that makes use of positive feedback (ie small changes in the input lead to larger changes in the output in the same phase) to implement hysteresis (delayed action) and is used to remove noise from an analog signal while converting it to a digital one.



- Not a flip-flop but shows a memory characteristic

Related: Schmitt-Trigger Devices

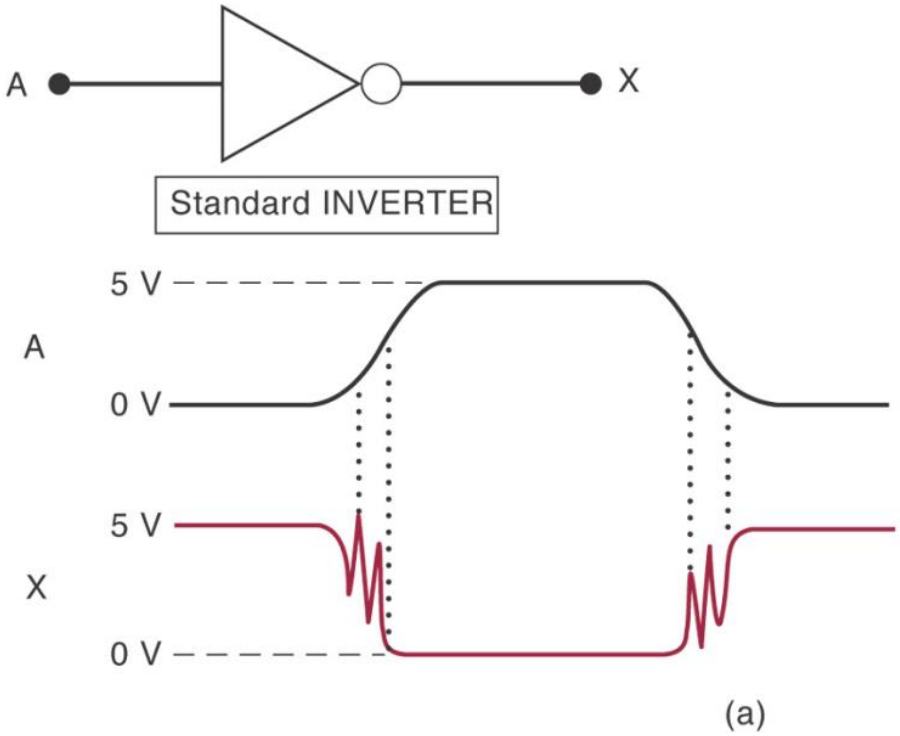
- Accepts slow changing signals and produces a signal that transitions quickly.



Related: Schmitt-Trigger Devices

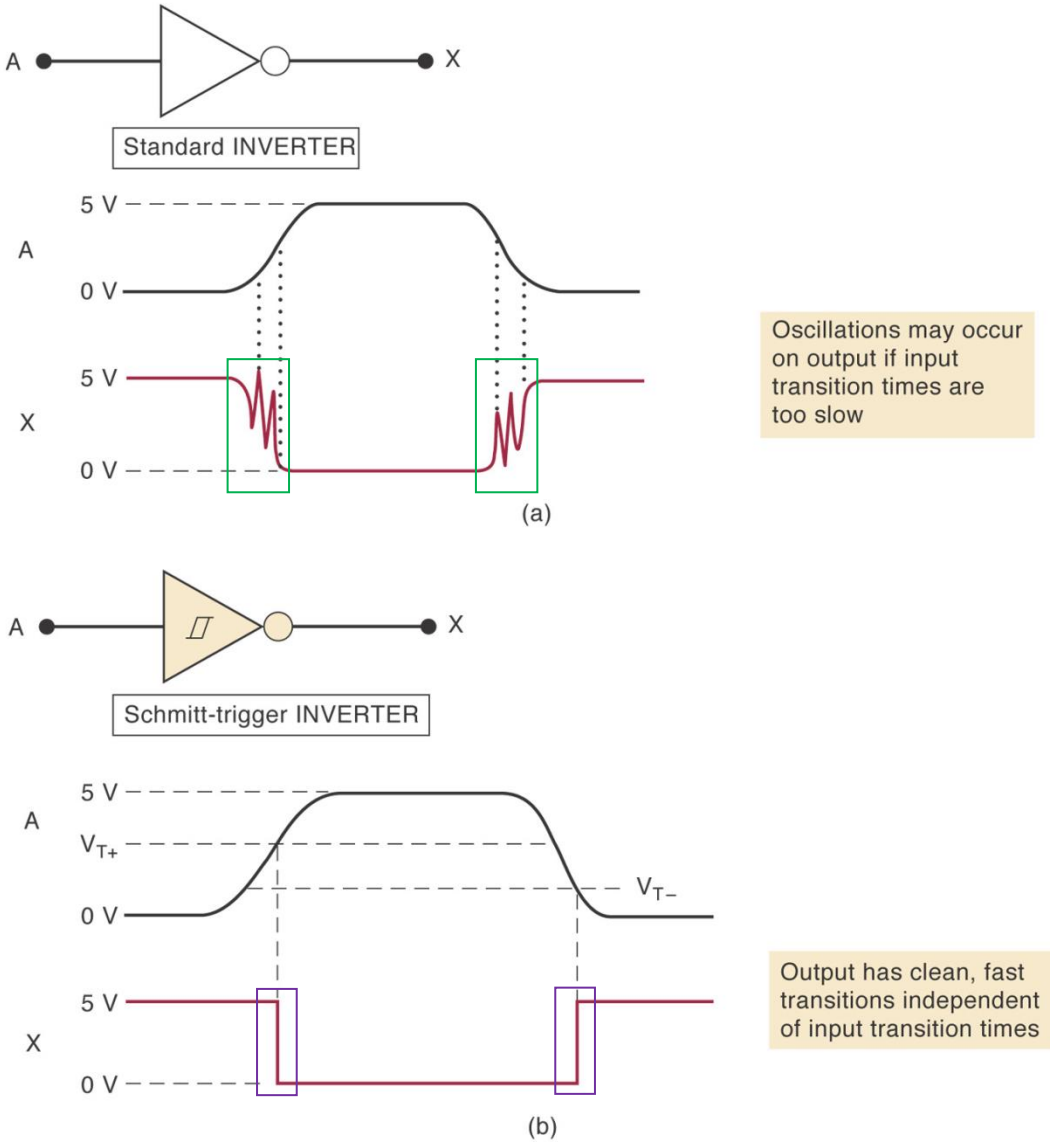
- A Schmitt trigger device will not respond to an input until it exceeds the positive or negative going threshold.
- There is a separation between the two threshold levels. This means that the device will “remember” the last threshold exceeded until the input goes to the opposite threshold.

Schmidt trigger inverter vs. standard inverter.



Oscillations may occur on output if input transition times are too slow

Schmidt trigger inverter vs. standard inverter.



Multivibrators

Latches and flip-flops are considered up to now can be described as **bistable multivibrators** – they have two equally stable O/P states. The device will be put in one of these states depending on the status of the input at the time of the clock pulse

However, we can define two more types of multivibrators:

1. Monostable multivibrator

2. Astable multivibrators

A monostable multivibrator (also called a one-shot) has only one stable state – the default or resting state.

The device will be in this stable state until triggered – then reverts to unstable state for a specific length of time.

The time in this quasi-stable state is determined by external components (usually resistors and capacitors).

Such monostable is normally used for simple timing applications, as capacitors and resistors often have poor stability.

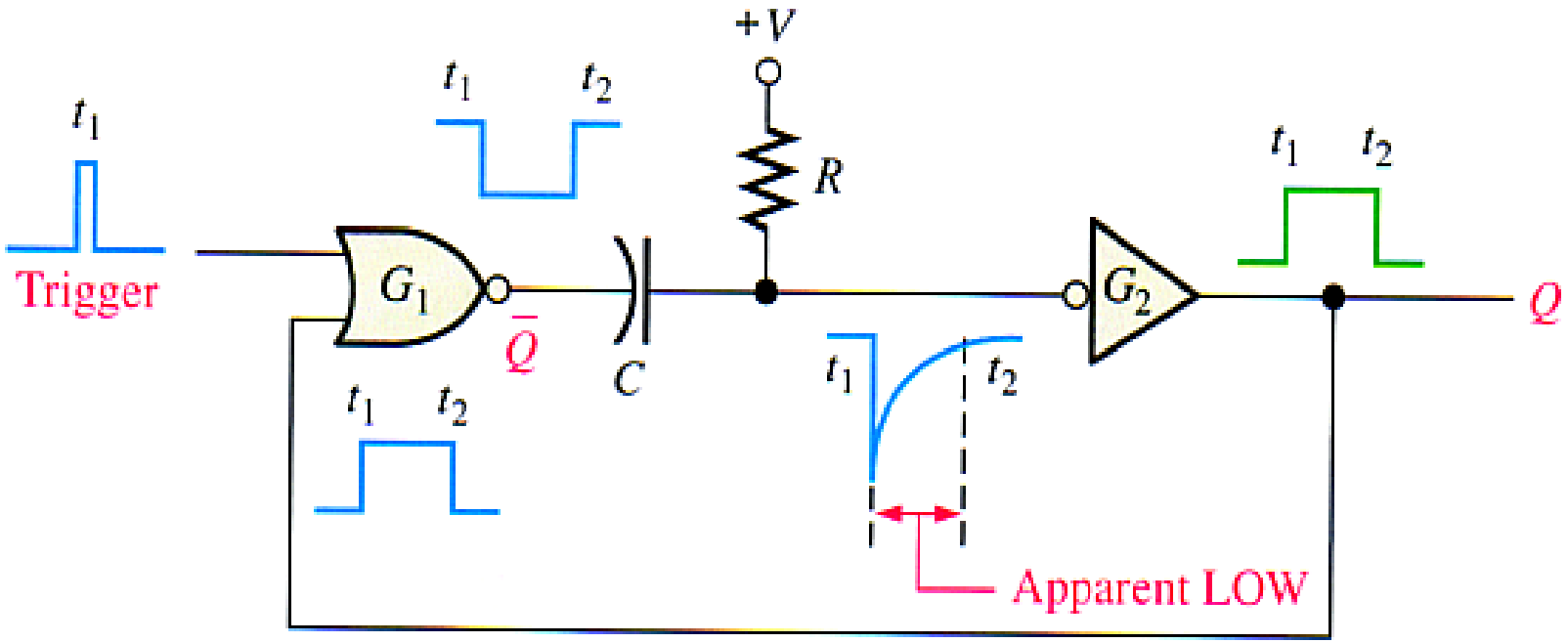
An astable multivibrator has two equally stable output states and will constantly flip between these states while the device is running.

This continuous HI-LO-HI-LO output thus makes it ideal for use as a clock signal. The frequency of output will again be determined by external resistors and capacitors that can be connected to the device.

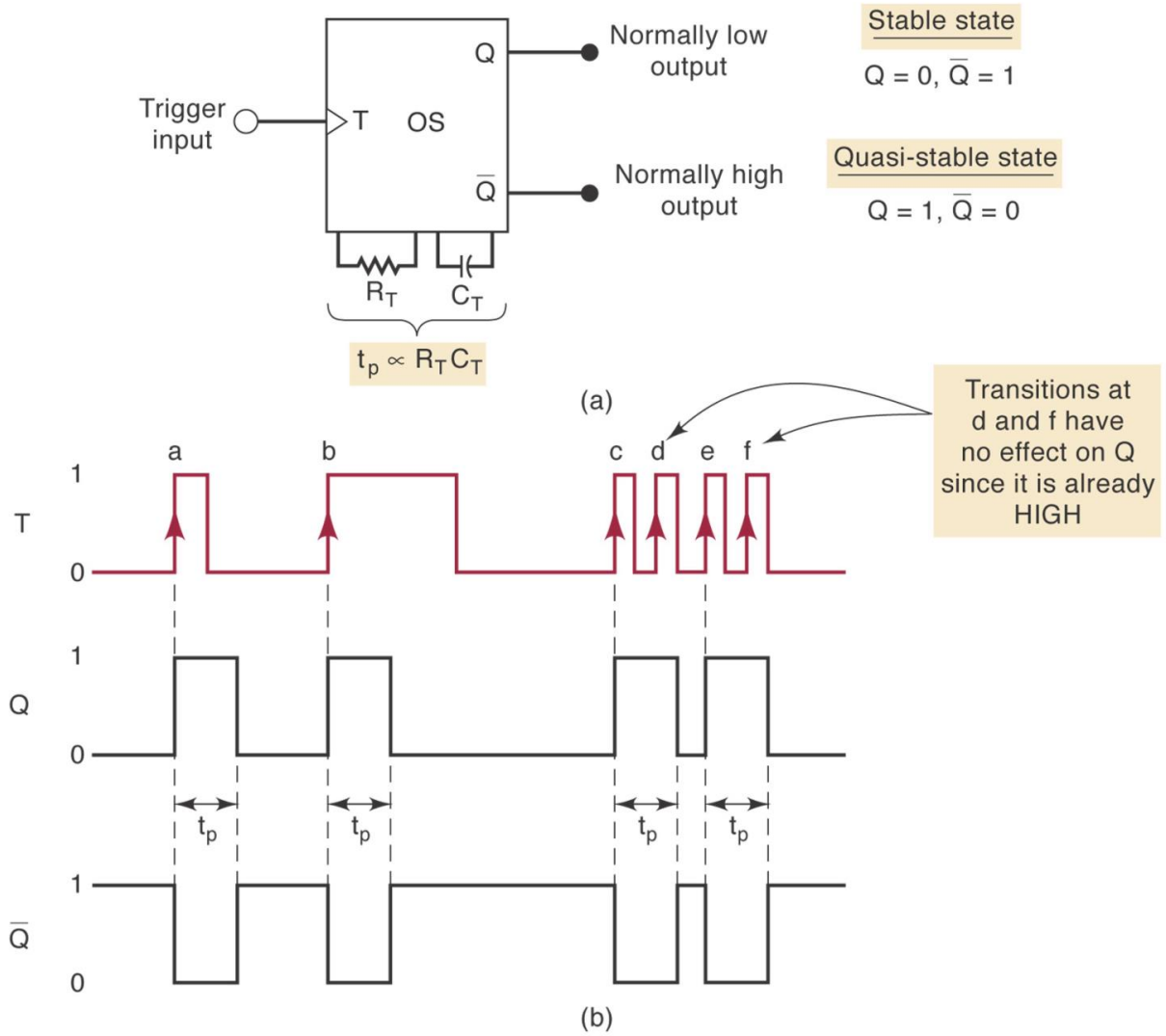
However, the precision and stability of these external components are again generally poor, so that such a clock will not be used in high precision applications.

Setting the time constant in monostables and astables.

We will normally use external components (resistors and capacitors) to set the timing of astable and monostables. The figure below shows how the RC time constant will determine the time in the unstable state (HI) for a monostable.

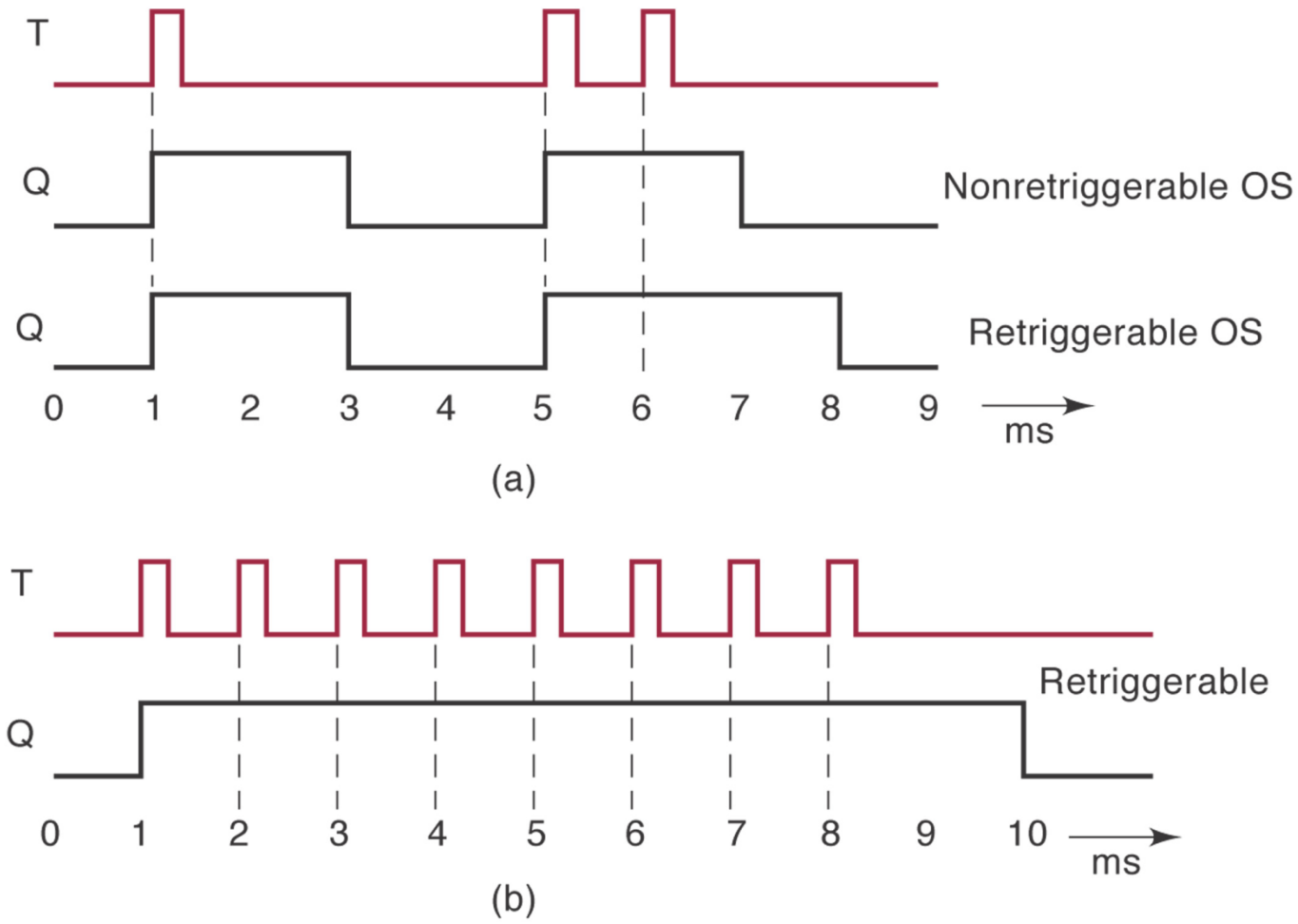


Operation of a One-Shot



Will be in the stable state until triggered – then in the unstable state for a time determined by the external components

Comparison of a non-retriggerable and retriggerable OS

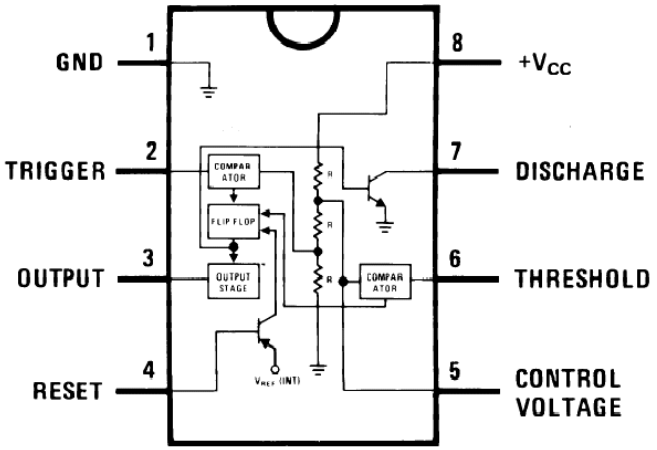


The 555 Timer

The 555 timer is a very useful IC as it can be configured as either a monostable or astable multivibrator.

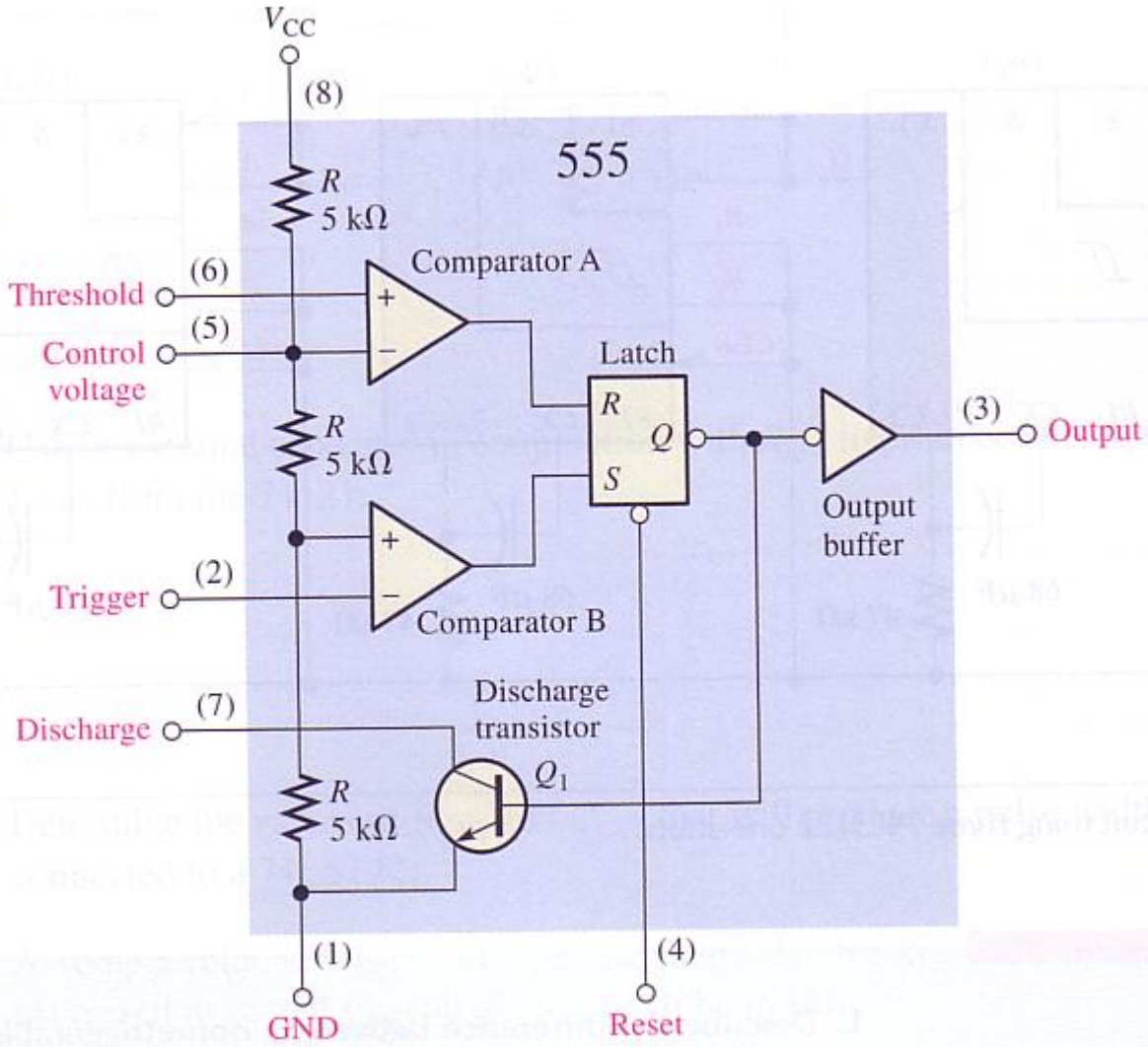
•Basic design ~1971. Now available in CMOS and in 2-in-1 version (556)

• Use 2 internal comparators: O/P is HI when the voltage on the non-inverting (+) input is higher than the voltage on the inverting (-) input.



LM555 Timer

Internal construction of a 555 Timer



Comparators: O/P is HI when the voltage on the non-inverting (+) input is higher than the voltage on the inverting (-) input.

Voltage divider consisting of **three** 5kΩ resistors – providing

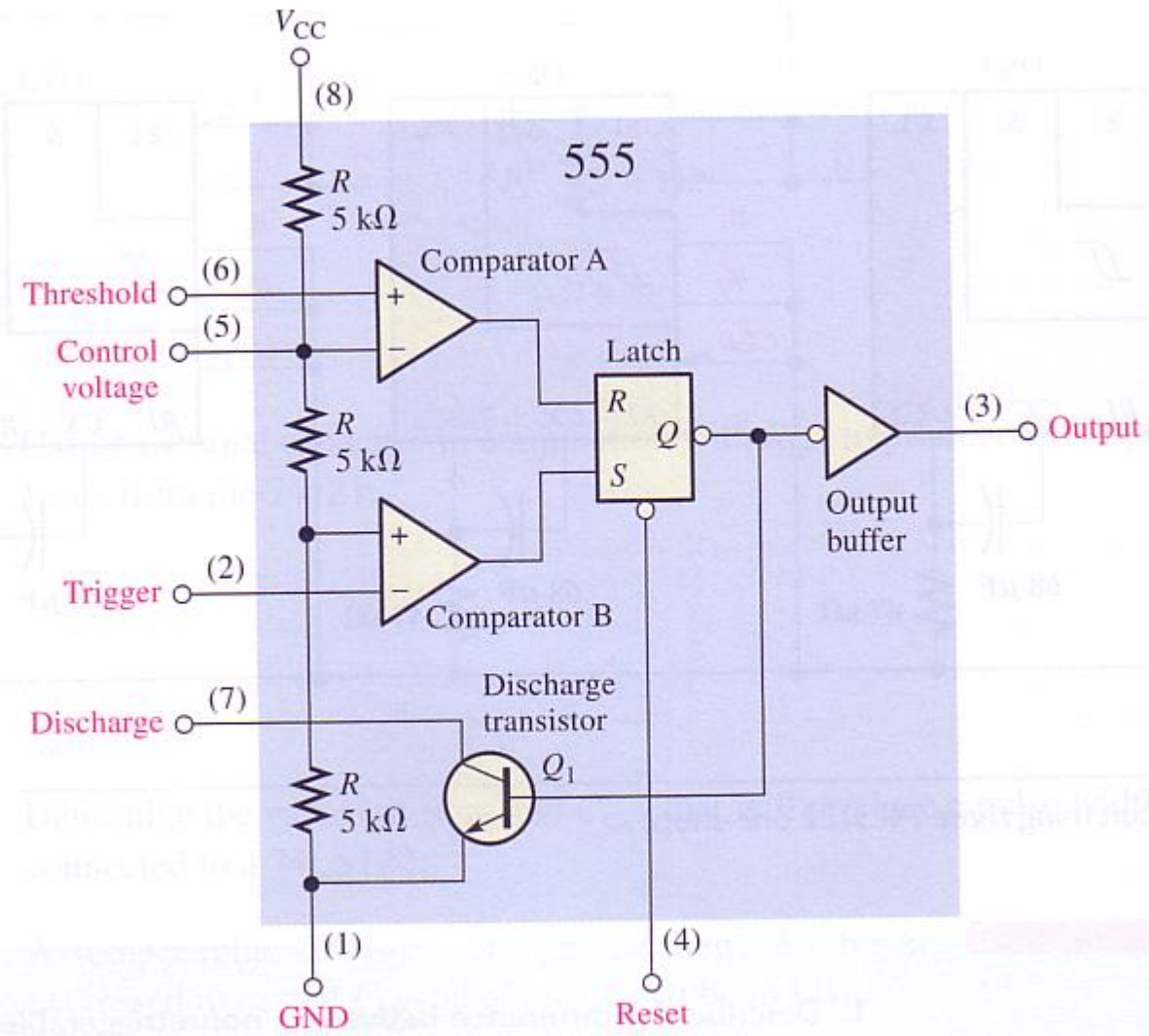
a trigger level = 1/3 V_{cc} and a threshold level = 2/3 V_{cc}

Trigger level normally HI – when drops below 1/3Vcc the comparator B O/P goes HI – sets the S-R latch

Will cause O/P (pin 3) to go HI

Also turn OFF the transistor Q_1 base current

Internal construction of a 555 Timer



O/P will stay HI until the normally LO threshold voltage goes > 2/3Vcc – Causes comparator A to switch and reset the latch

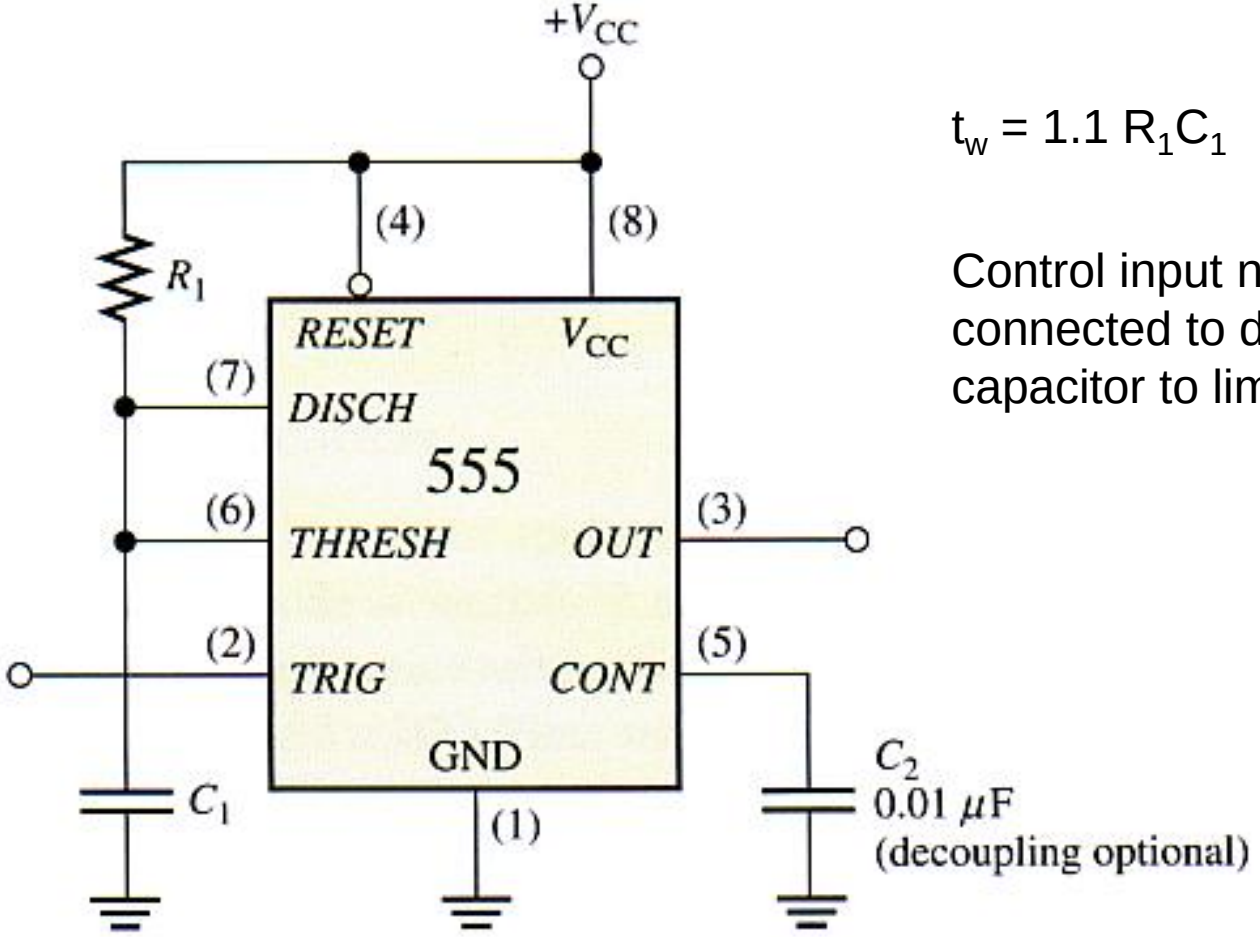
This turns O/P to LO again and switches on the discharge transistor.

External reset input can be used to reset the latch independent of internal operation.

Trigger (2) and threshold (6) pins are controlled by external components that can be connected for either monostable or astable operation.

555 Timer connected as a one-shot (monostable)

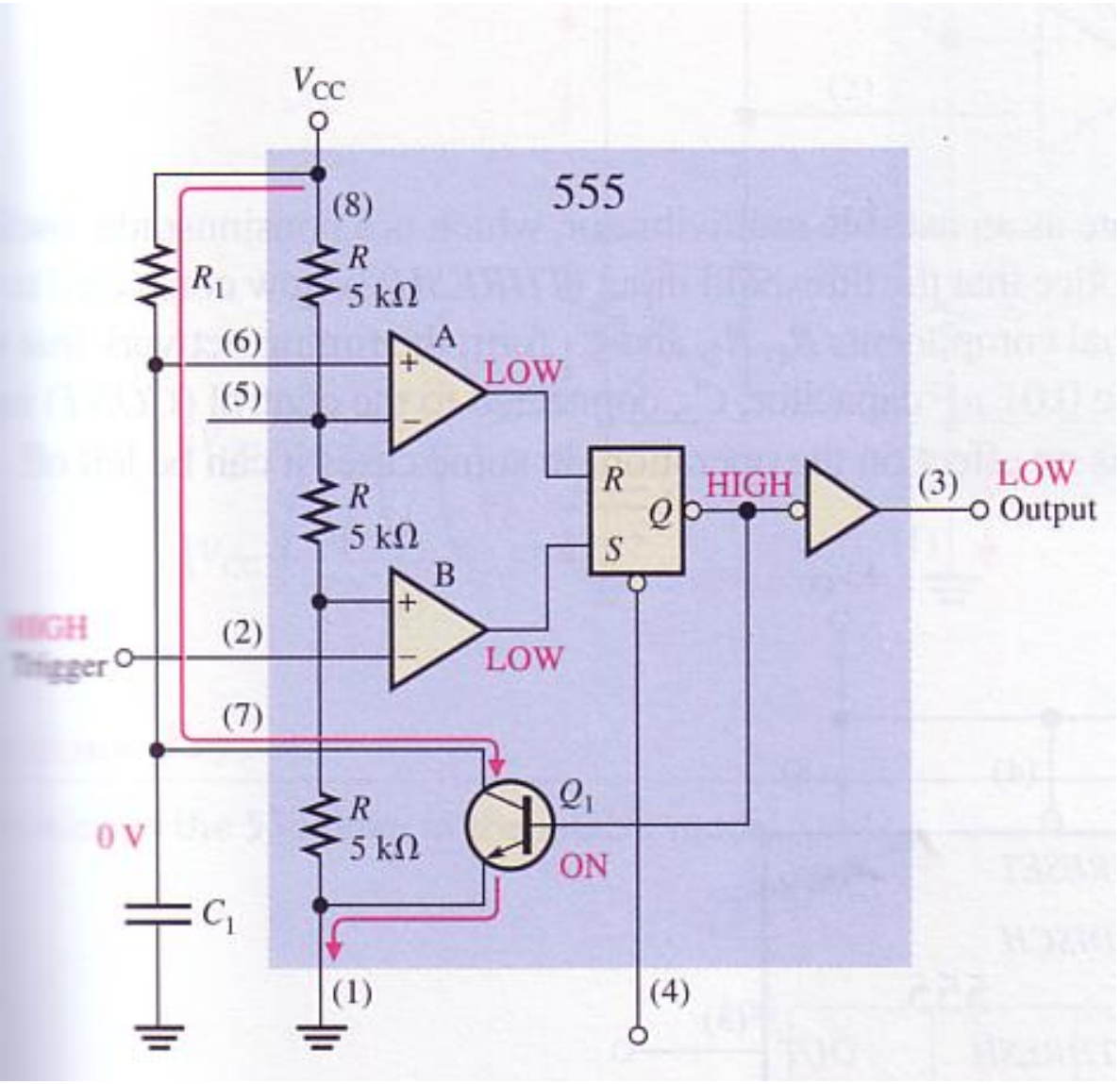
External R_1 and C_1 connected as shown below.



$t_w = 1.1\ R_1C_1$

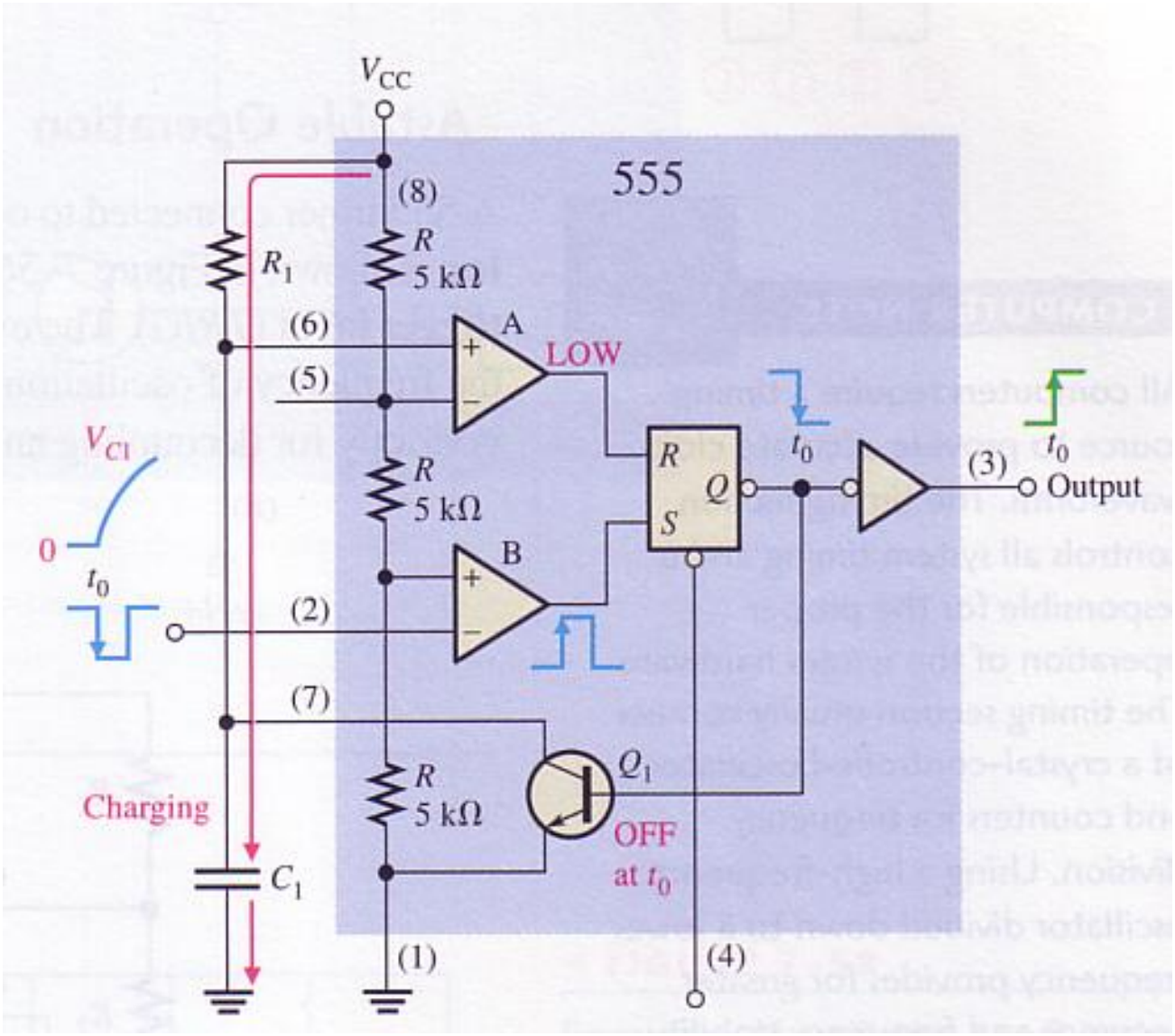
Control input not used – connected to decoupling capacitor to limit noise.

Prior to triggering



O/P is LO and Q1 is ON – keeps C1 discharged.

When triggered

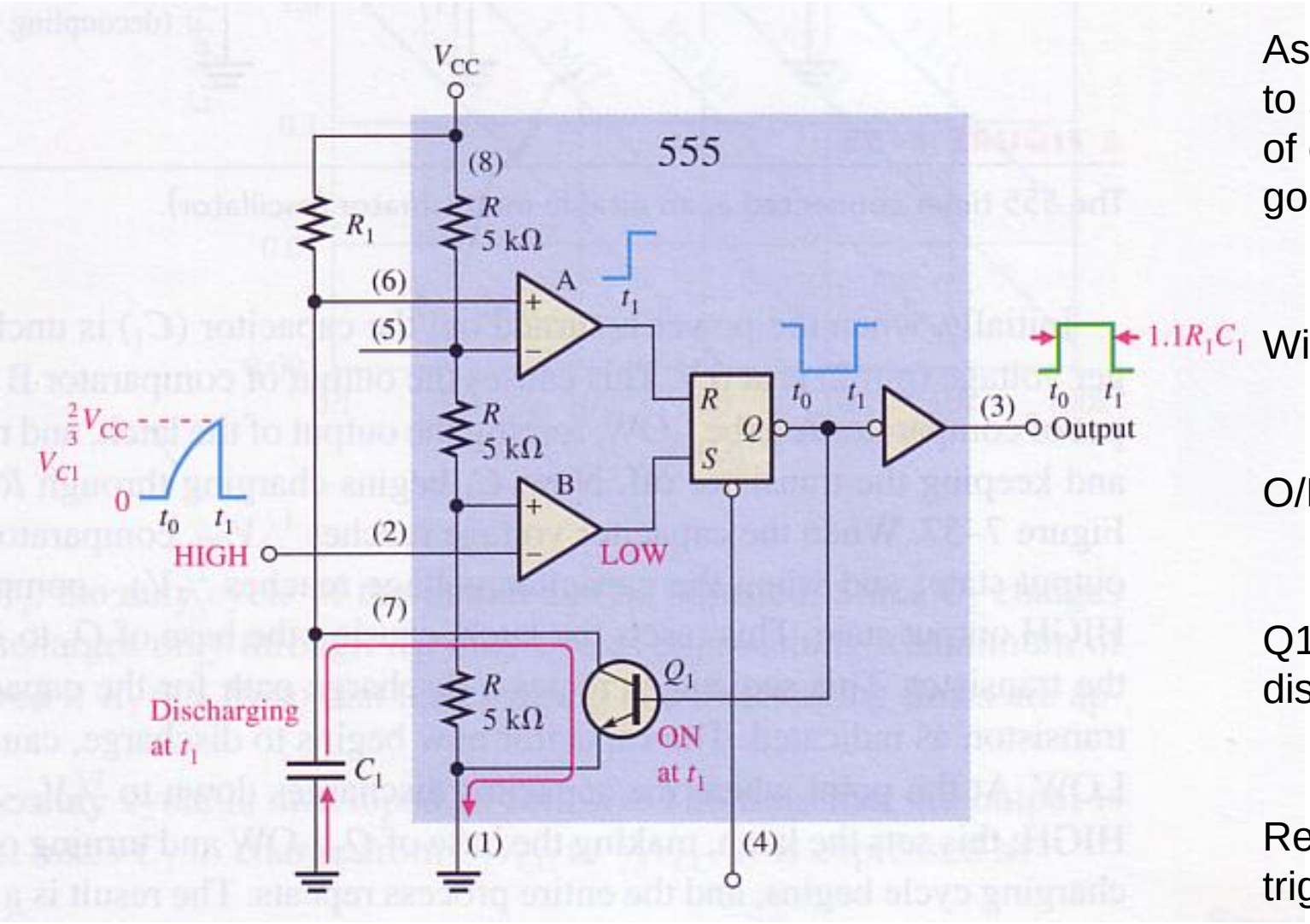


NG trigger pulse is applied – Comparator B switches to HI and the O/P switches to HI

Q1 turns off

Capacitor C1 starts to charge through R1

At end of charging interval



As C1 charges up to 2/3 Vcc, the O/P of comparator A will go HI at t1

Will reset the latch

O/P goes LO at t1

Q1 will turn ON and discharge C1

Ready for next trigger

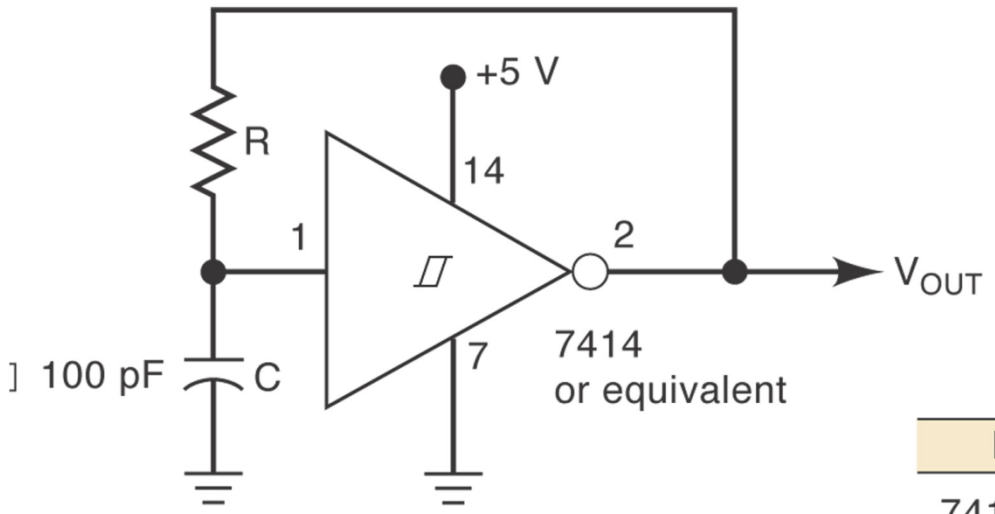
Astable Multivibrators = Clocks

Astable or **free-running multivibrators** switch back and forth between two unstable states. This makes it useful for generating clock signals for synchronous circuits.

Different applications place varying demand on clock circuits in terms of precision and long term stability

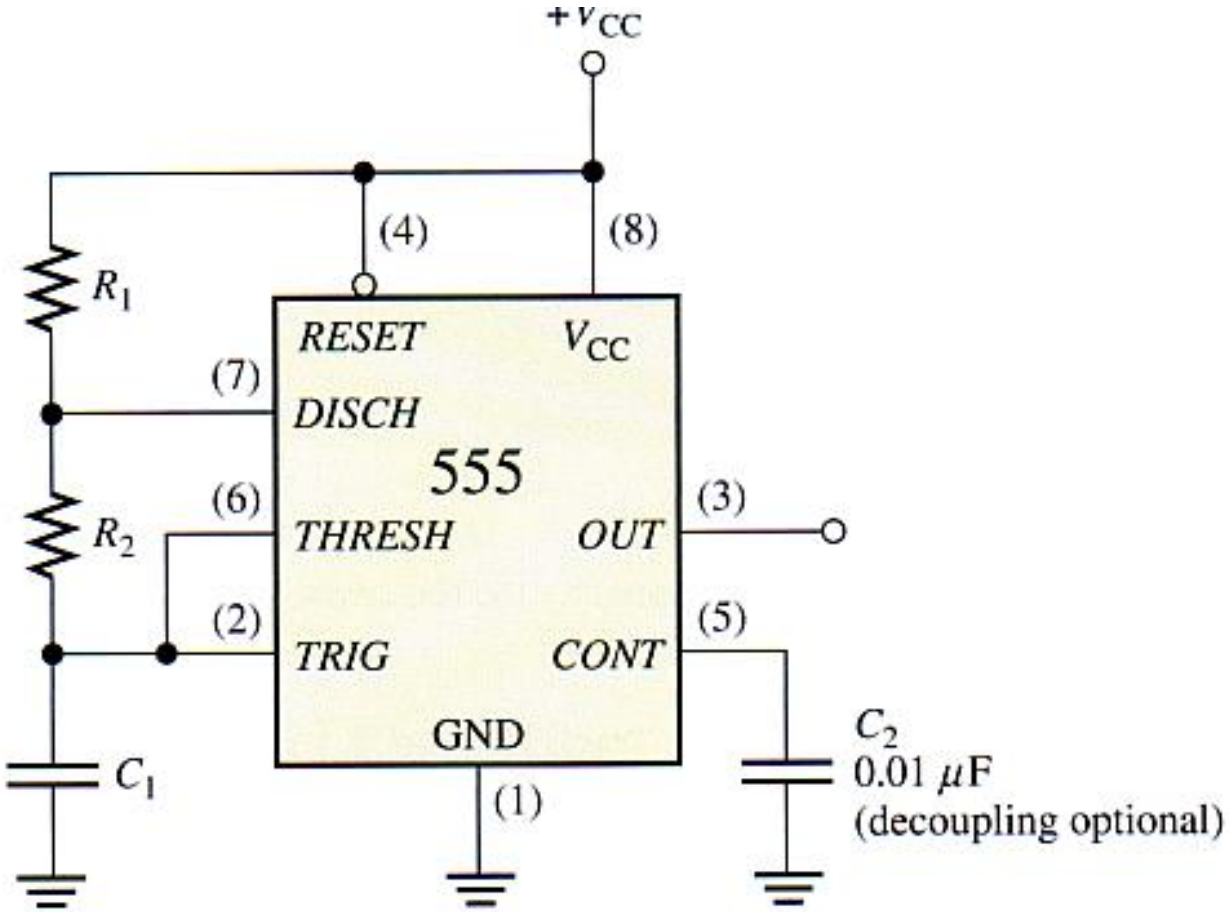
- Low end – Digital IC based clocks
- Medium – Crystal oscillator circuits
- Temperature controlled crystal oscillators, atomic clocks

Schmidt trigger oscillator as an example of an astable

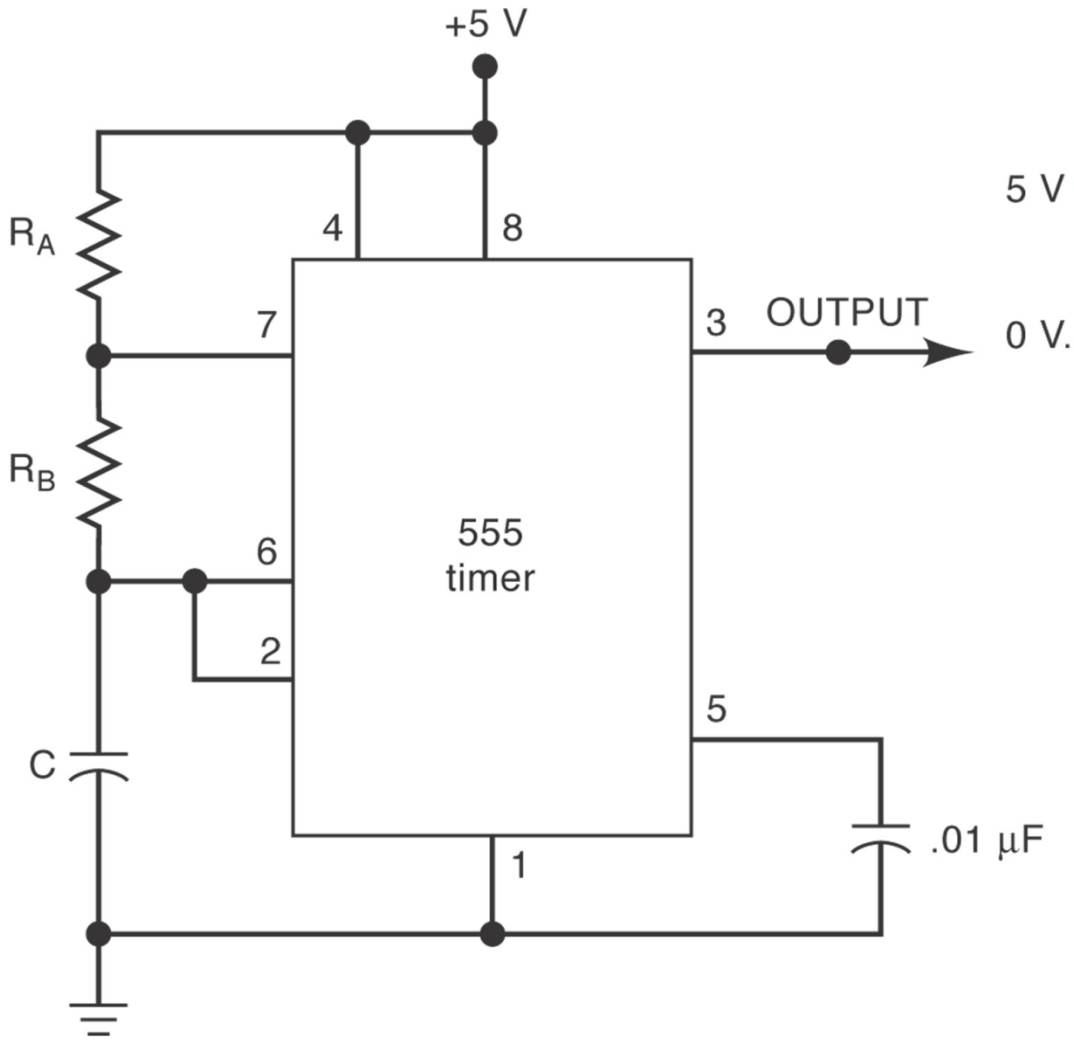


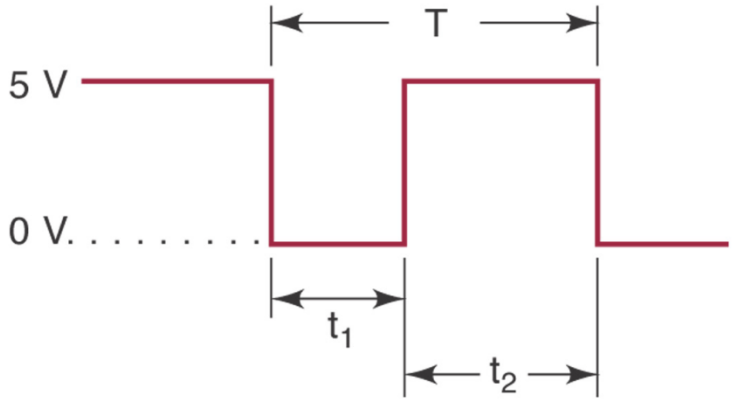
IC	Frequency	
7414	≈ 0.8/RC	(R * 500 V)
74LS14	≈ 0.8/RC	(R * 2 kV)
74HC14	≈ 1.2/RC	(R * 10 MV)

The 555 connected as an astable (free running) multivibrator

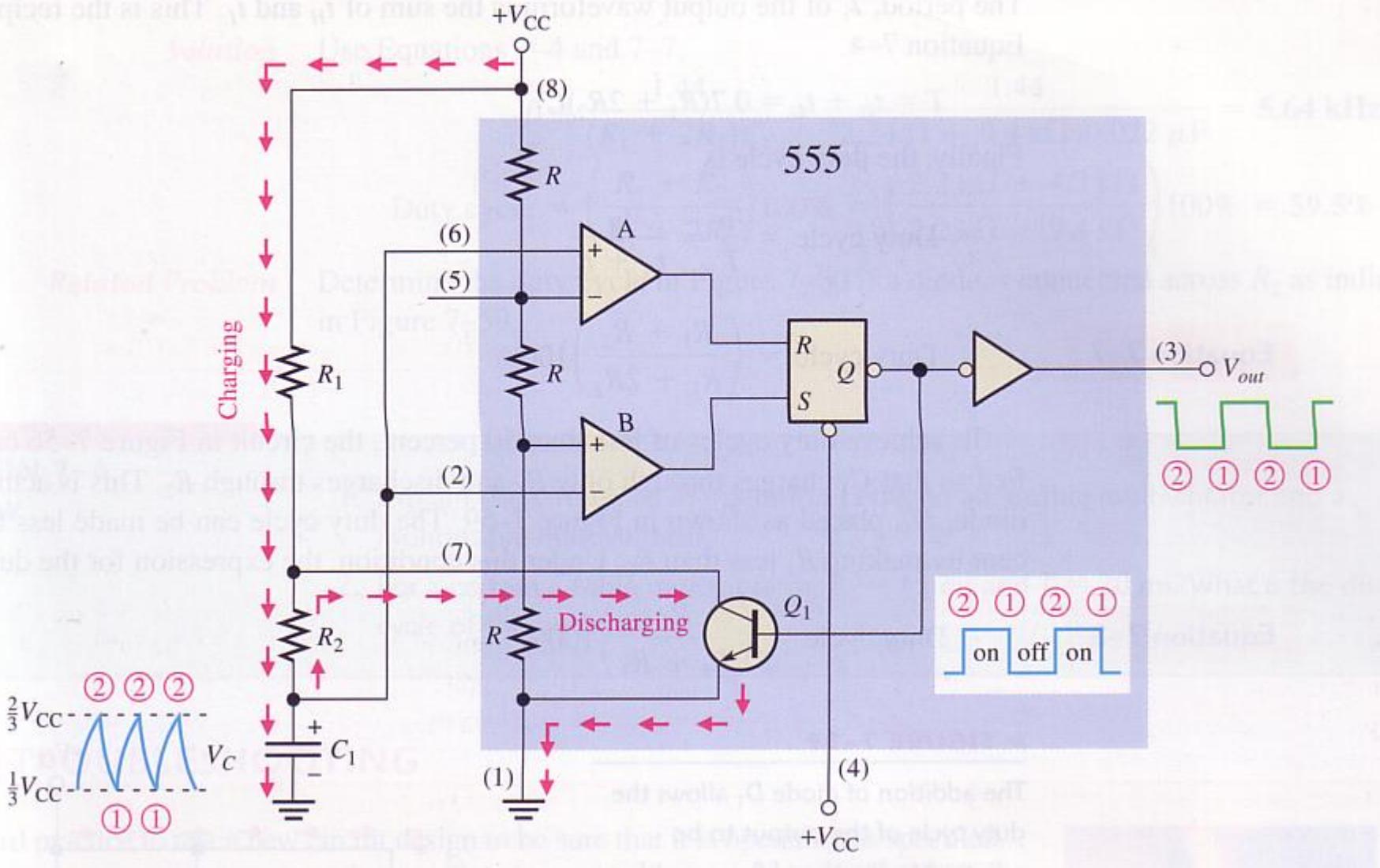


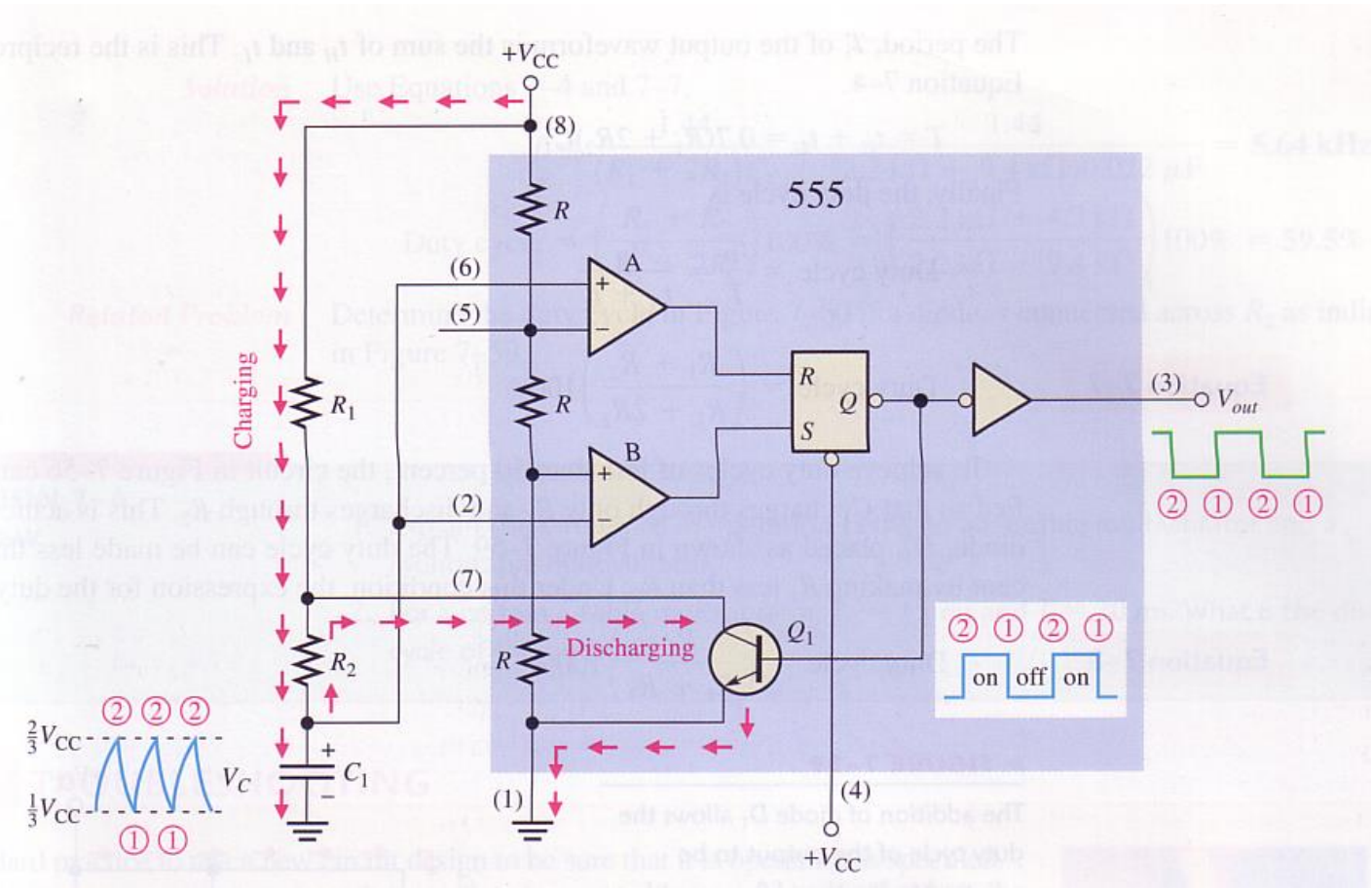
The 555 Timer as an Astable Multivibrator.





$t_1 = 0.693\ R_B C$
$t_2 = 0.693\ (R_A + R_B)C$
$T = t_1 + t_2$
frequency = 1/T
duty cycle = $t_2/T \times 100\%$
R_A] 1 kV
$R_A + R_B$ * 6.6 MV
C] 500 pF


+VCC
(8)
555
R
(6)
A
(5)
R
R1
Charging
R
Q
S
(3)
Vout
B
(2)
(7)
Q1
R2
R
Discharging
on
off
on
(1)
(4)
+VCC
C1
VC
2/3VCC
1/3VCC



Astable operation

Threshold (6) now connected to the trigger (2) input

Two external resistors and a capacitor

2nd Capacitor (on Control) for decoupling only – can be left off

Initially capacitor is uncharged – trigger pin (2) is at 0V

This causes O/P of Comp B = HI and Comp A = LO This will keep Q1 OFF

Capacitor will now start to charge through R1 and R2

When it reaches 1/3 Vcc Comp B will switch to LO, when it reached 2/3 Vcc Comp A will switch to HI – Will now reset the latch.

This switches on Q1 and discharges capacitor through R2.

When capacitor discharges to 1/3Vcc Comp B goes HI and sets the latch again.

This turns off Q1 – Another charge cycle of the capacitor starts

Astable operation

Threshold (6) now connected to the trigger (2) input

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High precision Crystal controlled oscillator clocks