ID Number: ……...…………….

Full Name: …………… …………..………..….

ECEN202

DIGITAL ELECTRONICS

Practice TEST

2024

Time allowed: 60 MINUTES

CLOSED BOOK

Permitted materials: No programmable calculators are allowed.

No electronic dictionaries are allowed.

Paper foreign to English language dictionaries are allowed.

Instructions: Attempt ALL questions.

There are 4 questions in this test paper:

Space for working out your solutions is provided at the end of every section.

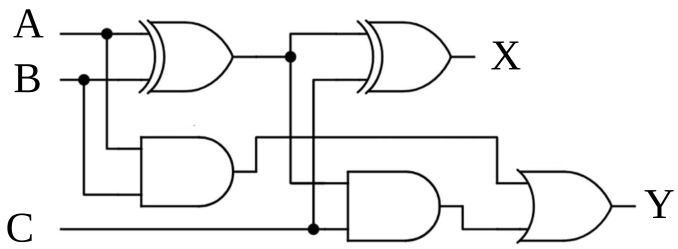
Question	Topic	Allocated Marks	Obtained Marks	
1	Logic and Boolean Algebra	25		
2	Combinational Logic	35		
3	Latches and Flip Flops	15		
4	Counters and Frequency Dividers	25		
	TOTAL	**100**		

ID Number: ……..……………………

[**CLEARLY** write your ID number in the space shown above]

Question 1 – Logic and Boolean Algebra **25 marks**

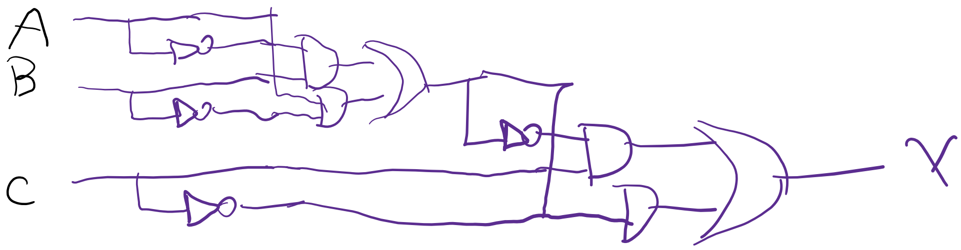
a) Write the Boolean expression for the outputs X and Y of the following circuit. (10 marks)



X = A xor B xor C = (A'B+AB') C'+(A'B+AB')' C

Y = AB+C (A xor B)

b) Draw a circuit diagram for **X** in part a) using only AND, OR and NOT gates. (8 marks)



c) Simplify using Boolean Algebra (3 marks)

$$X = (\overline{AB})(\bar{A} + B)(\bar{B} + B)$$

$$= (\bar{A} + \bar{B})(\bar{A} + B)$$

$$= \bar{A} + \bar{A}B + \bar{A}\bar{B} + B\bar{B}$$

$$= \bar{A} + \bar{A}\bar{B} = \bar{A}$$

a) Simplify using Boolean Algebra (4 marks)

$$X = ABC + A\bar{B}(\overline{\bar{A}\bar{C}})$$

$$= ABC + A\bar{B}(A + C)$$

$$= ABC + A\bar{B} + A\bar{B}C$$

$$= AC + A\bar{B}$$

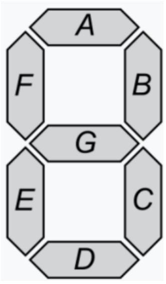
$$= A(C + \bar{B})$$

ID Number: ……..……………………

[**CLEARLY** write your ID number in the space shown above]

Question 2 – Combinational Logic **35 marks**

We want to design a logic circuit for a 7-segment LED display shown below.



The inputs are 4 binary digits **d**, **c**, **b**, **a**, which represent the number to be displayed on the LED. Bit **d** is the most significant bit (MSB), and **a** is the least significant bit (LSB). Each LED segment (labelled A, B, C, … G on the diagram) has its own logic. For example, LED D is ON when **dcba** represent decimal numbers 0, 2, 3, 5, 6, 8 or 9.

a) Produce a truth table to drive LED labelled **E** **0 2 6 8** (10 marks)

d	**c**	**b**	**a**	**E**
0	0	0	0	**1**
0	0	0	1	0
0	0	1	0	**1**
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	**1**
0	1	1	1	0
1	0	0	0	**1**
1	0	0	1	0
1	0	1	0	X
1	0	1	1	X
1	1	0	0	X
1	1	0	1	X
1	1	1	0	X
1	1	1	1	X

b) Write the sum-of-products (SOP) expression for E (5 marks)

E=d’c’b’a’ + d’c’b a’ +d’cba’ +d c’b’a’

ID Number: ……..………………….

[**CLEARLY** write your ID number in the space shown above]

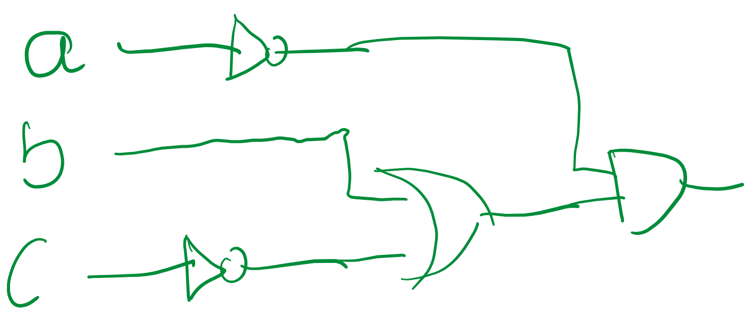
c) Use a K-map to simplify the logic expression for E. (10 marks)

(Write your answer in the table provided below. Clearly mark the loop(s) of adjacent 1s.

	b'a'	b'a	ba	ba'
d'c'	1	0	0	1
d'c	0	0	0	1
dc	X	x	x	x
dc'	1	0	x	x

E = c'a' + ba' = a'(b+c')

d) Draw a logic diagram for G using as **few gates as possible**. (10 marks)

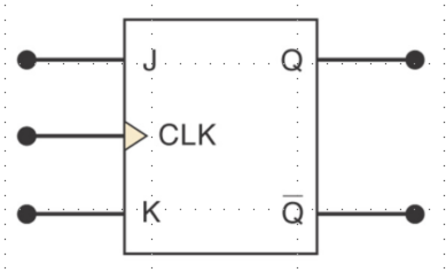


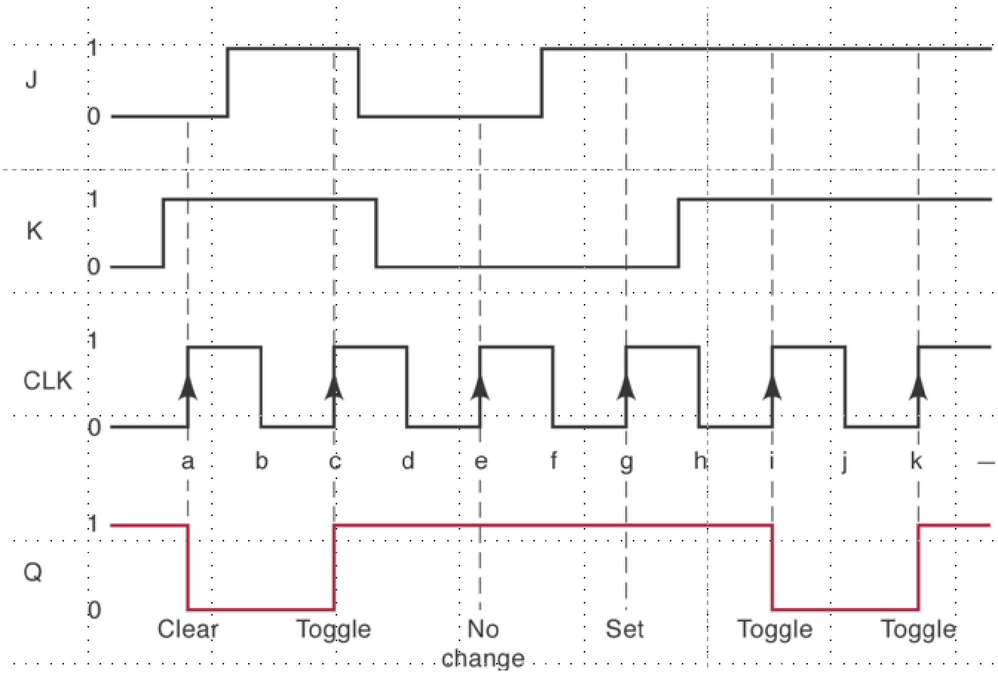
ID Number: ……..…………………

[**CLEARLY** write your ID number in the space shown above]

Question 3 – Latches and Flip Flops **15 marks**

For the Flip Flop and the timing diagram below, draw the resulting output waveform Q. **Explain the reason for each change in the value of Q**. Assume Q starts **high**.





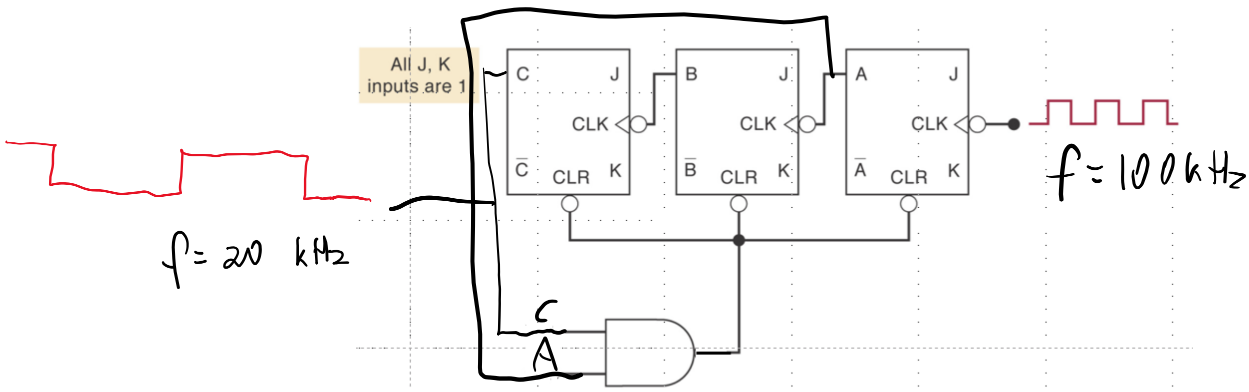
ID Number: ……..…………………

[**CLEARLY** write your ID number in the space shown above]

Question 4 – Counters and Frequency Dividers **25 marks**

a) Using J-K Flip Flops, design a circuit that produces a 20 kHz clock from a 100kHz clock. You must use an **asynchronous** design. (7 marks)

To divide the clock by 5, we need a MOD 5 counter. Thus, we use 3 JK FFs and use C=A=1 to reset it at 5. All J,K inputs = 1.



b) Using J-K Flip Flops, design a logic circuit that produces a 30 kHz clock from a 90 kHz clock. This time use a **synchronous** design. (18 marks)
Hint: What is the Mod Number? How many FFs do you need? You can use the JK excitation table at the back of the test.

We require a MOD 3 counter, so 2 FFs are needed. The states of the counter are: 00 – 01 – 10 – 00 … Use excitation table for JK:

Q(n)		Q(n+1)		J1	K1	J0	K0
B	A	B	A				
0	0	0	1	0	x	1	x
0	1	1	0	1	x	x	1
1	0	0	0	x	1	0	x
1	1	x	x	x	x	x	x

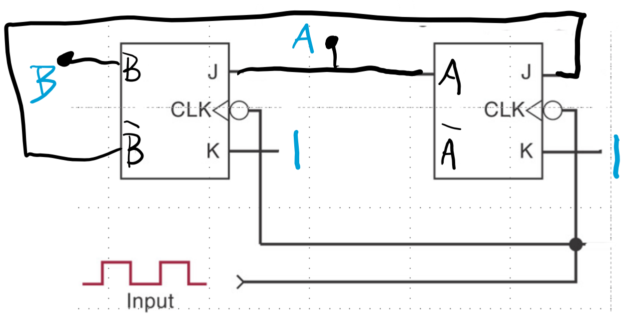
J1	A'	A
B'	0	1
B	x	x

K1	A'	A
B'	x	x
B	1	x

J0	A'	A
B'	1	x
B	0	x

K0	A'	A
B'	x	1
B	x	x

J1=A, J0=B', K1=1, K0=1;



ID Number: ……..………………….

[**CLEARLY** write your ID number in the space shown above]

ID Number: …….....………………….

[**CLEARLY** write your ID number in the space shown above]

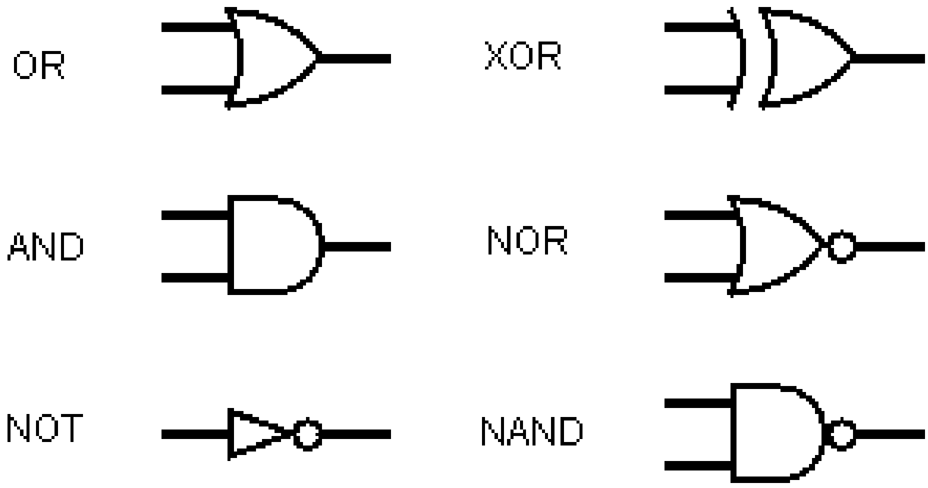
Fundamental Laws and Theorems of Boolean Algebra

1.	$X + 0 = X$	OR operations
2.	$X + 1 = 1$	
3.	$X + X = X$	
4.	$X + \overline{X} = 1$	
5.	$X . 0 = 0$	AND operations
6.	$X . 1 = X$	
7.	$X . X = X$	
8.	$X . \overline{X} = 0$	
9.	$\overline{\overline{X}} = X$	Double complement
10.	$X + Y = Y + X$	Commutative laws
11.	$XY = YX$	
12.	$(X + Y) + Z = X + (Y + Z)$	Associative laws
13.	$(X . Y). Z = X. (Y. Z)$	
14.	$X (Y + Z) = XY + XZ$	Distribution Law
15.	$X + Y .Z = (X + Y) . (X + Z)$	Dual of Distributive Law
16.	$X + XZ = X$	Laws of absorption
17.	$X (X + Z) = X$	
18.	$X + \overline{X} Y = X + Y$	Identity Theorems
19.	$X (\overline{X} + Y) = X.Y$	
20.	$\overline{X+Y} = \overline{X} . \overline{Y}$	De Morgan's Theorems
21.	$\overline{X.Y} = \overline{X} + \overline{Y}$	

ID Number: ……..……………………

[**CLEARLY** write your ID number in the space shown above]

Logic Gate Symbols:



Excitation tables:

JK FF:

Present Q	Next Q	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

D FF:

Present State Q(n)	Next State Q(n+1)	Input D
0	0	0
0	1	1
1	0	0
1	1	1