ID Number: ……...…….

Full Name: …… ……..……..….

**ECEN202**

**DIGITAL ELECTRONICS**

**Practice TEST**

2024

**Time allowed:** 60 MINUTES

**CLOSED BOOK**

**Permitted materials:** No programmable calculators are allowed.

No electronic dictionaries are allowed.

Paper foreign to English language dictionaries are allowed.

**Instructions:** Attempt ALL questions.

There are 4 questions in this test paper:

**Space for working out your solutions is provided at the end of every section.**

| Question | Topic | Allocated Marks | Obtained Marks | |
|---|---|---|---|---|
| 1 | Logic and Boolean Algebra | 25 | | |
| 2 | Combinational Logic | 35 | | |
| 3 | Latches and Flip Flops | 15 | | |
| 4 | Counters and Frequency Dividers | 25 | | |
| | **TOTAL** | **100** | | |

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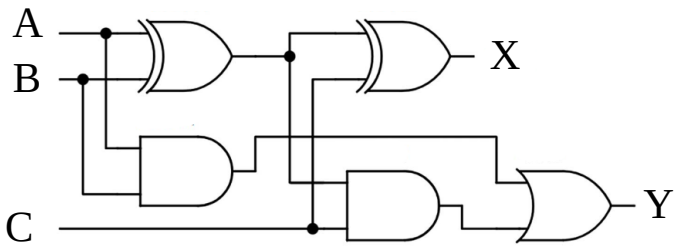
**Question 1 – Logic and Boolean Algebra** **25 marks**

a) Write the Boolean expression for the outputs X and Y of the following circuit. (10 marks)




X = _____

Y = _____

b) Draw a circuit diagram for **X** in part a) using only AND, OR and NOT gates. (8 marks)

c) Simplify using Boolean Algebra (3 marks)

$$X = (\overline{A\bar{B}})(\bar{A} + B)(\bar{B} + B)$$

a) Simplify using Boolean Algebra (4 marks)

$$X = ABC + A\bar{B}(\overline{\bar{A}\bar{C}})$$

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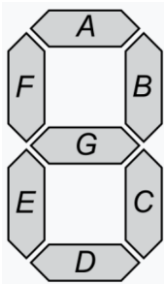
**Question 2 – Combinational Logic** **35 marks**

We want to design a logic circuit for a 7-segment LED display shown below.




The inputs are 4 binary digits **d**, **c**, **b**, **a**, which represent the number to be displayed on the LED. Bit **d** is the most significant bit (MSB), and **a** is the least significant bit (LSB). Each LED segment (labelled A, B, C, … G on the diagram) has its own logic. For example, LED D is ON when **dcba** represent decimal numbers 0, 2, 3, 5, 6, 8 or 9.

a) Produce a truth table to drive LED labelled **E** (10 marks)

| d | c | b | a | E |
|---|---|---|---|---|
| | | | | |
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b) Write the sum-of-products (SOP) expression for E (5 marks)

c) Use a K-map to simplify the logic expression for E. (10 marks)

(Write your answer in the table provided below. Clearly mark the loop(s) of adjacent 1s.

| | | | | |
|---|---|---|---|---|
| | | | | |
| | | | | |
| | | | | |
| | | | | |

E =

d) Draw a logic diagram for G using as **few gates as possible**. (10 marks)

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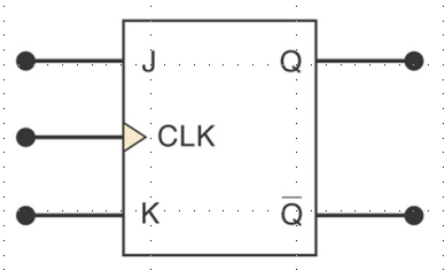
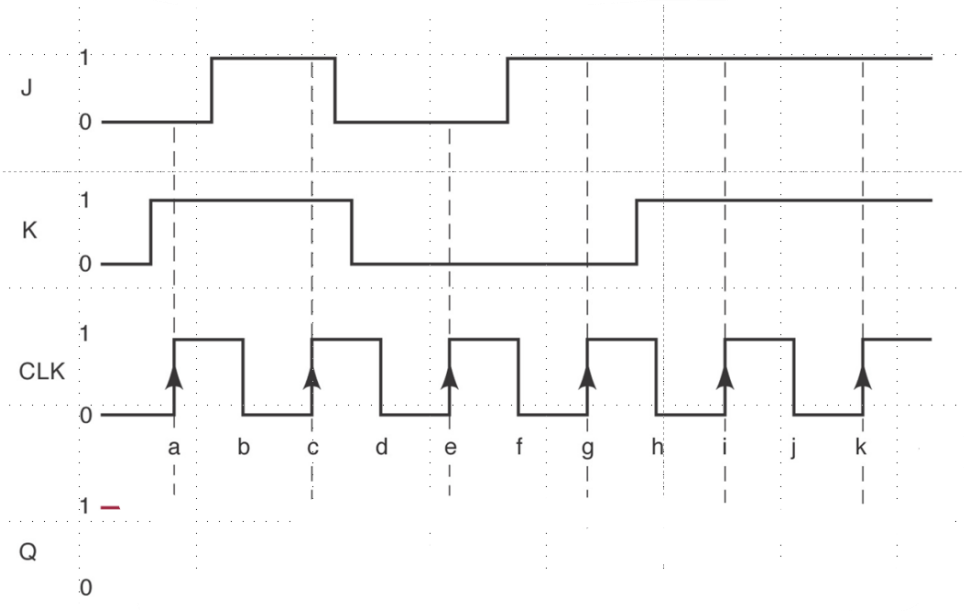
**Question 3 – Latches and Flip Flops** **15 marks**

For the Flip Flop and the timing diagram below, draw the resulting output waveform Q. **Explain the reason for each change in the value of Q**. Assume Q starts **high**.



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**Question 4 – Counters and Frequency Dividers** **25 marks**

a) Using J-K Flip Flops, design a circuit that produces a 20 kHz clock from a 100kHz clock. You must use an **asynchronous** design. (7 marks)

b) Using J-K Flip Flops, design a logic circuit that produces a 30 kHz clock from a 90 kHz clock. This time use a **synchronous** design. (18 marks)
Hint: What is the Mod Number? How many FFs do you need? You can use the JK excitation table at the back of the test.

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# Fundamental Laws and Theorems of Boolean Algebra

| | | |
|---|---|---|
| 1. | $X + 0 = X$ | OR operations |
| 2. | $X + 1 = 1$ | |
| 3. | $X + X = X$ | |
| 4. | $X + \overline{X} = 1$ | |
| 5. | $X \cdot 0 = 0$ | AND operations |
| 6. | $X \cdot 1 = X$ | |
| 7. | $X \cdot X = X$ | |
| 8. | $X \cdot \overline{X} = 0$ | |
| 9. | $\overline{\overline{X}} = X$ | Double complement |
| 10. | $X + Y = Y + X$ | Commutative laws |
| 11. | $XY = YX$ | |
| 12. | $(X + Y) + Z = X + (Y + Z)$ | Associative laws |
| 13. | $(X \cdot Y) \cdot Z = X \cdot (Y \cdot Z)$ | |
| 14. | $X(Y + Z) = XY + XZ$ | Distribution Law |
| 15. | $X + Y \cdot Z = (X + Y) \cdot (X + Z)$ | Dual of Distributive Law |
| 16. | $X + XZ = X$ | Laws of absorption |
| 17. | $X(X + Z) = X$ | |
| 18. | $X + \overline{X} Y = X + Y$ | Identity Theorems |
| 19. | $X(\overline{X} + Y) = XY$ | |
| 20. | $\overline{X+Y} = \overline{X} \cdot \overline{Y}$ | De Morgan's Theorems |
| 21. | $\overline{XY} = \overline{X} + \overline{Y}$ | |

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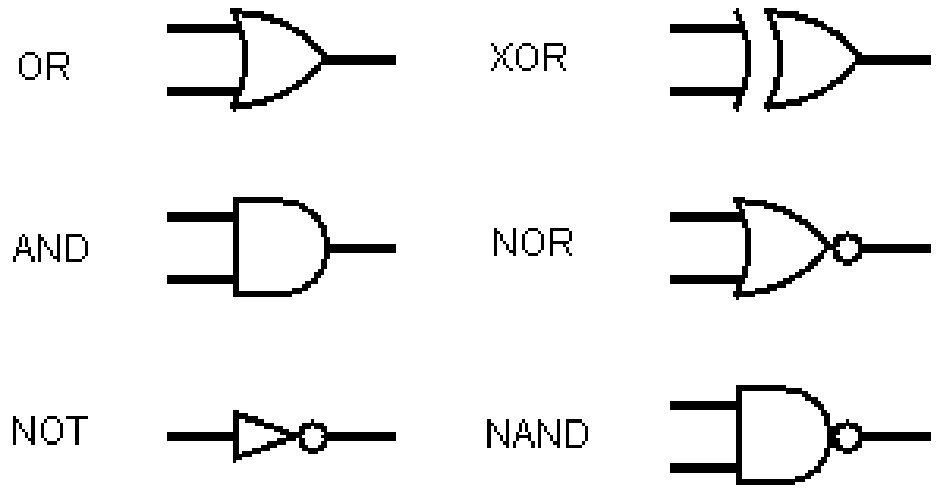
**Logic Gate Symbols:**




**Excitation tables:**

**JK FF:**

| Present Q | Next Q | J | K |
|---|---|---|---|
| 0 | 0 | 0 | x |
| 0 | 1 | 1 | x |
| 1 | 0 | x | 1 |
| 1 | 1 | x | 0 |

**D FF:**

| Present State Q(n) | Next State Q(n+1) | Input D |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |