ENGR 101
Engineering Technology

Felix Yan

School of Engineering and Computer Science
Victoria University of Wellington

Victoria
UNIVERSITY OF WELLINGTON
Te Whare Wānanga
o te Ūpoko o te Ika a Māui

CAPITAL CITY UNIVERSITY

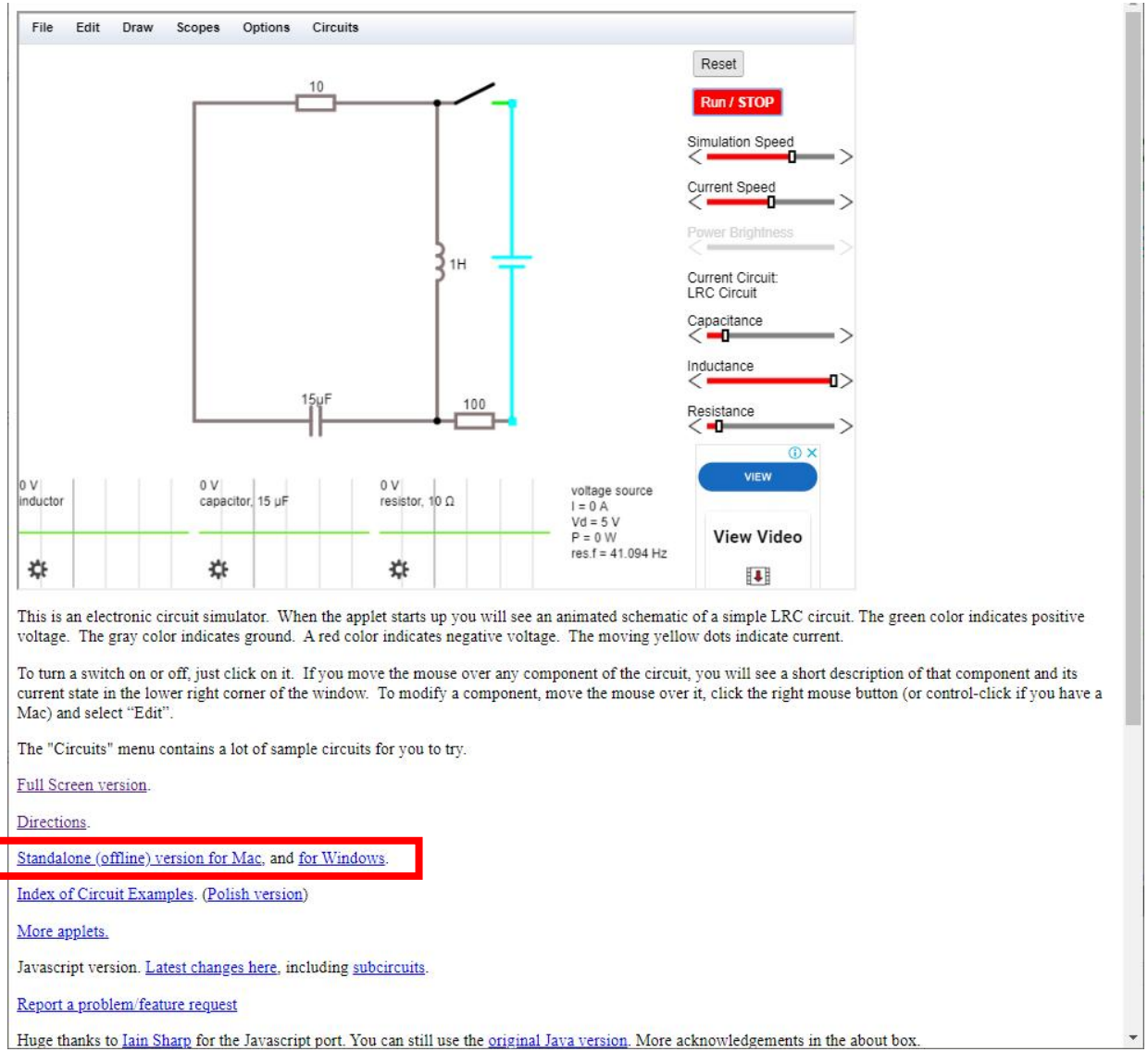
Simulator Address

- Circuit simulator

  https://www.falstad.com/circuit/

Drawing Logic Circuits using on-line simulator

https://www.falstad.com/circuit/



Standalone version

https://www.falstad.com/circuit/

Standalone versions

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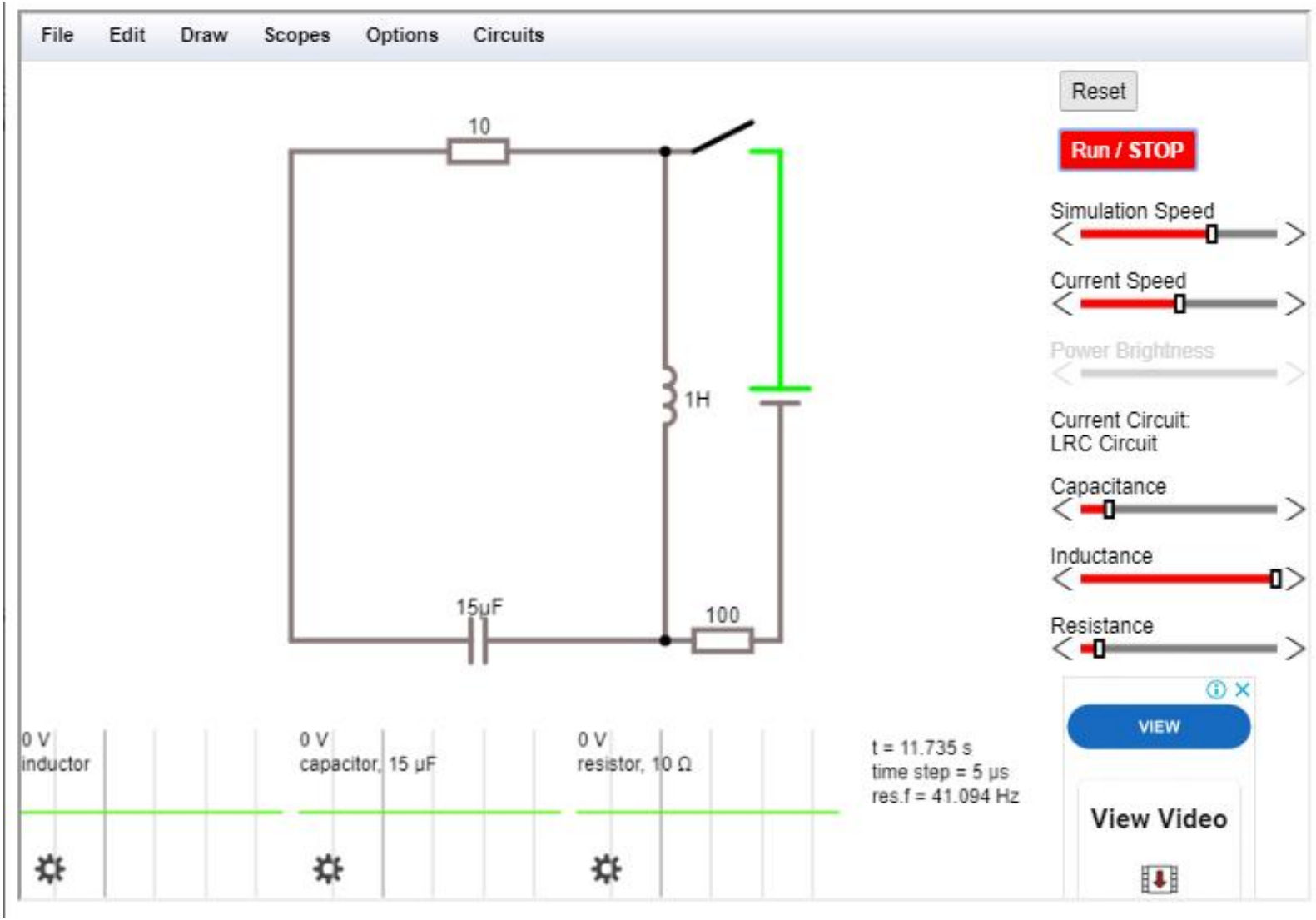

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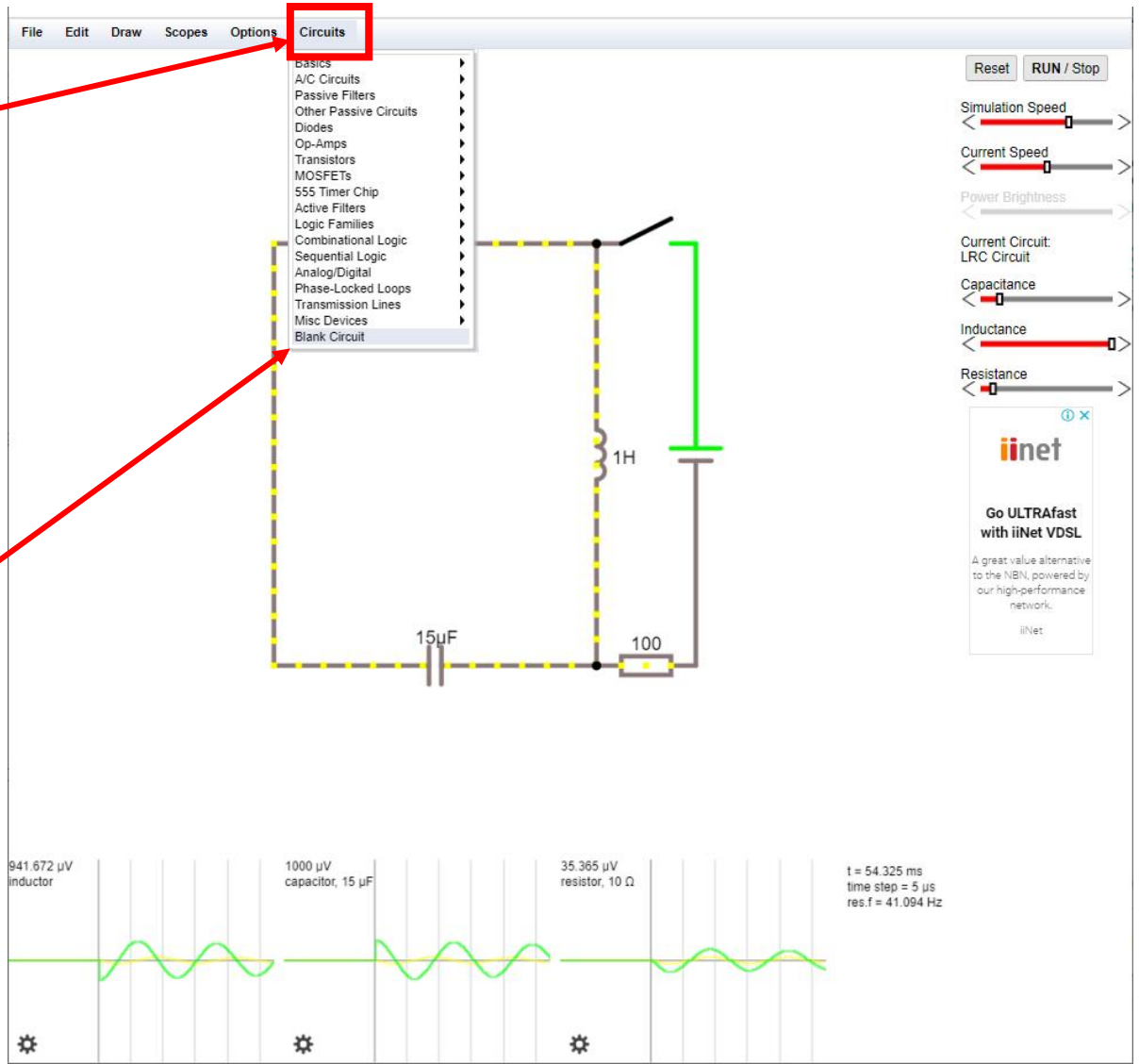
1. Click on the Circuits drop-down menu

2. Click on the Blank Circuit option



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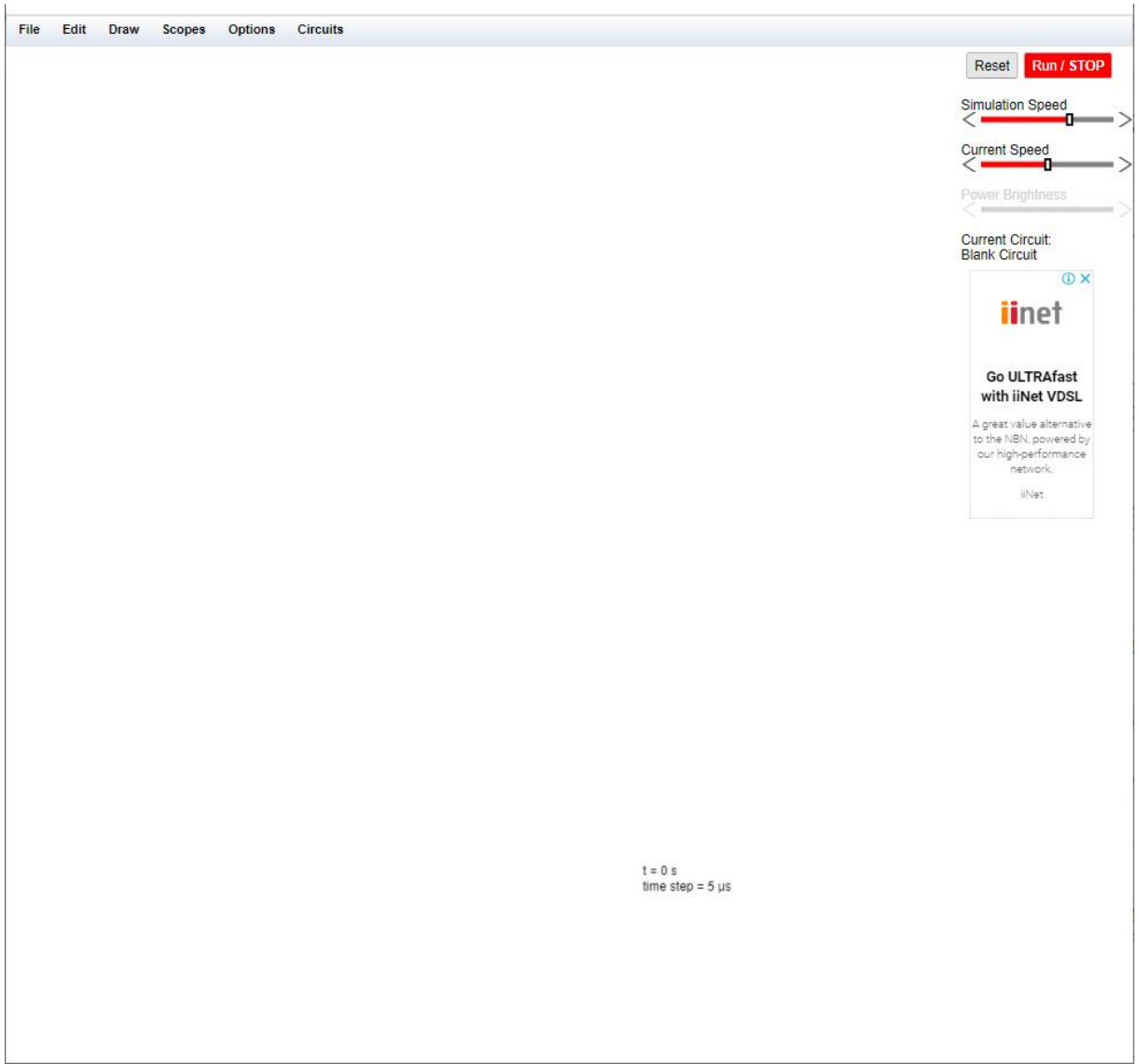

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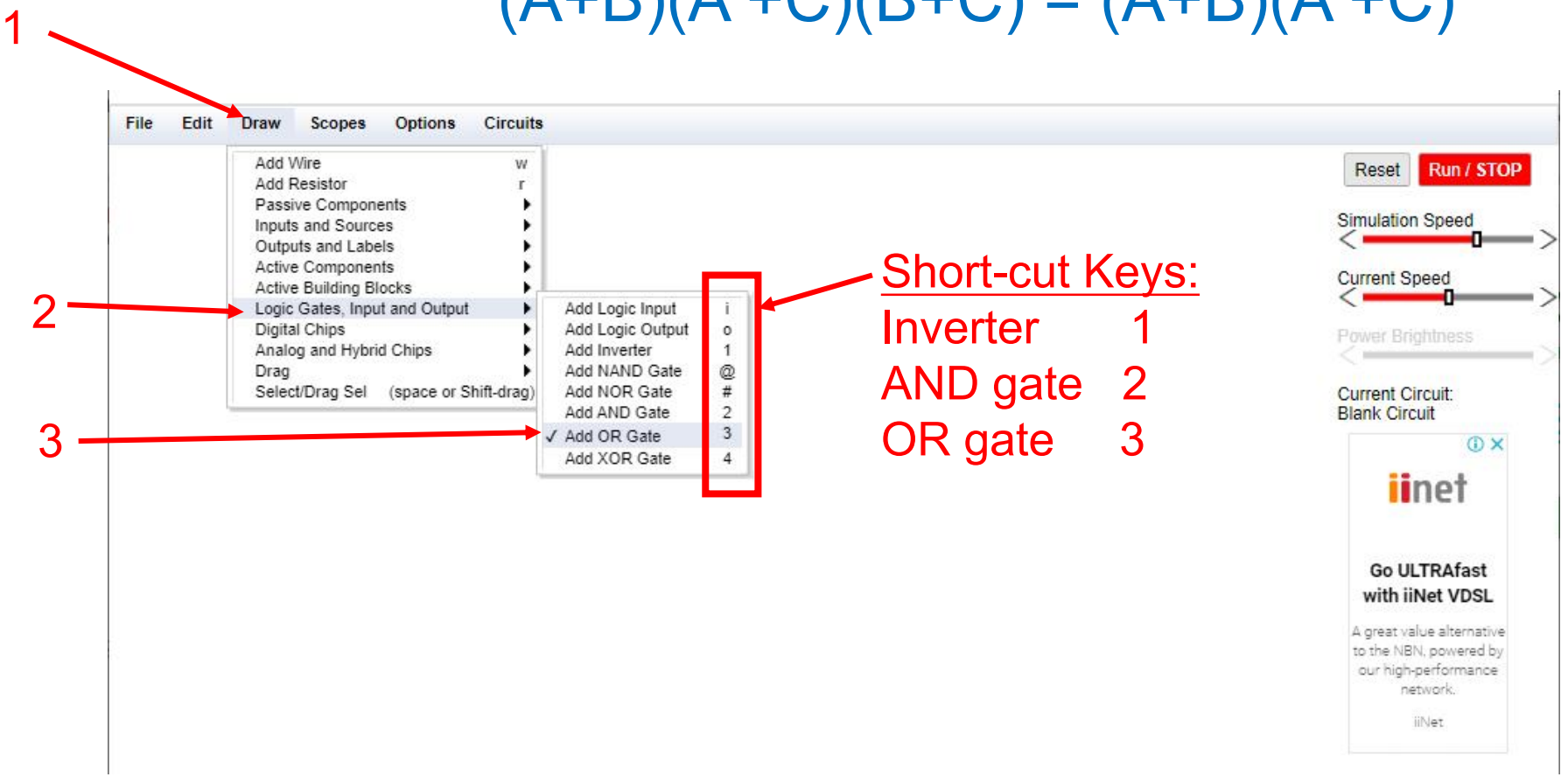

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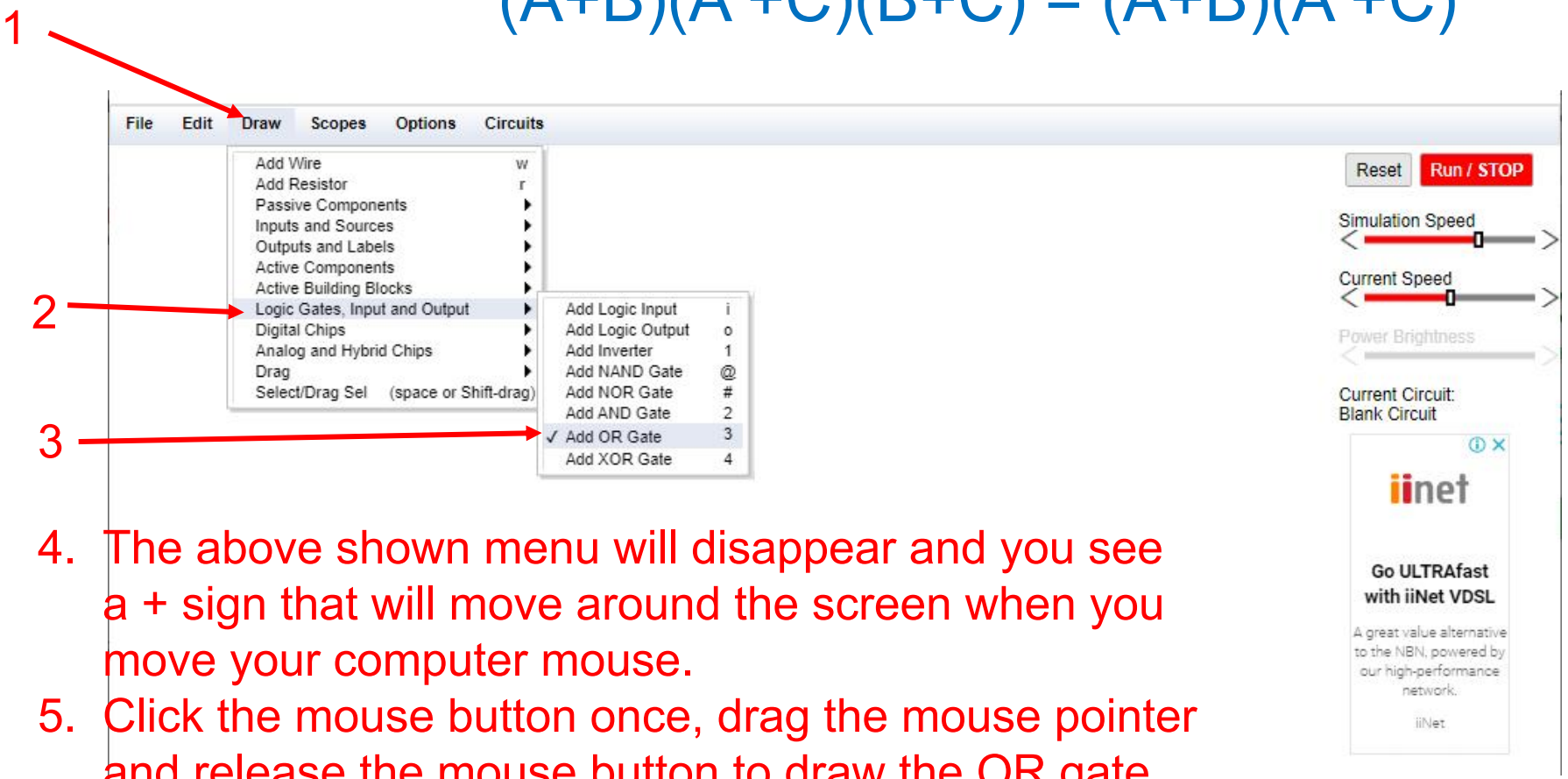

4. The above shown menu will disappear and you see a + sign that will move around the screen when you move your computer mouse.
5. Click the mouse button once, drag the mouse pointer and release the mouse button to draw the OR gate

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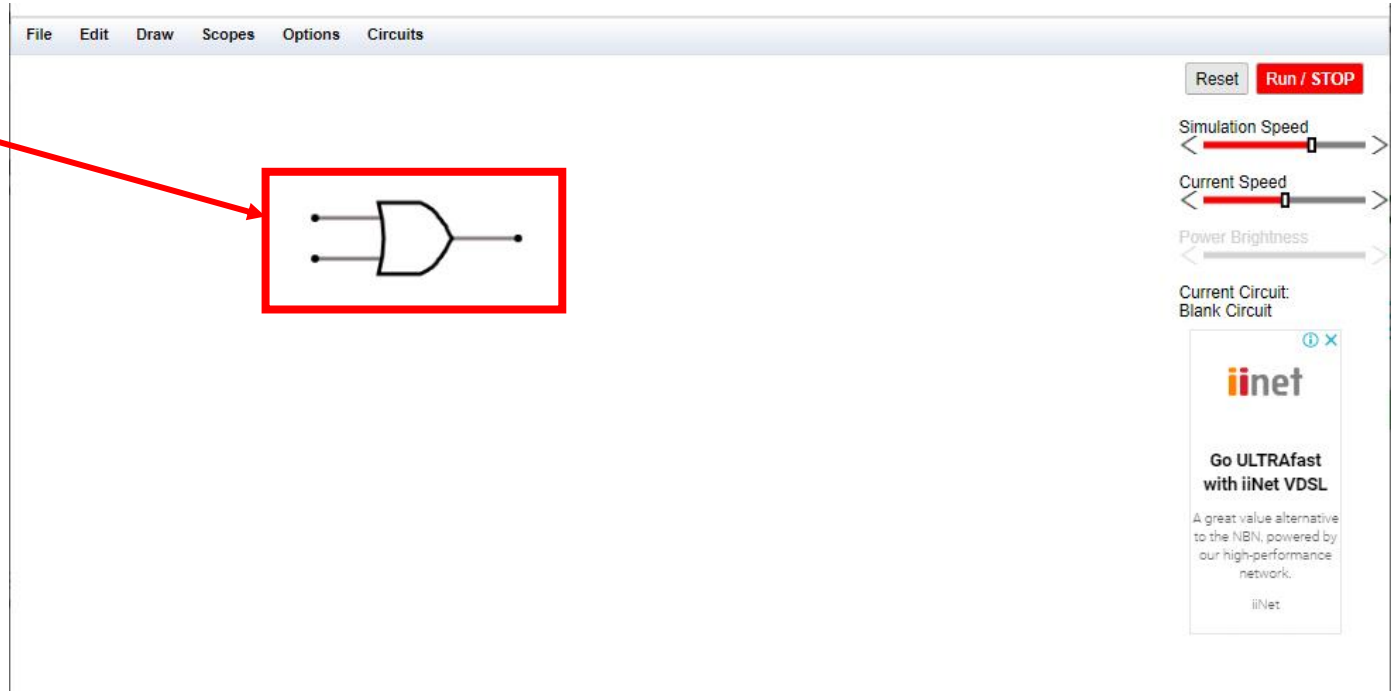

OR gate

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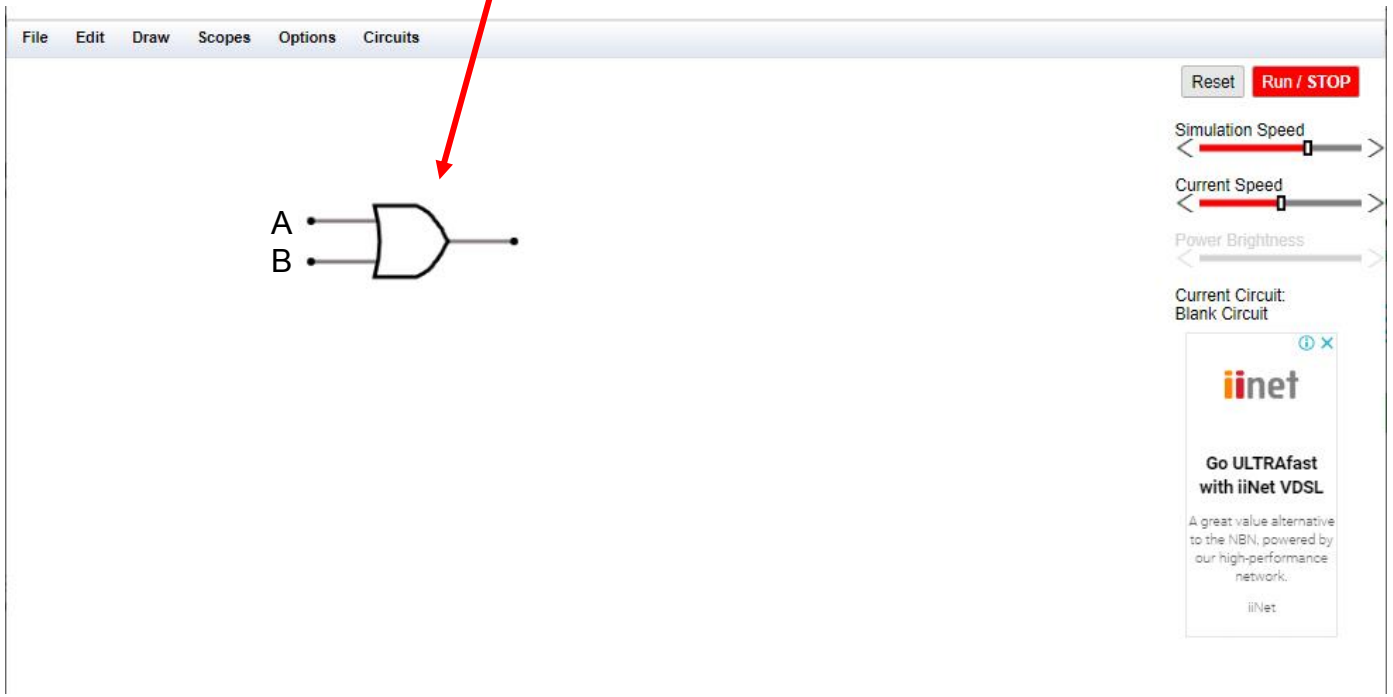

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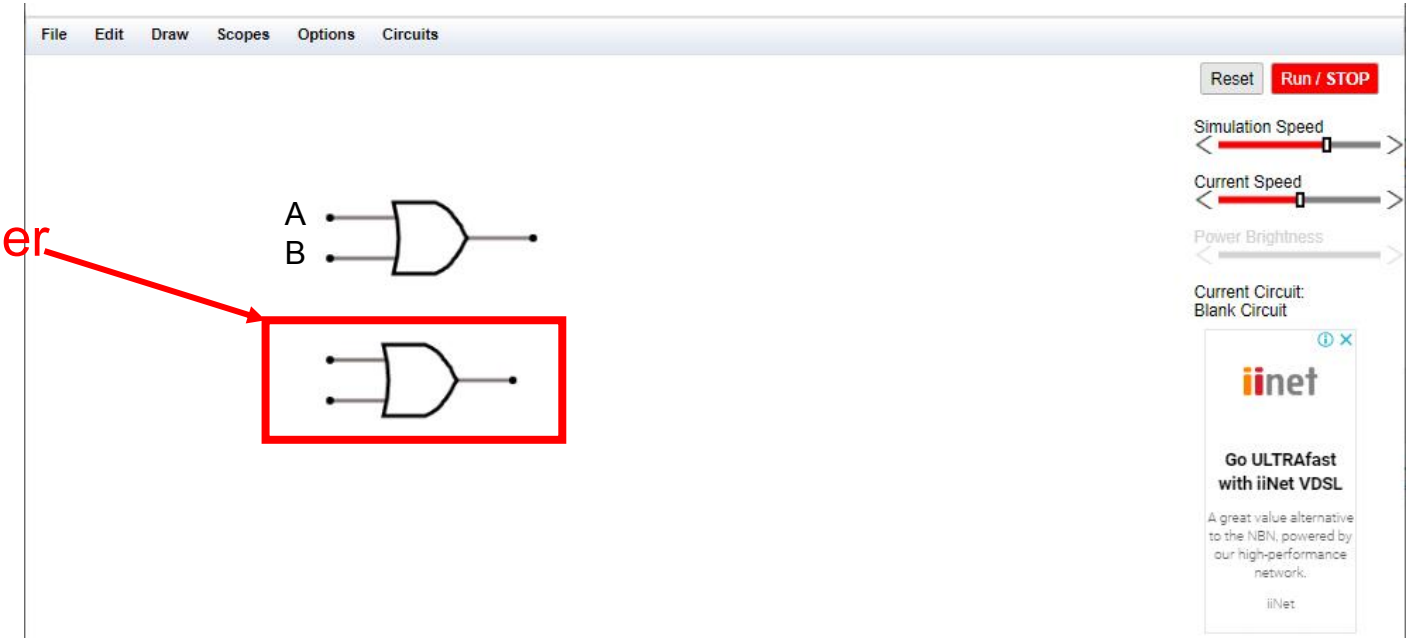
Add another OR gate



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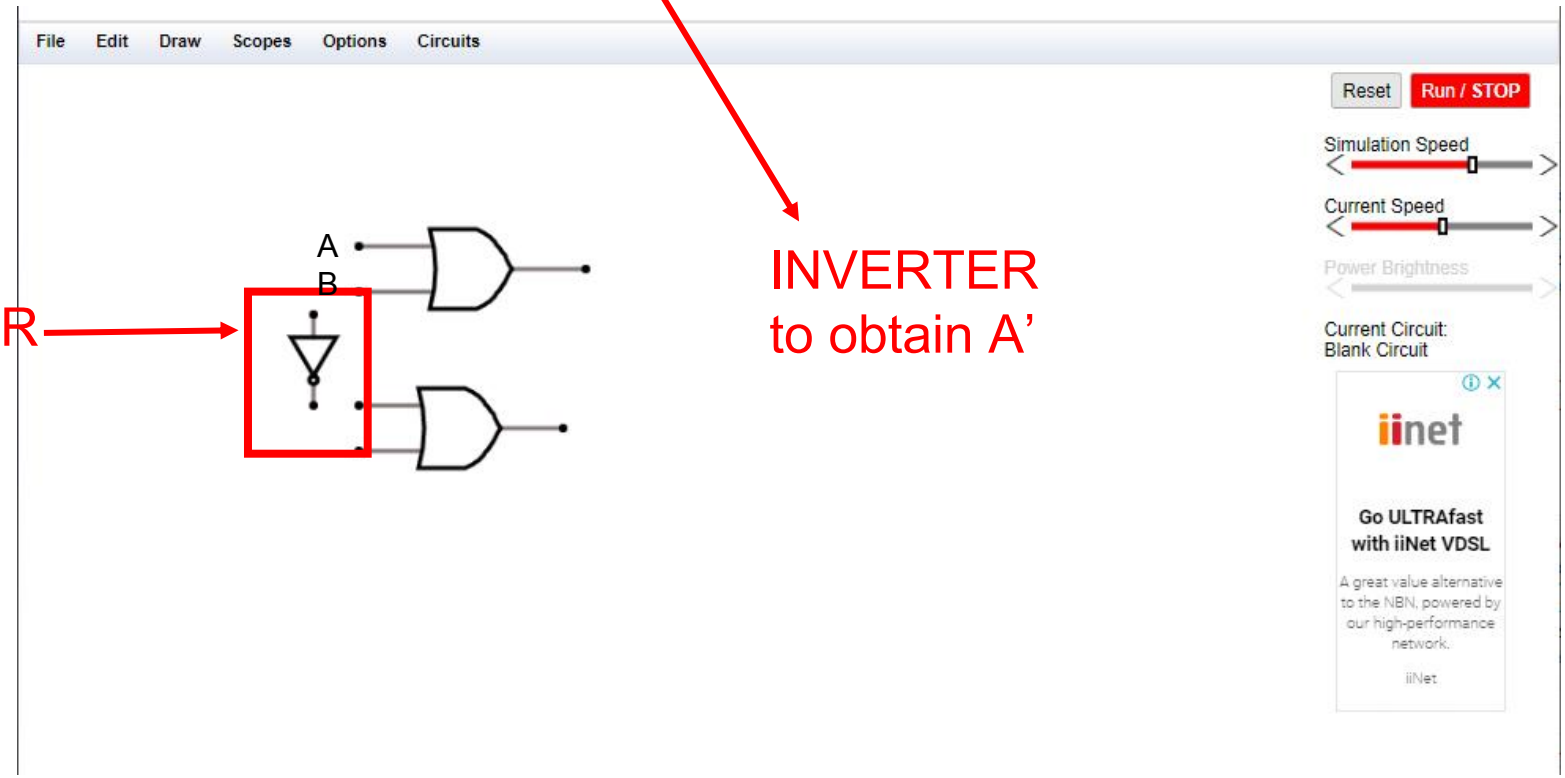

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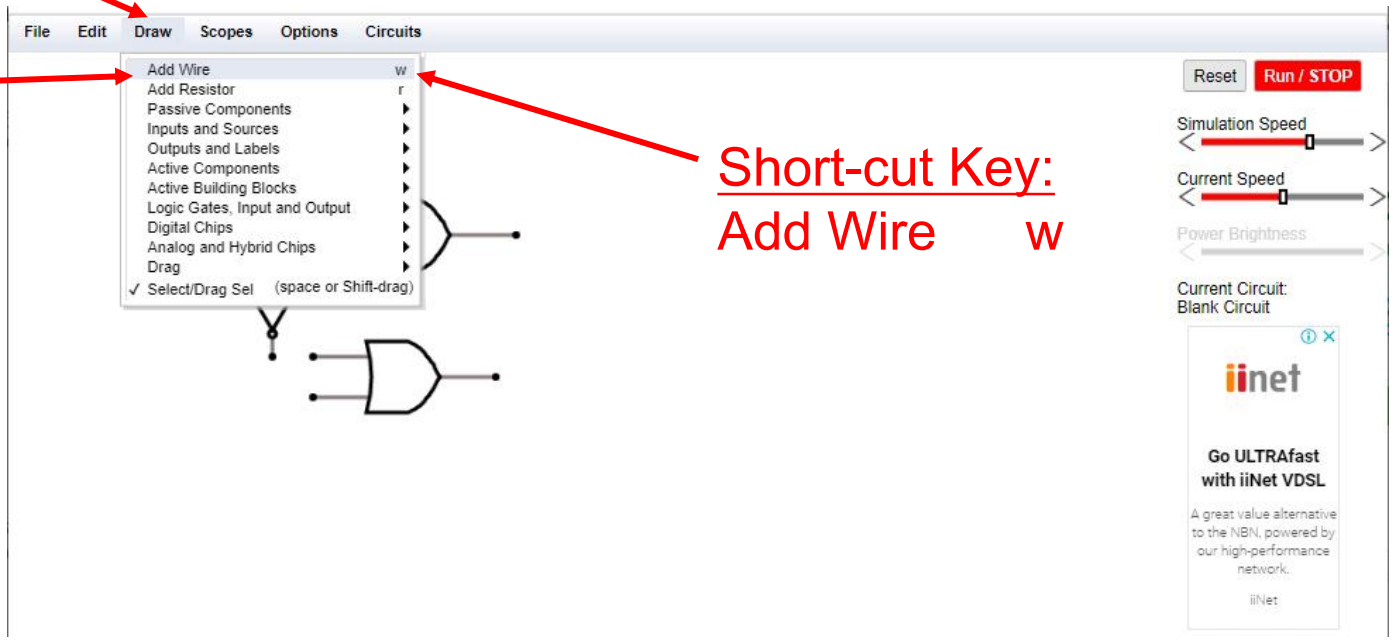
1

2



Short-cut Key:
Add Wire w

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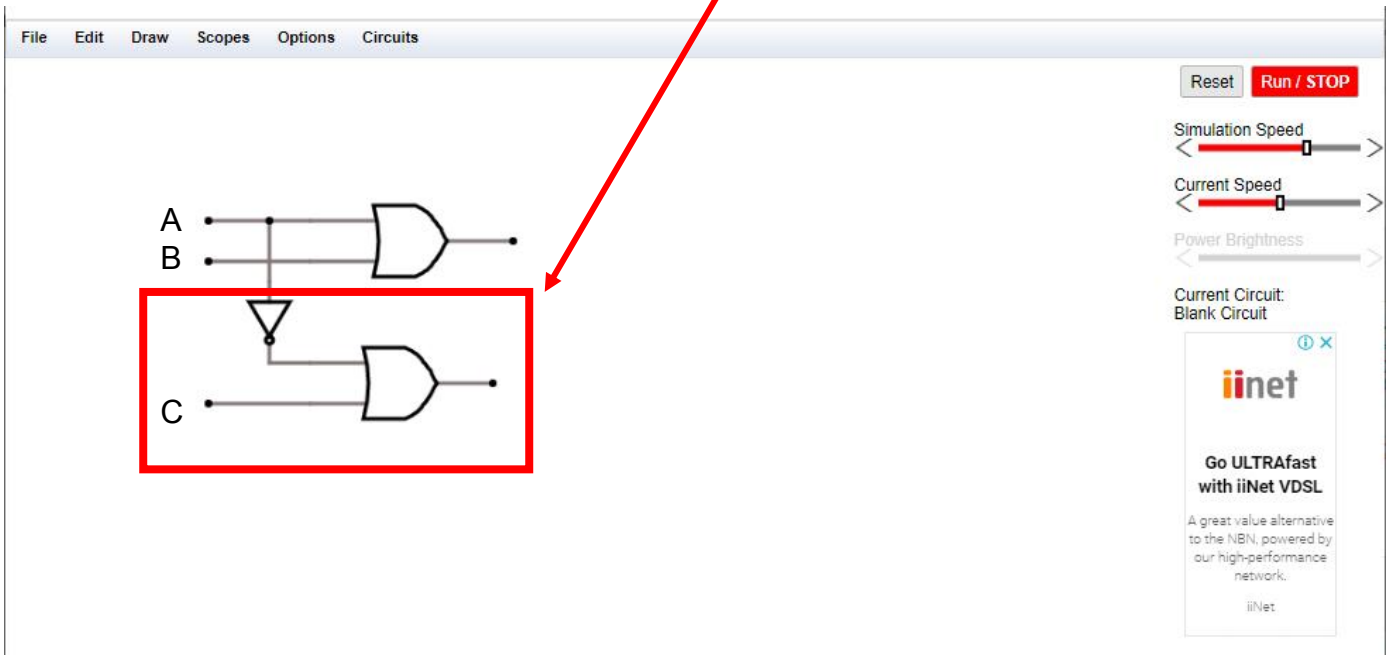

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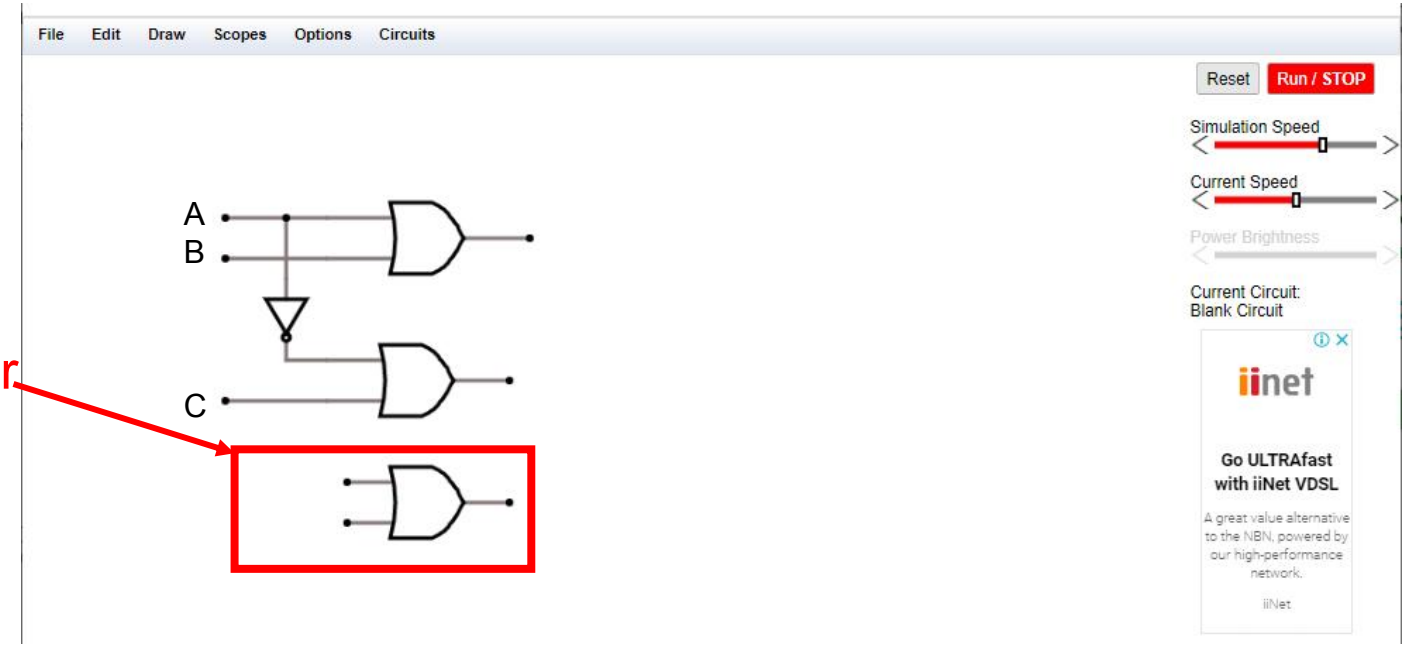

Add another OR gate

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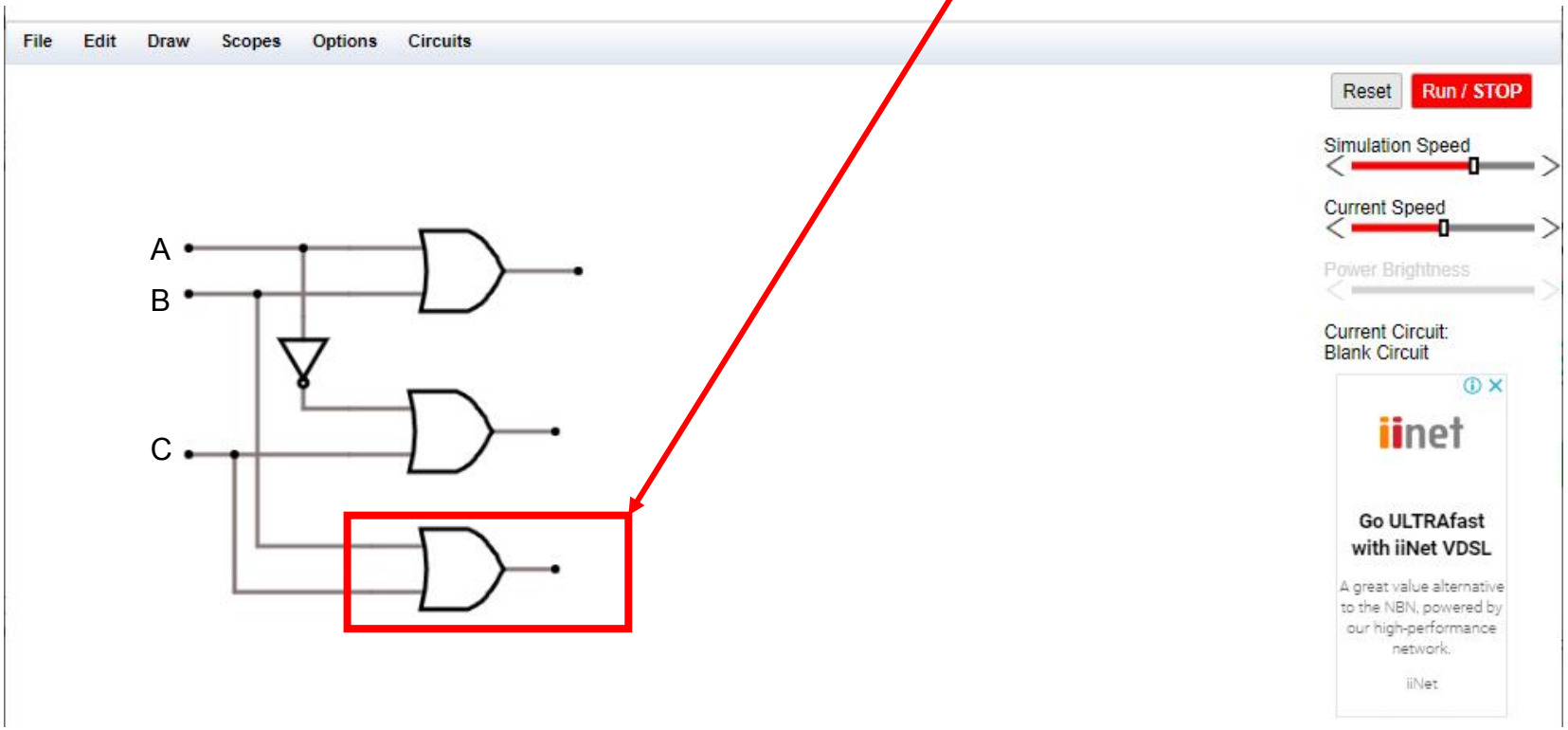

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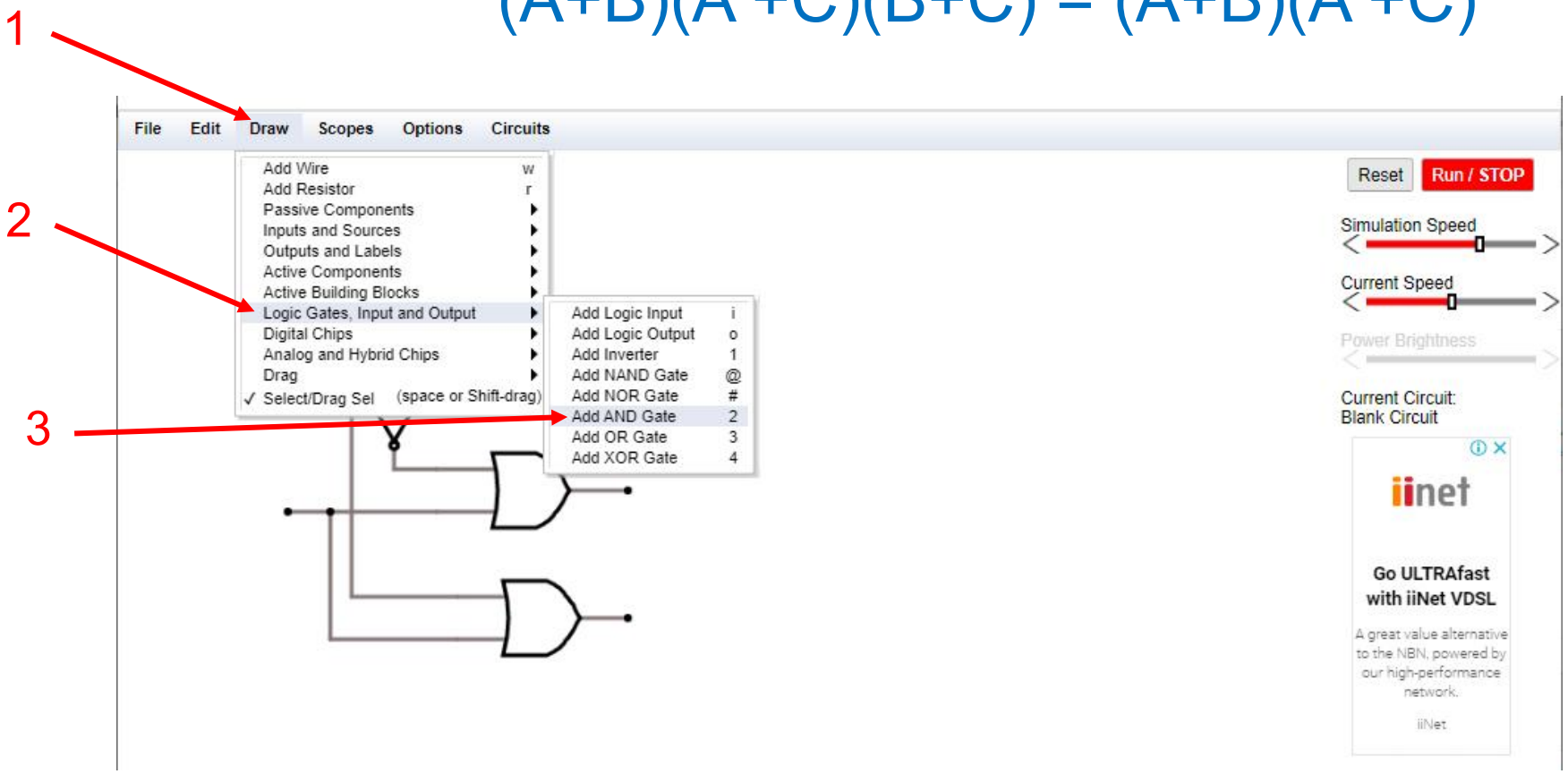

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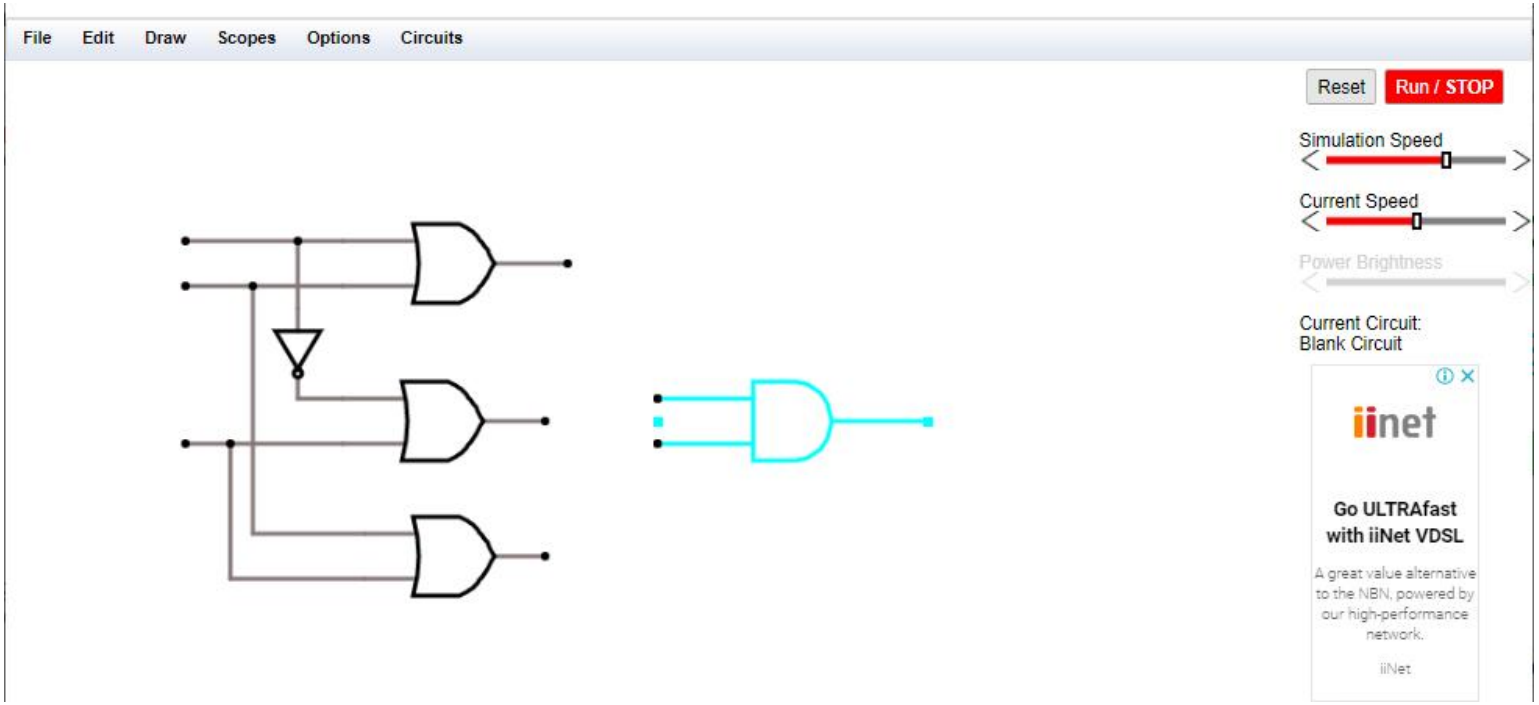

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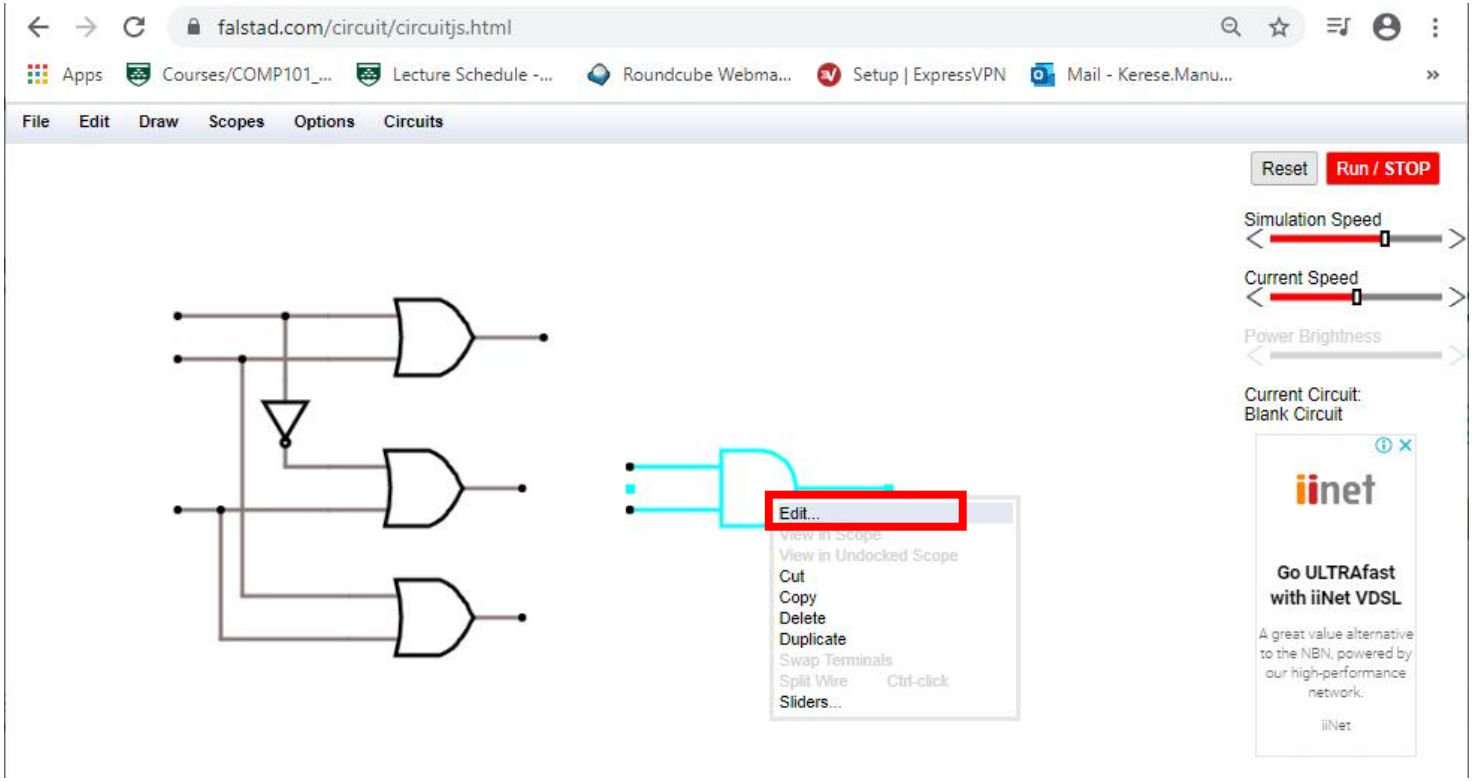

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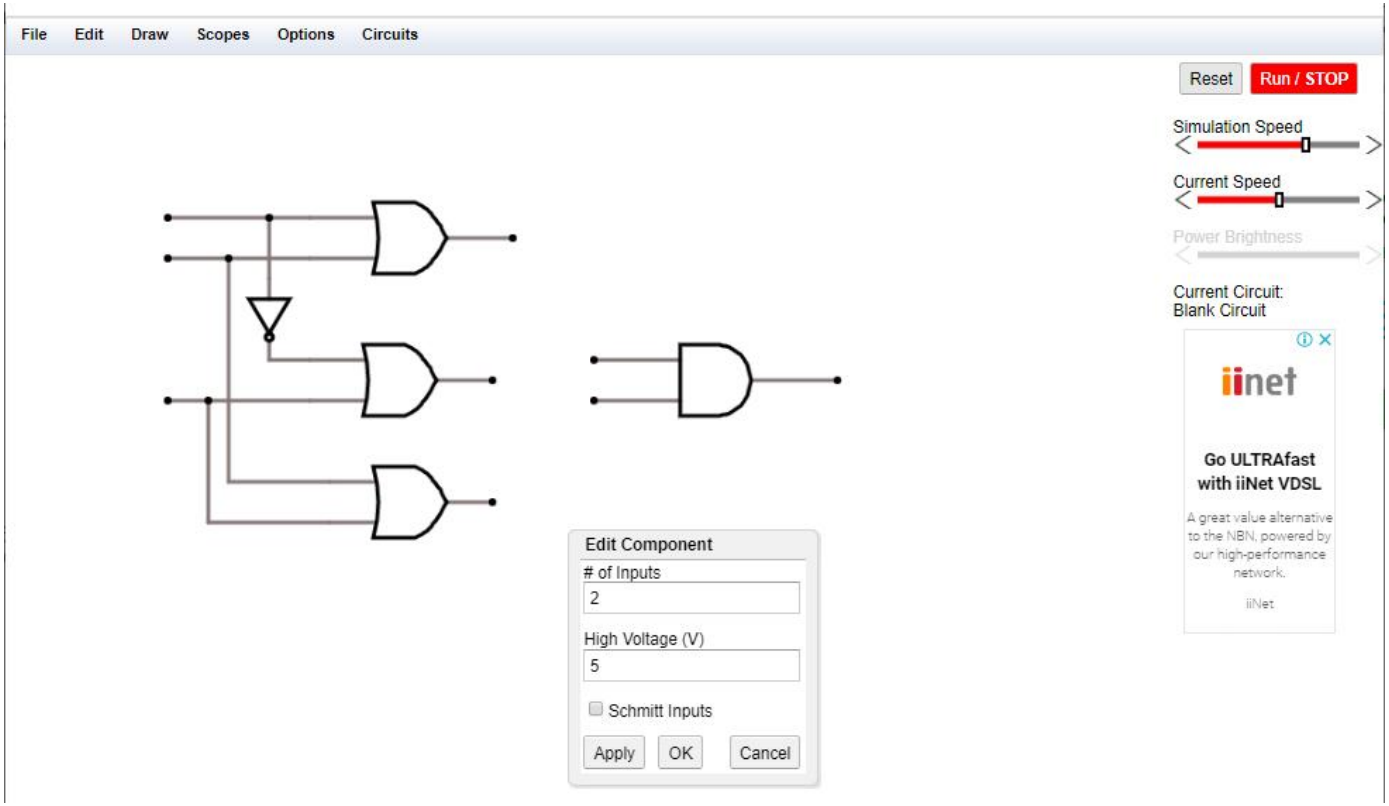

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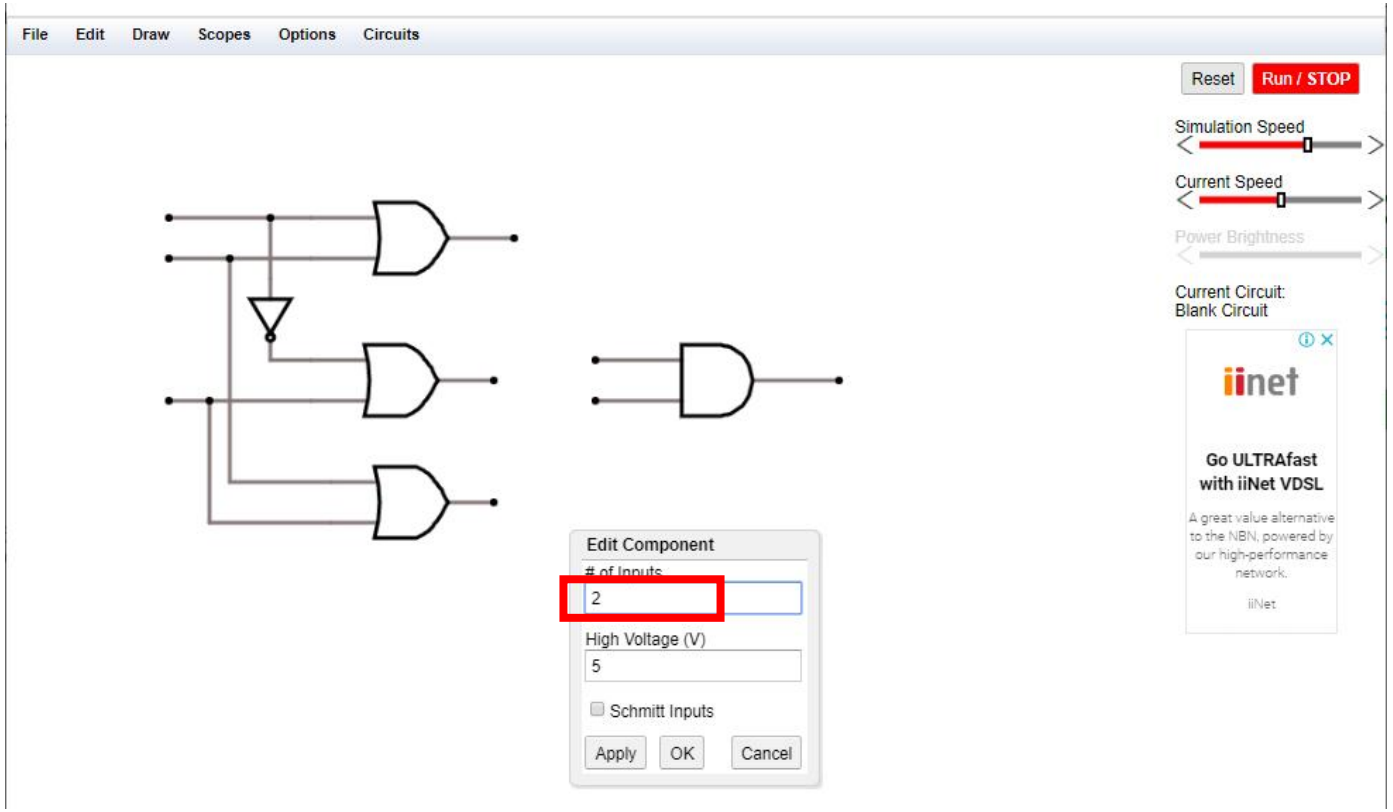

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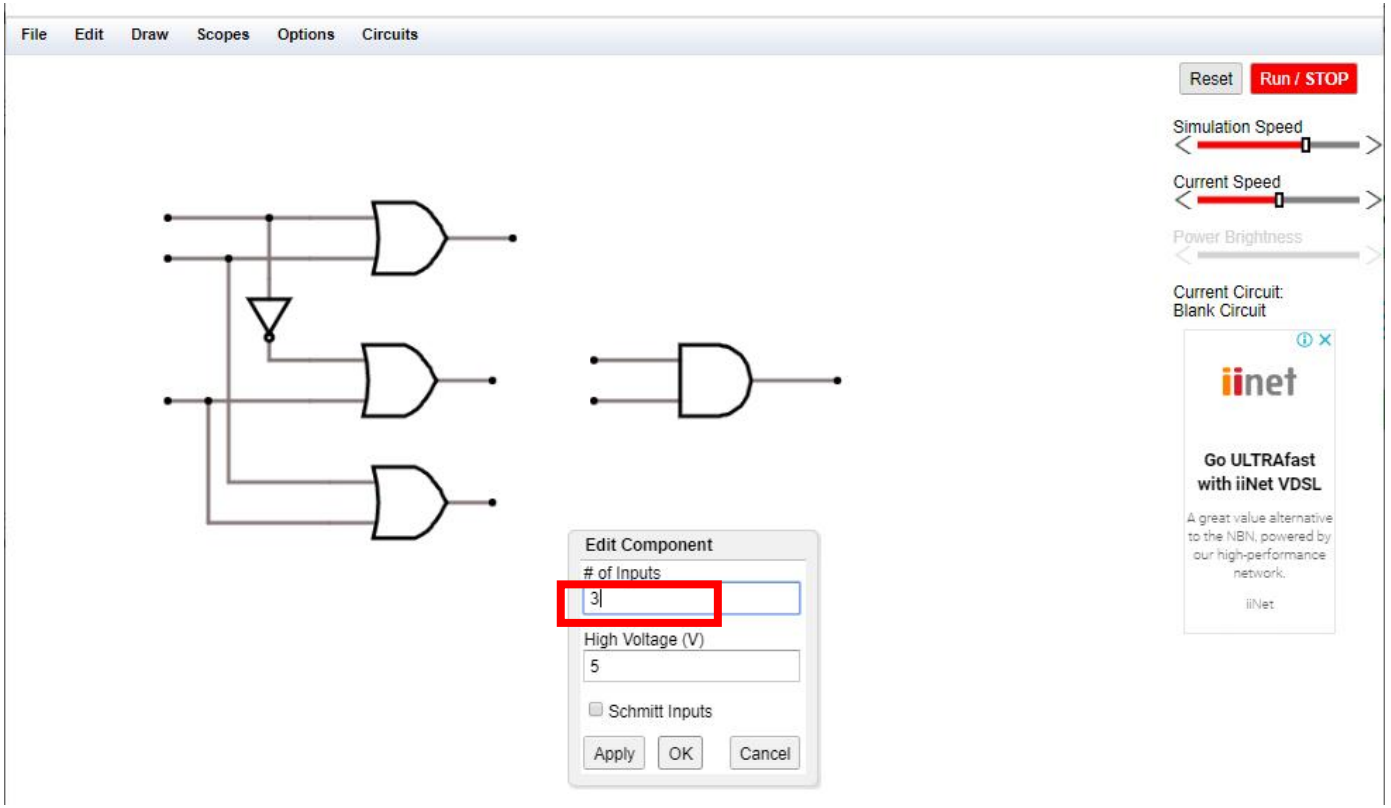

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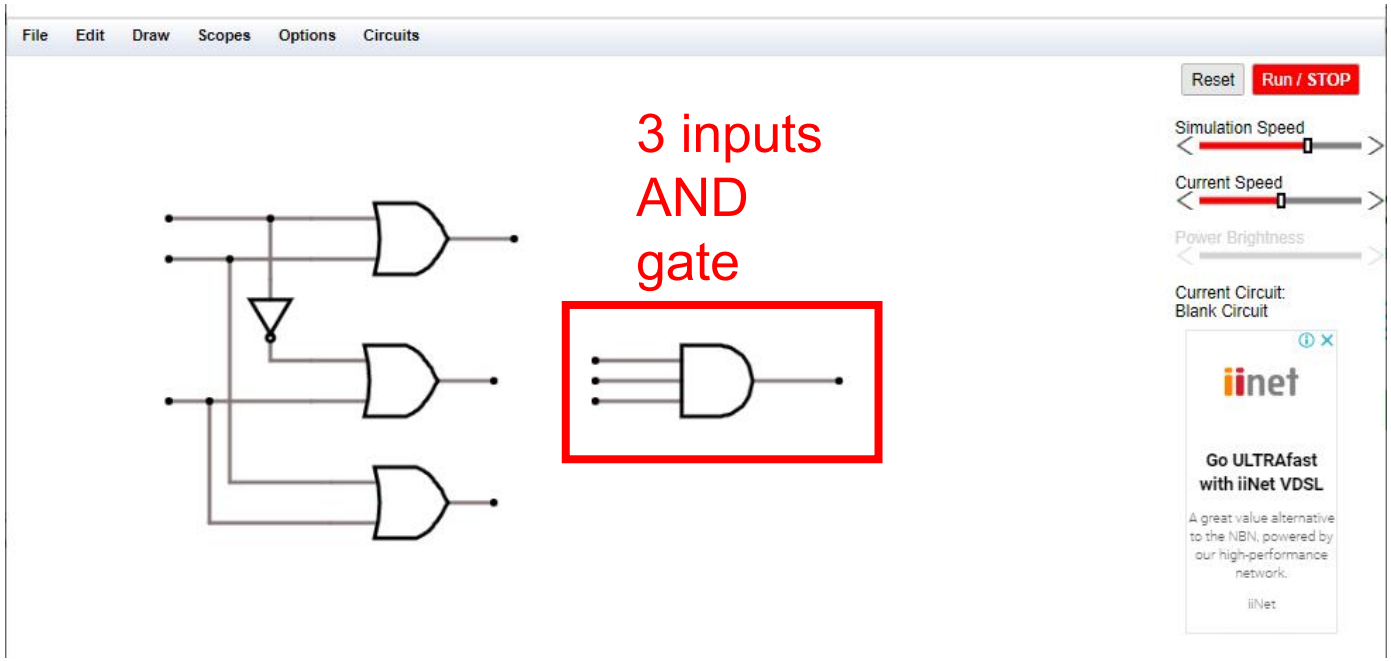

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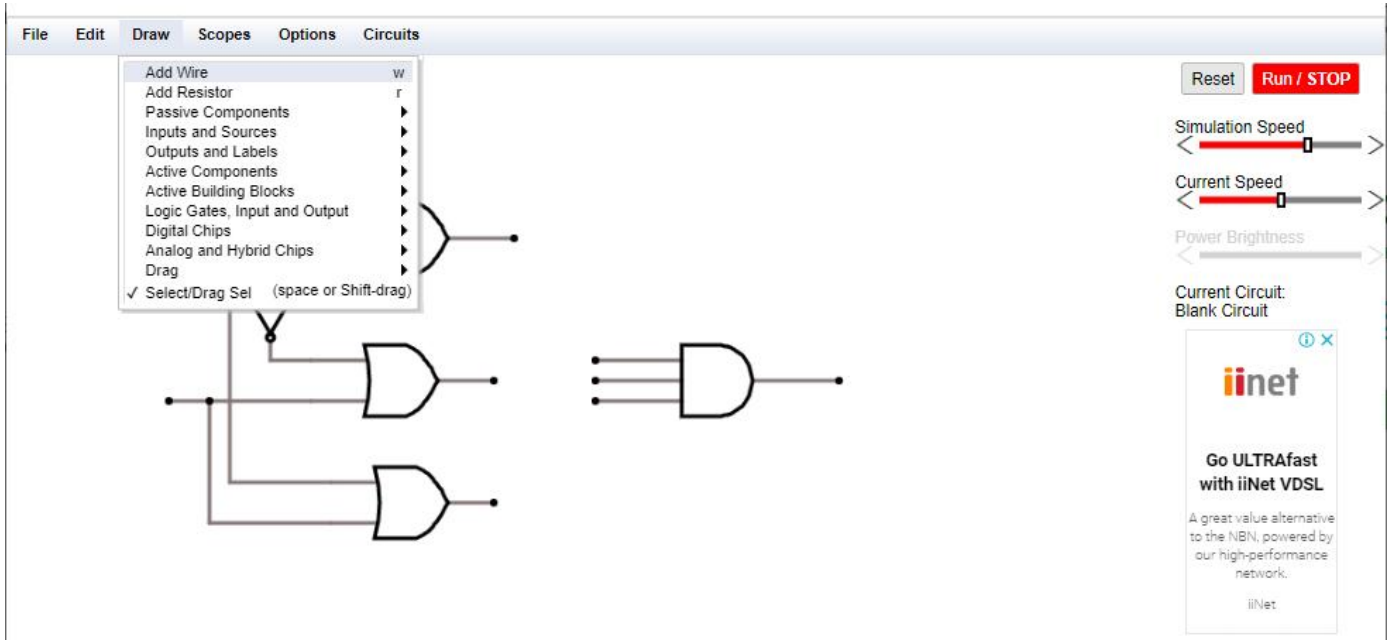

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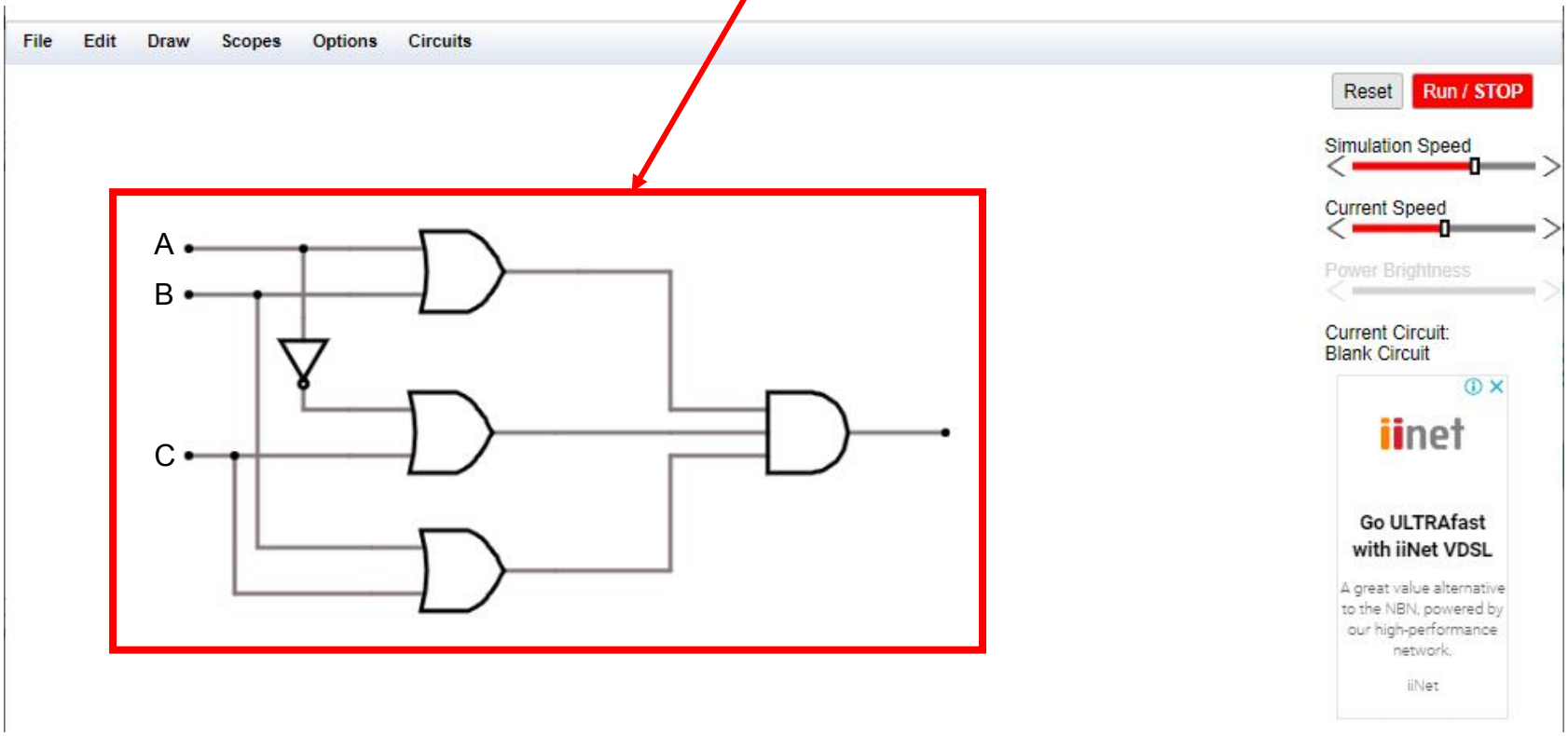

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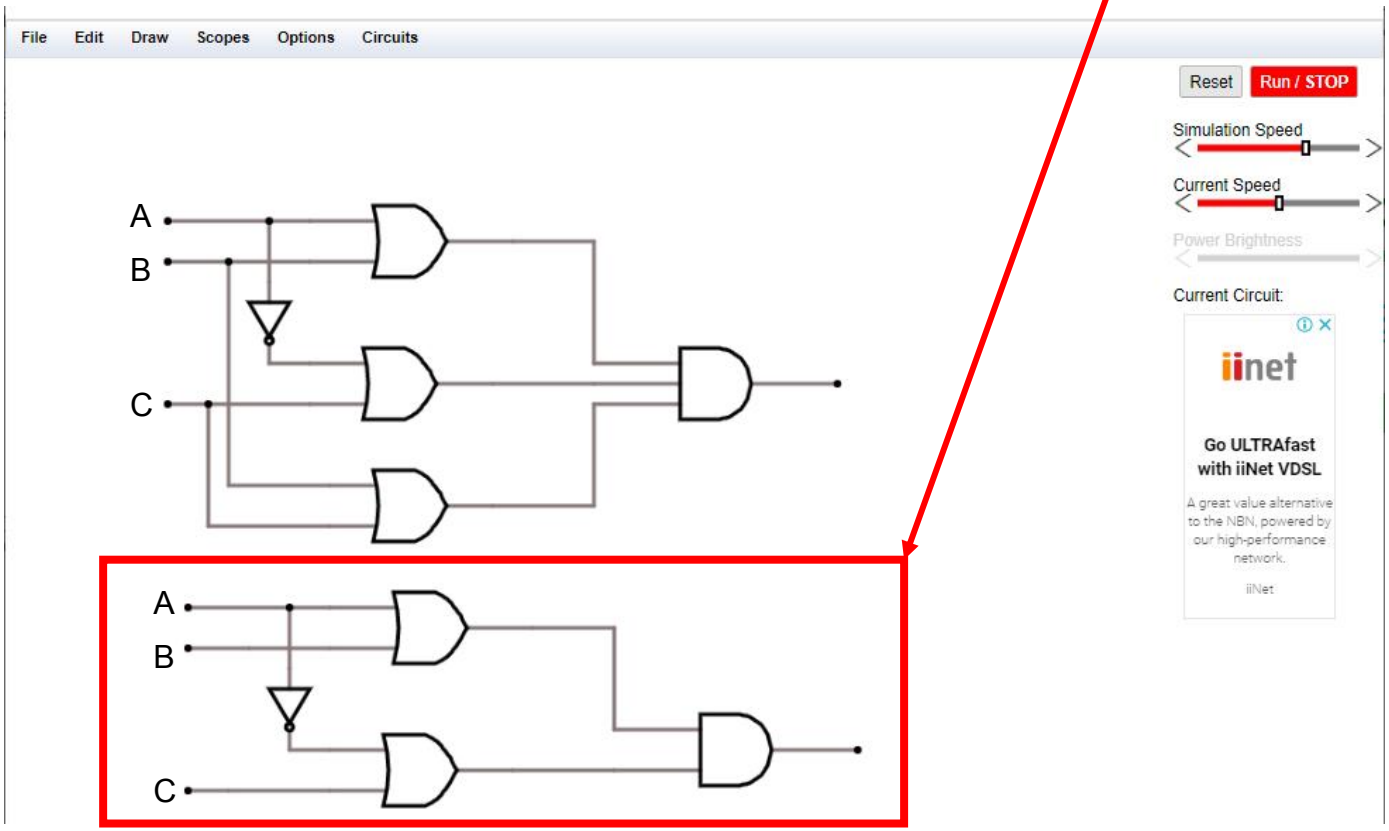

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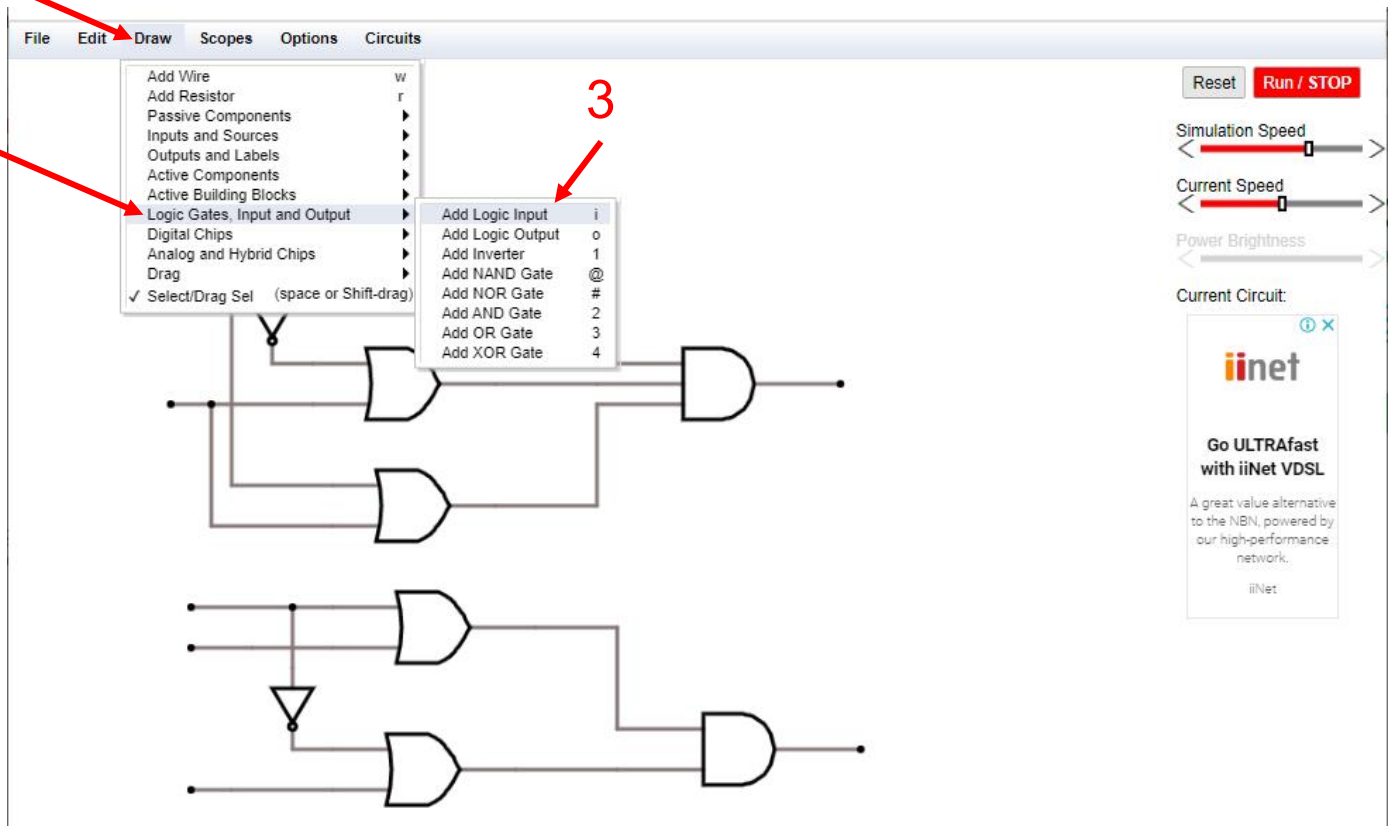

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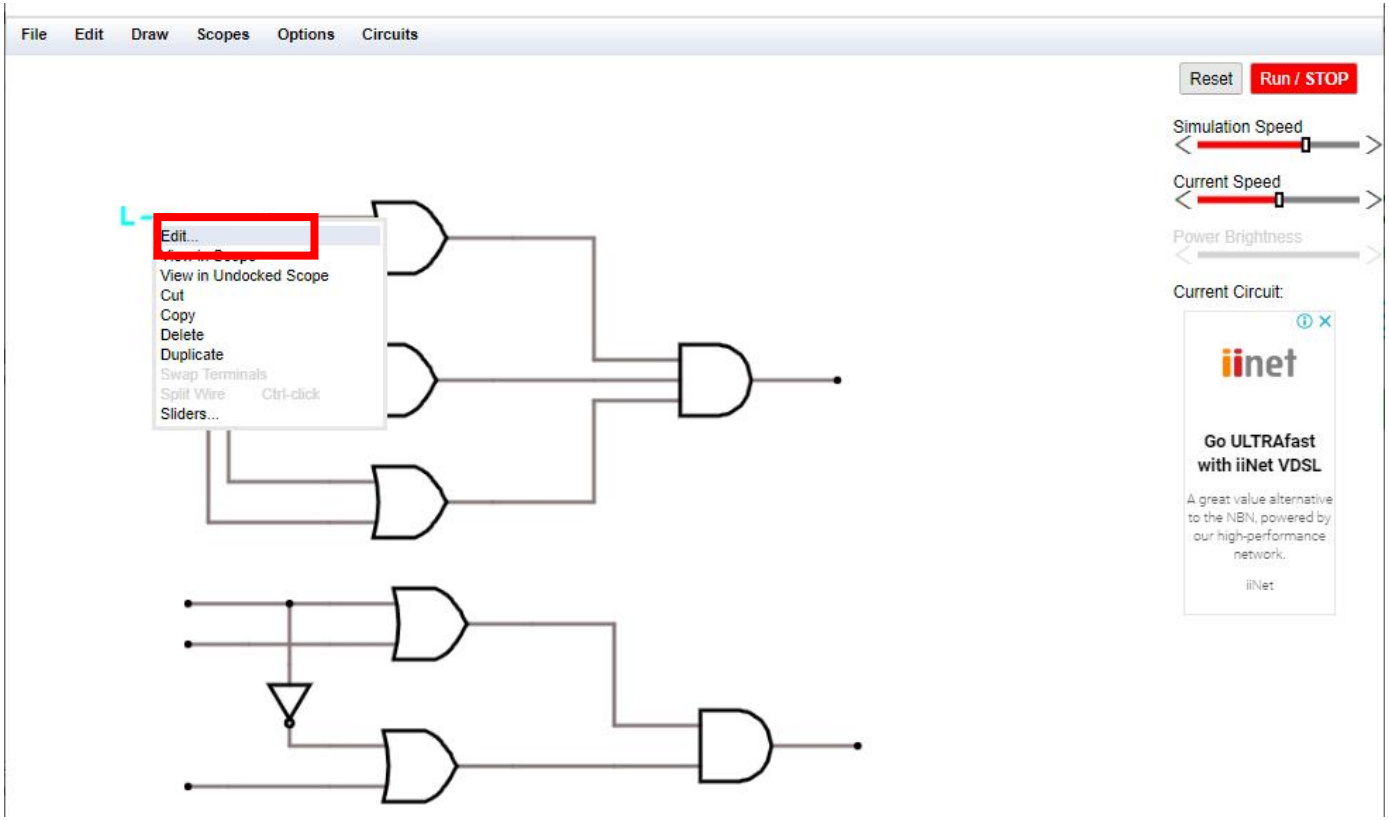

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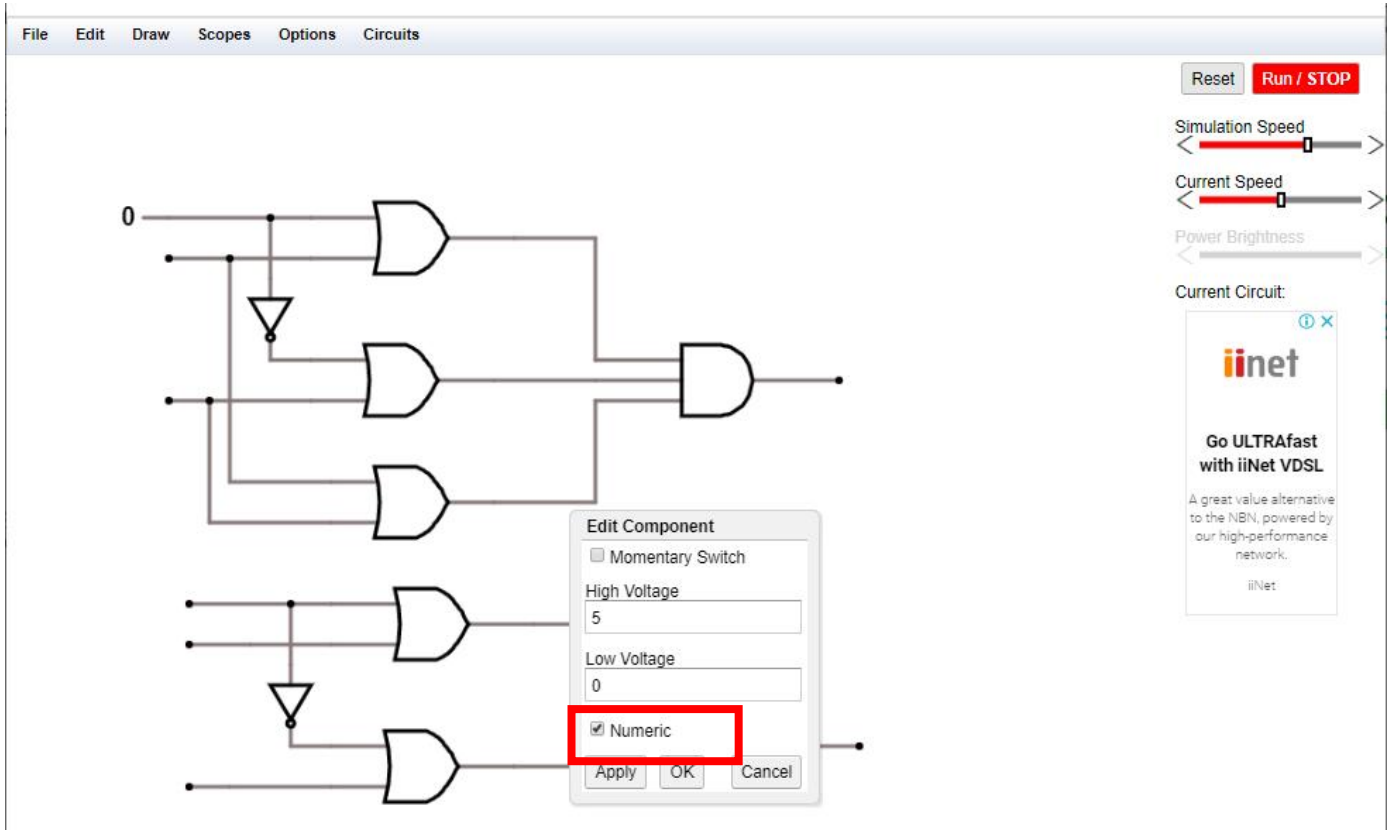

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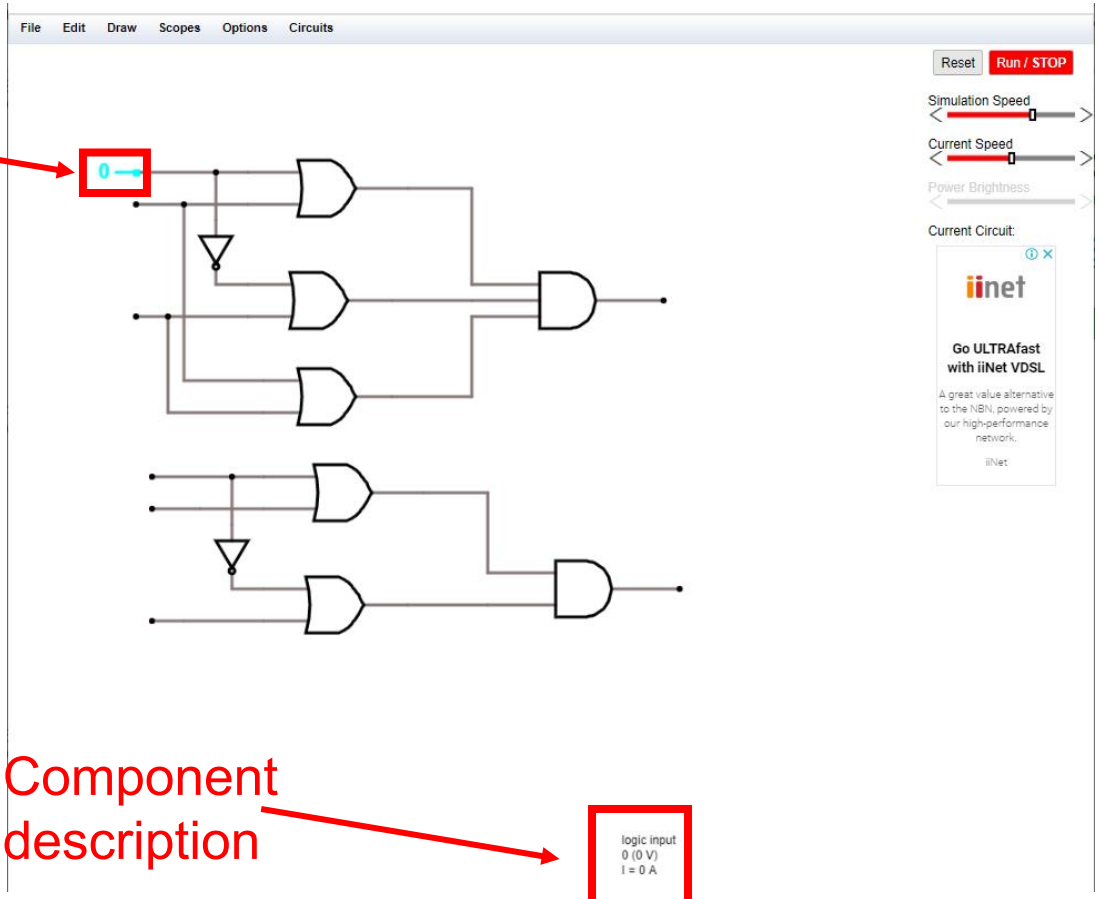
Click on component



Component description

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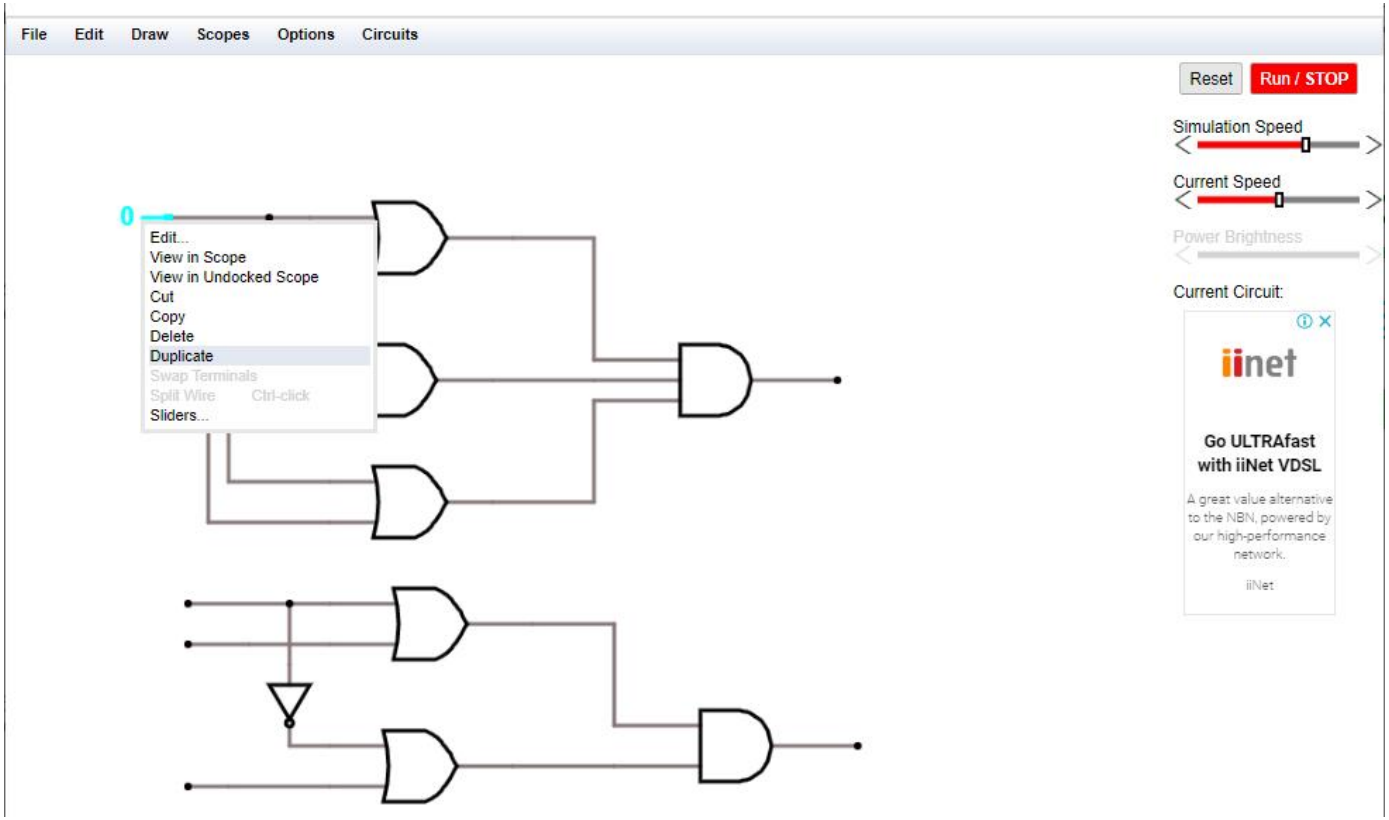

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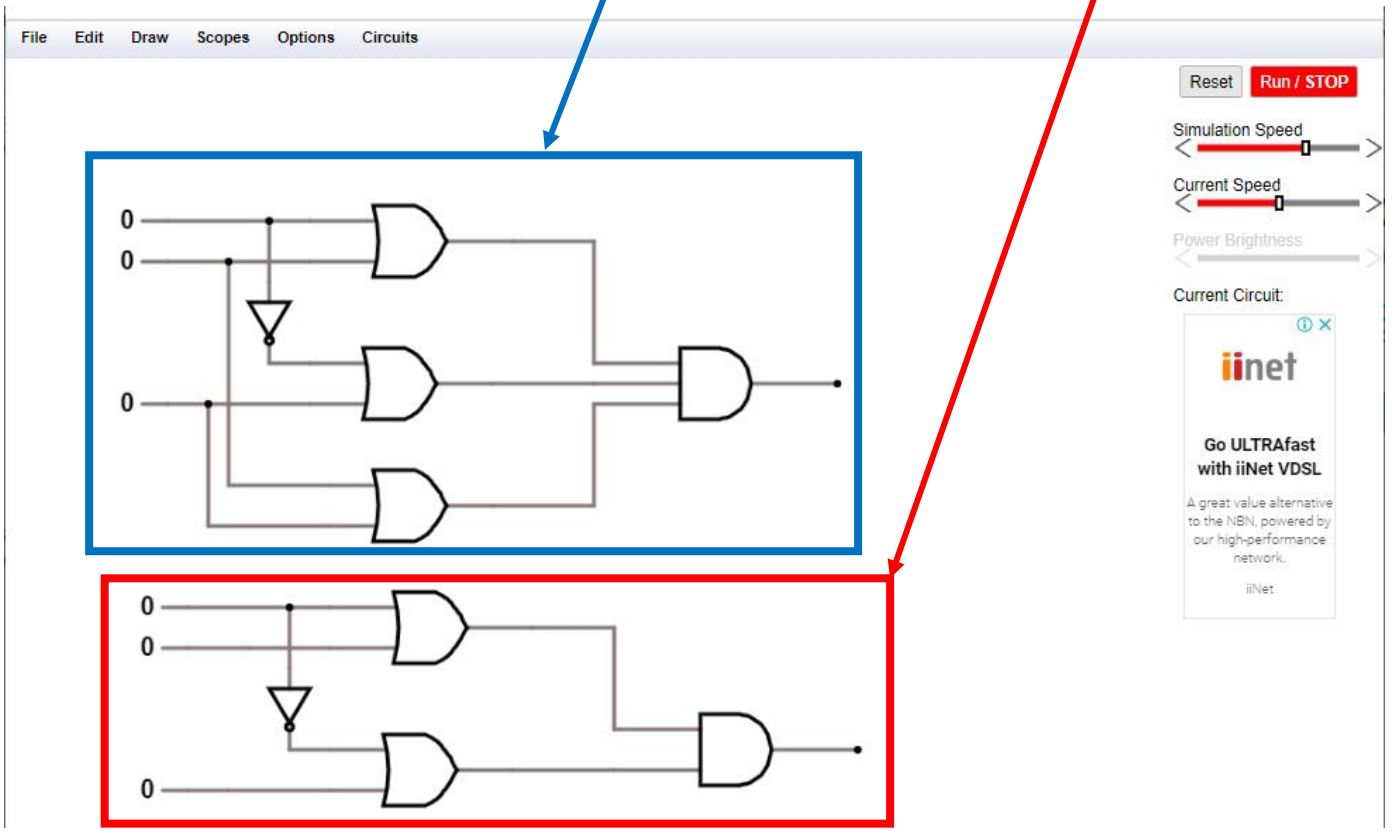

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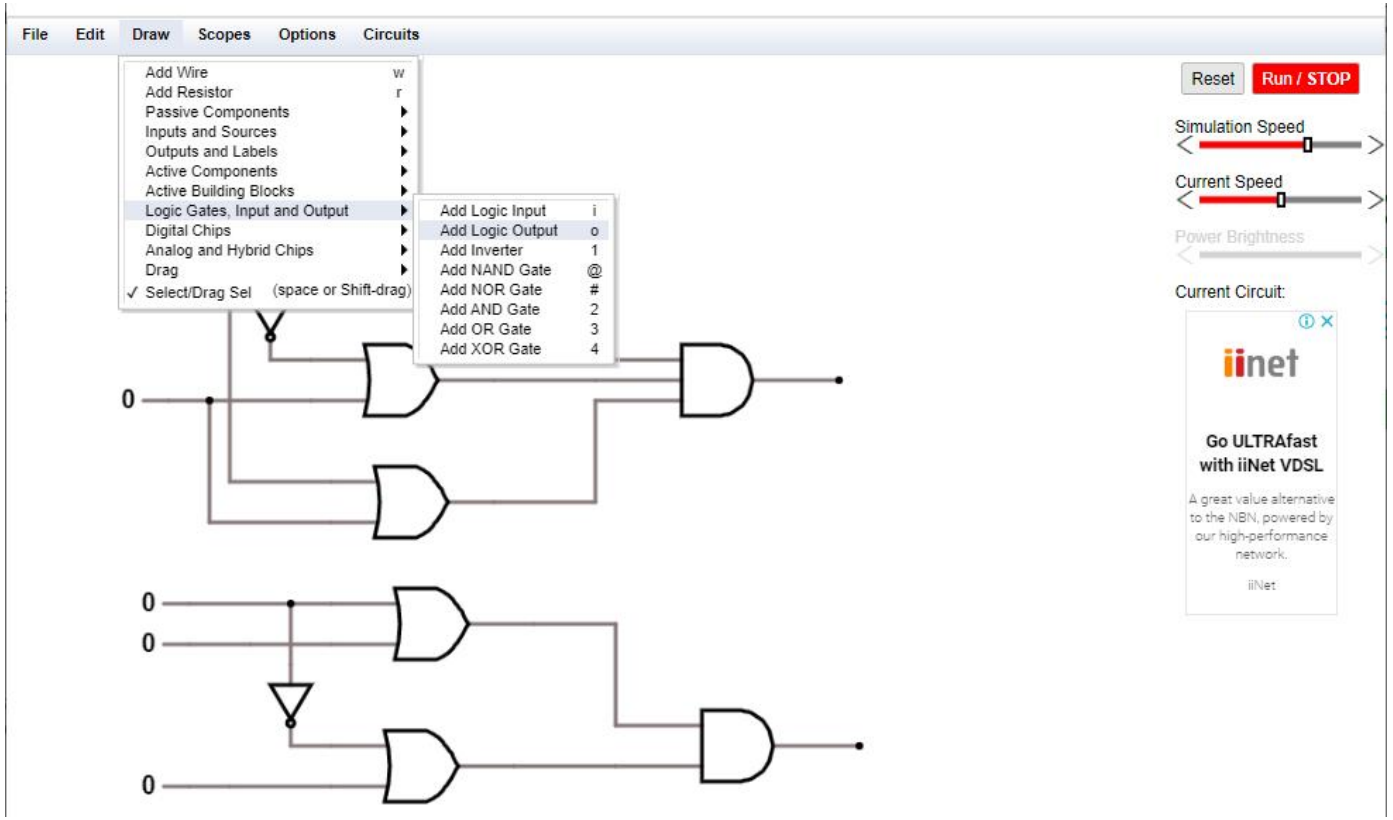

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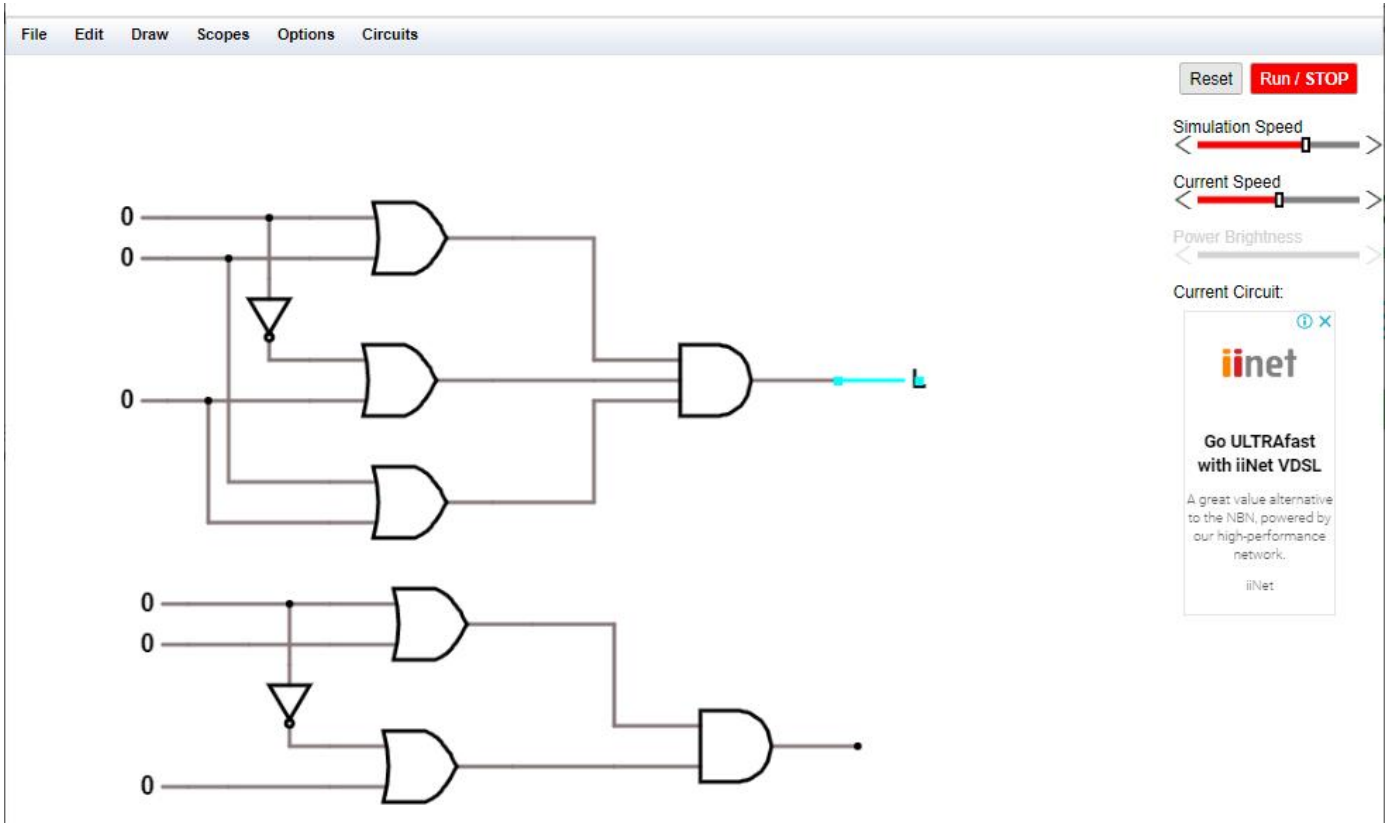

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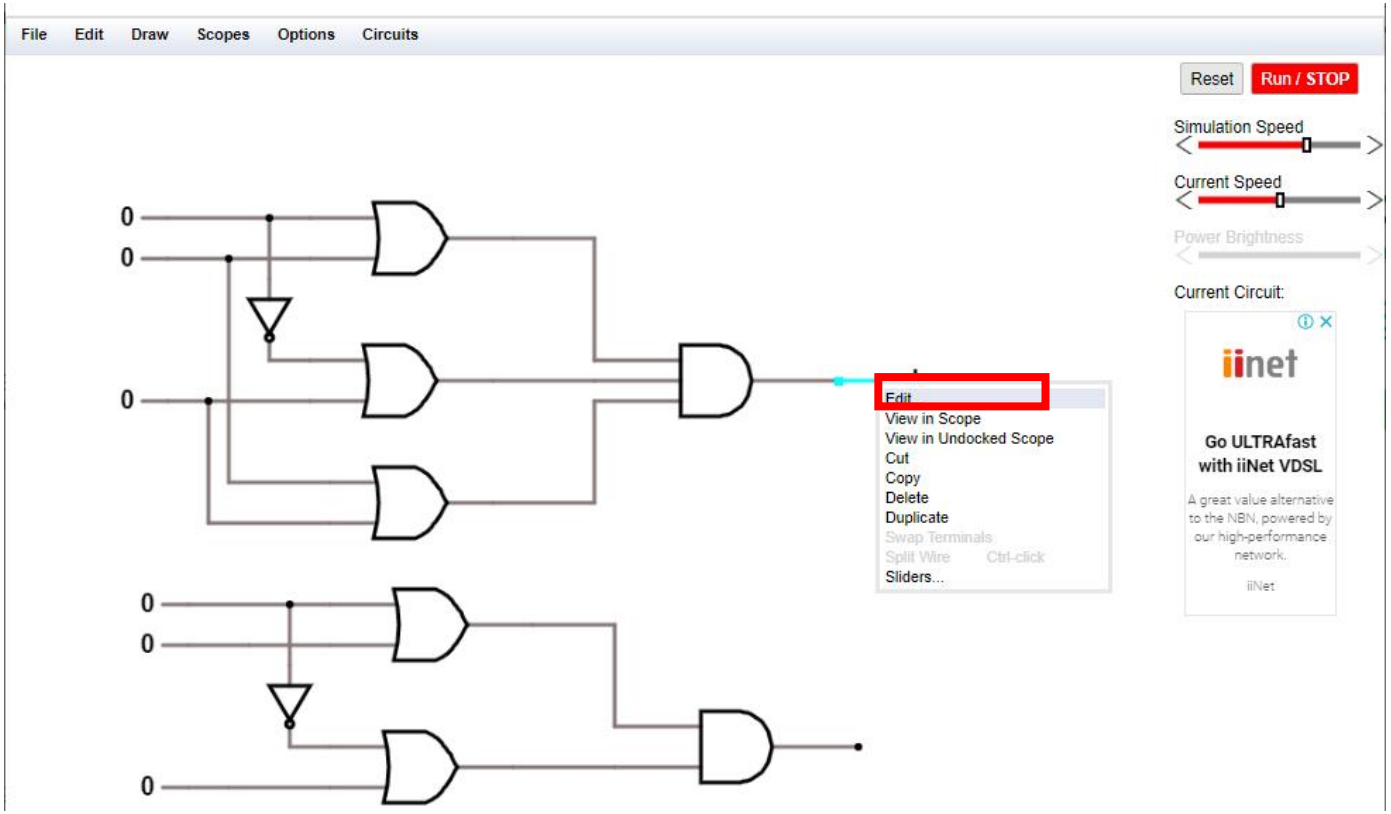

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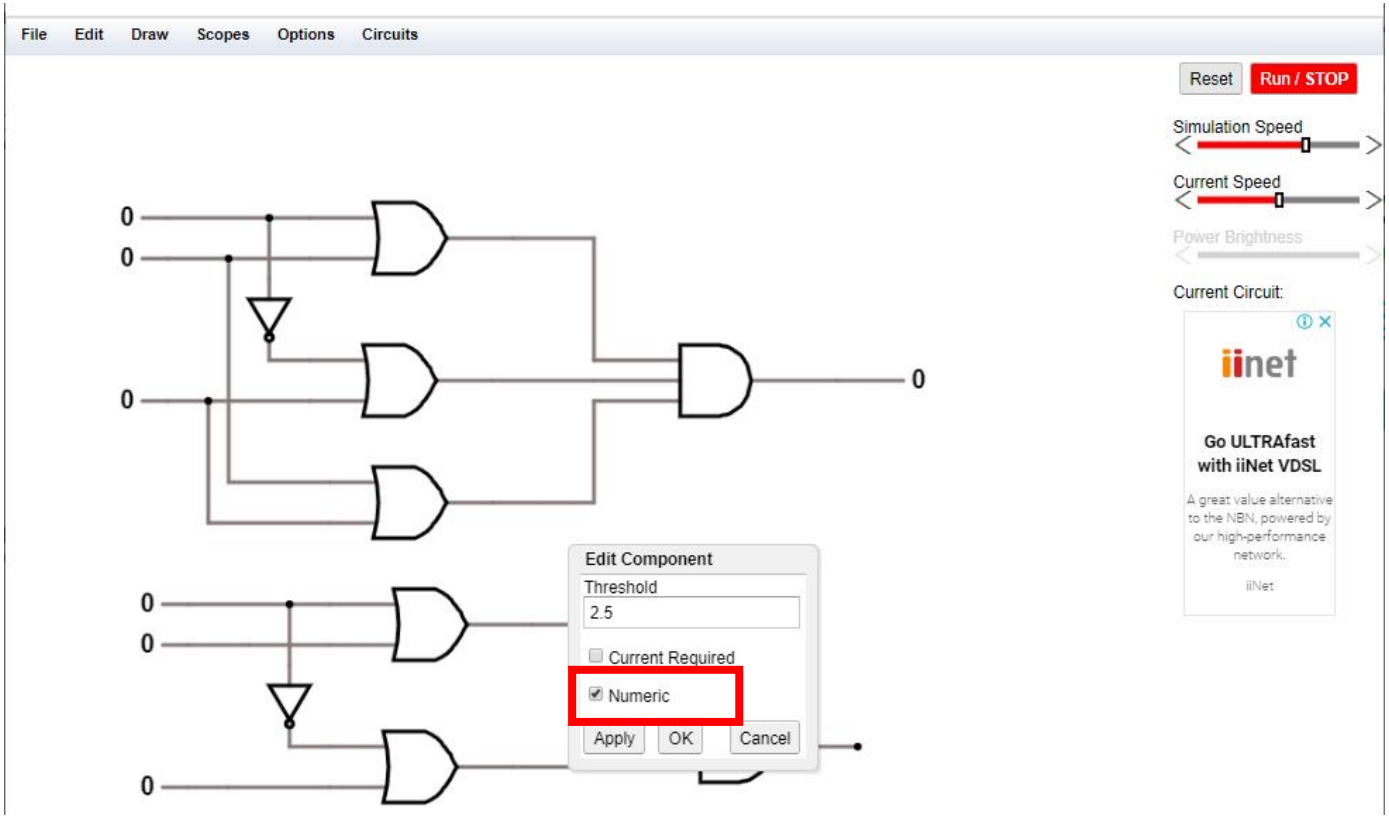

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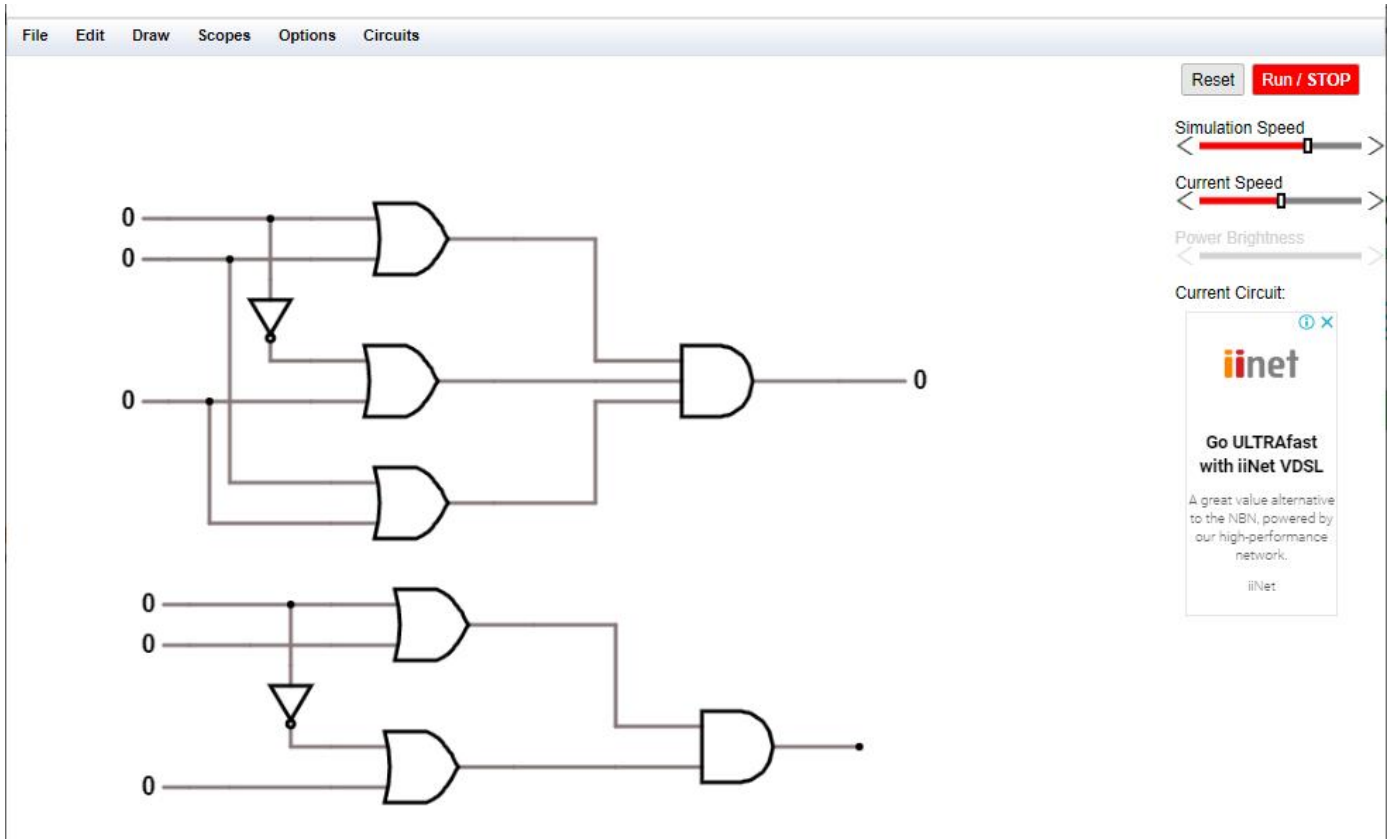

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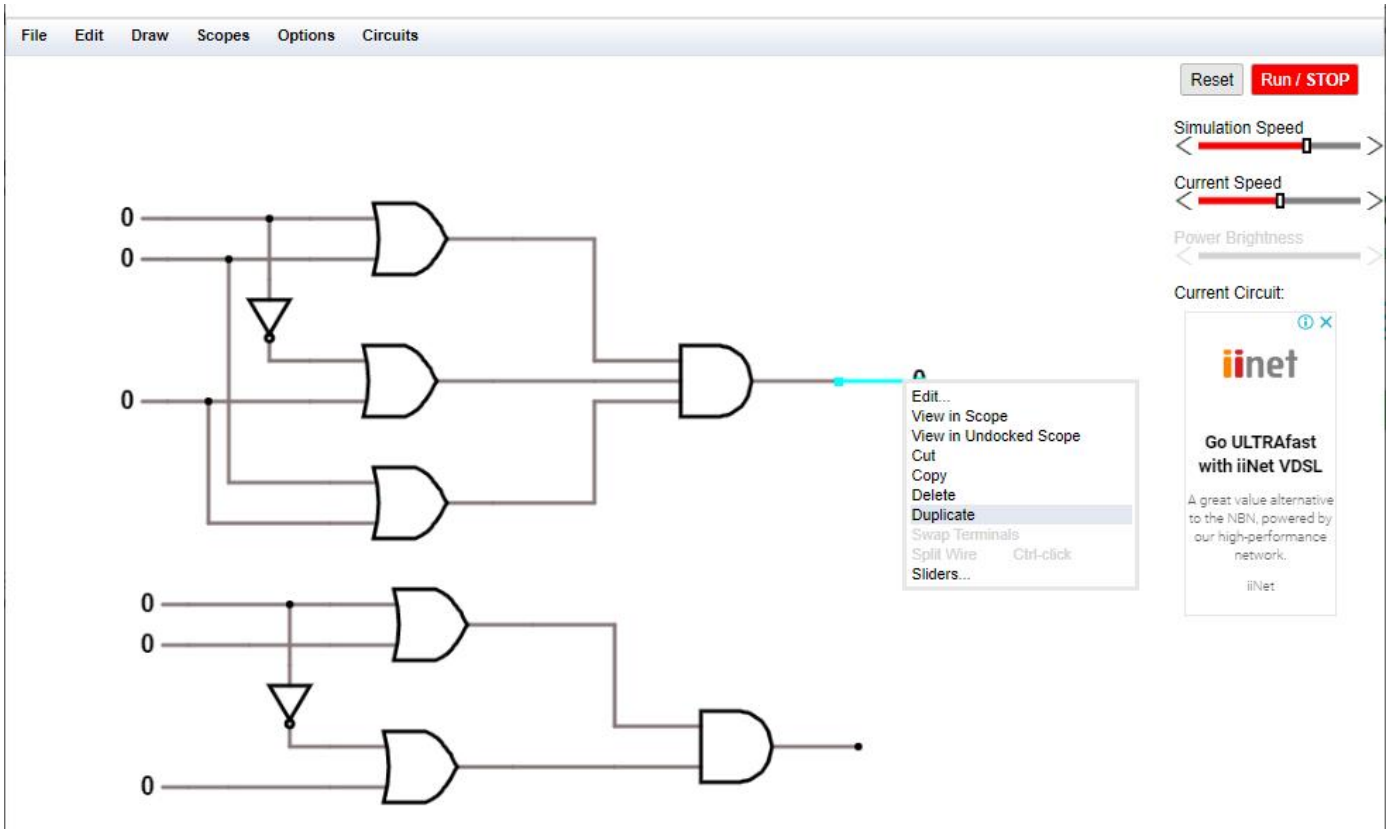

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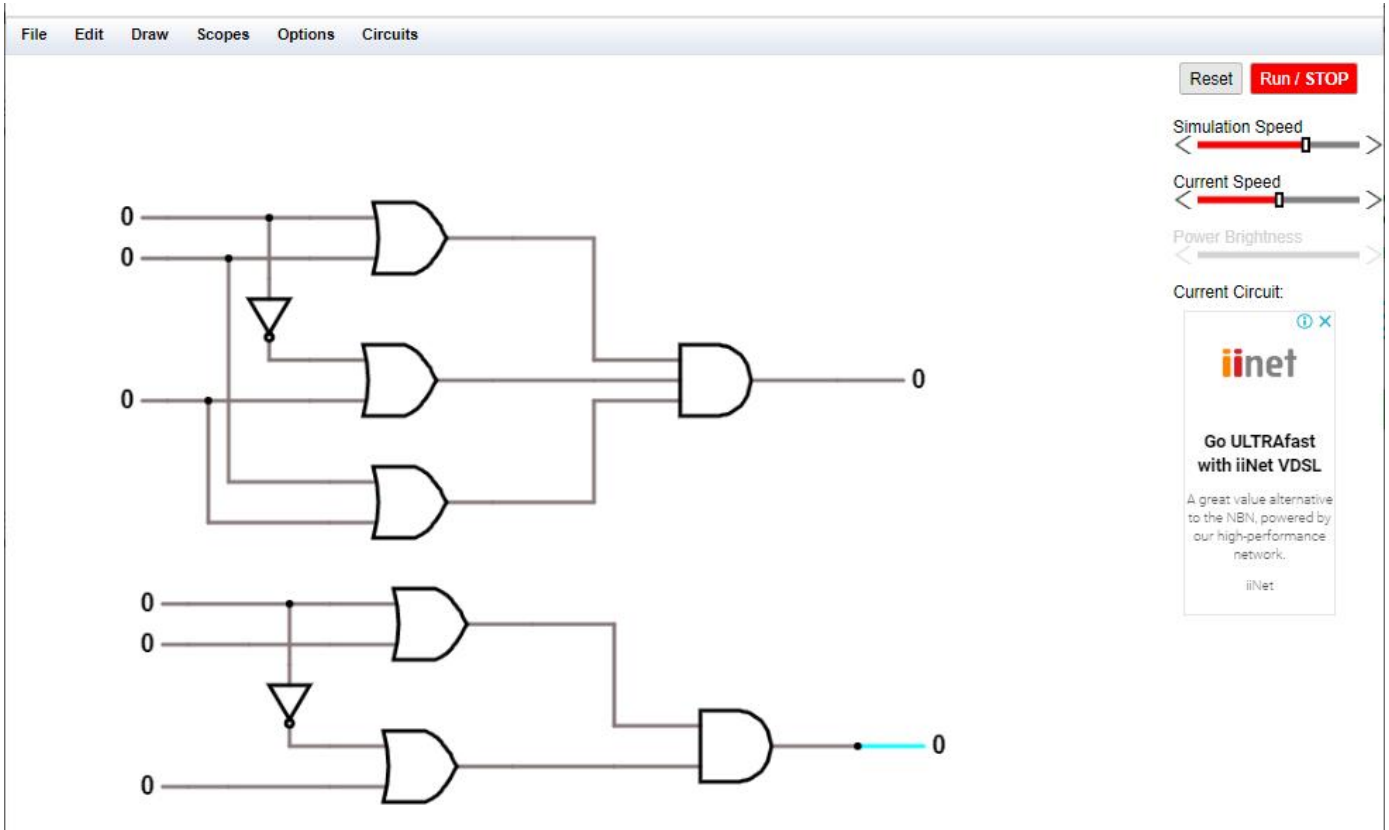

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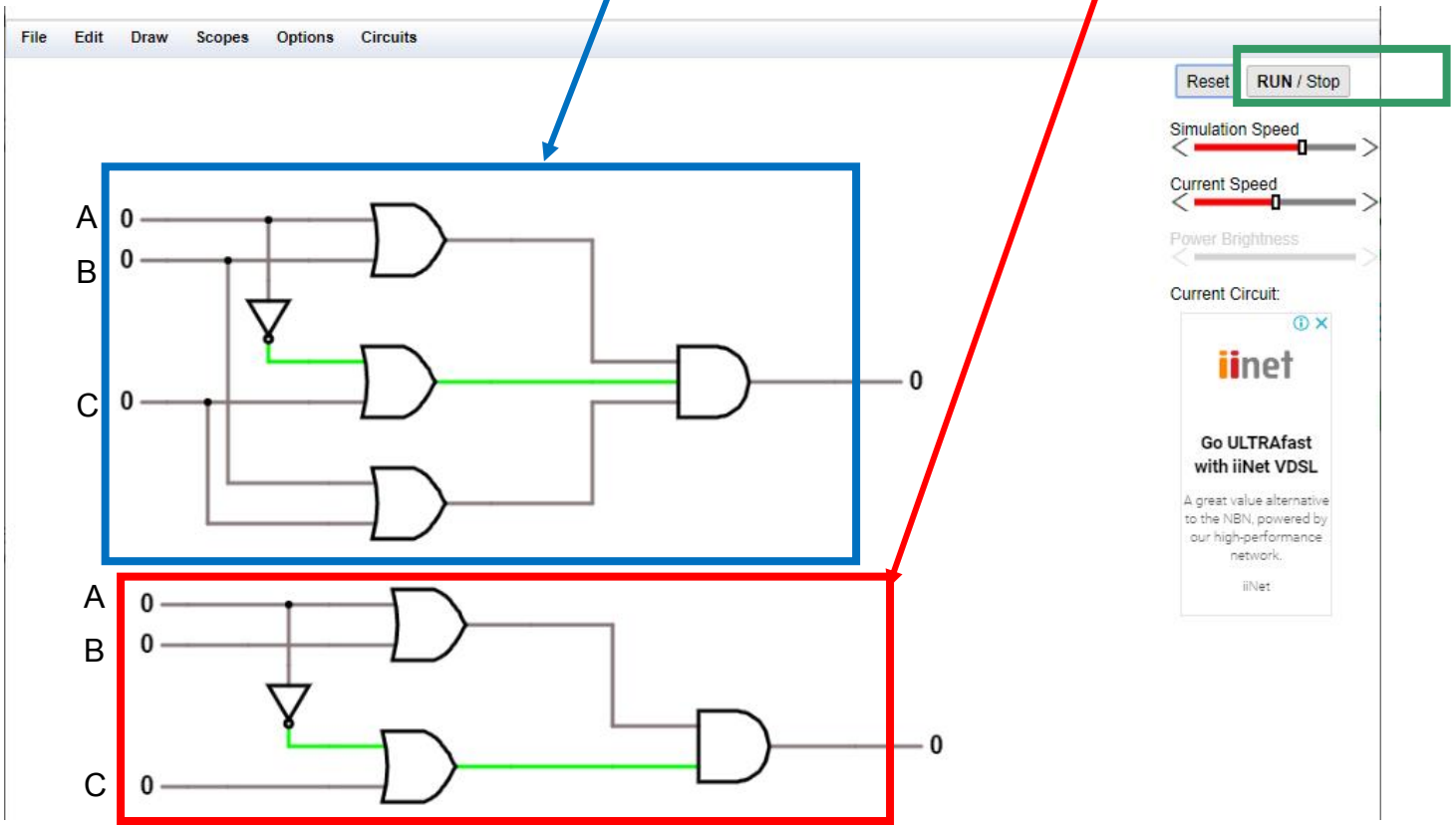

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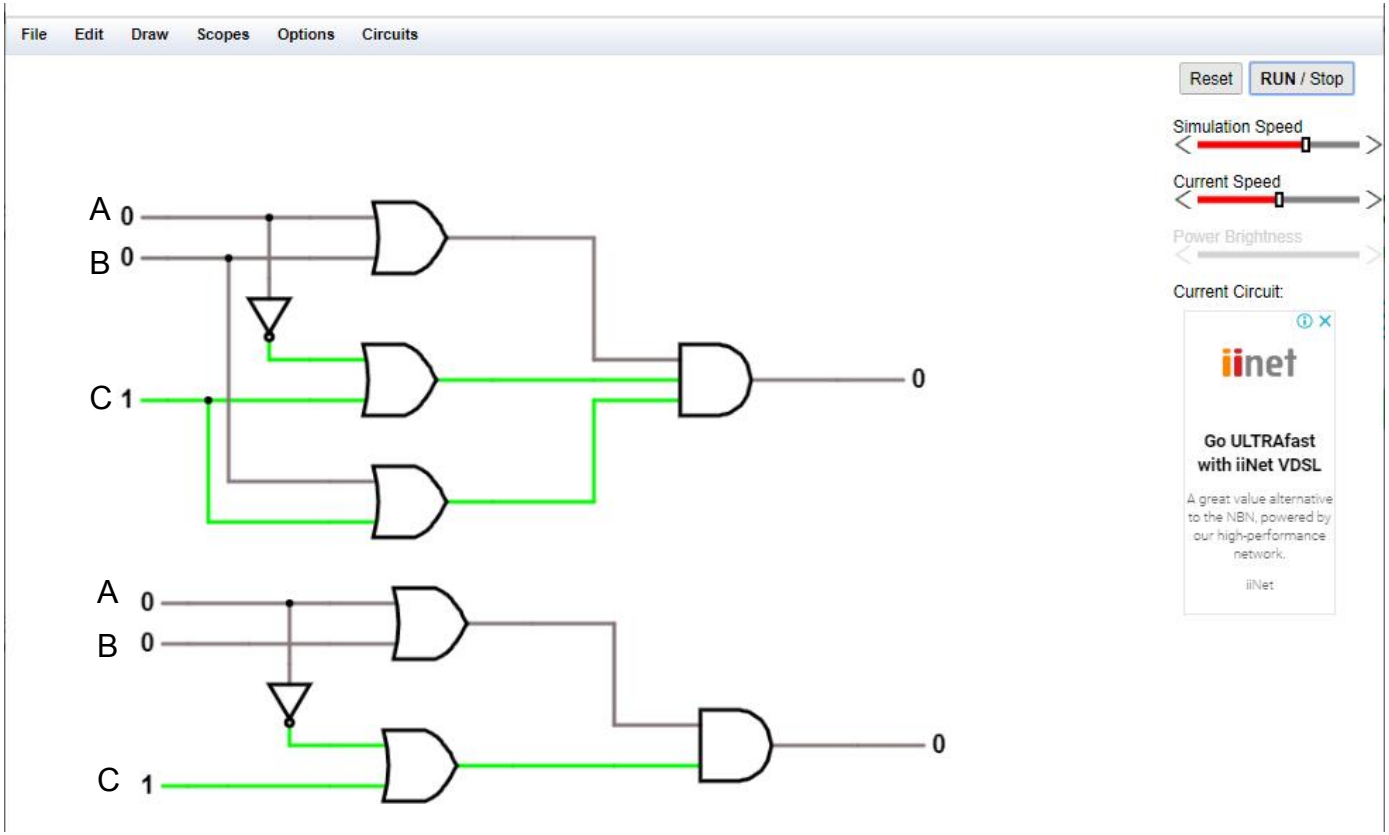
Exercise 6.1 (d): $(A+B)(\bar{A}+C)(B+C) = (A+B)(\bar{A}+C)$

$(A+B)(A'+C)(B+C) = (A+B)(A'+C)$



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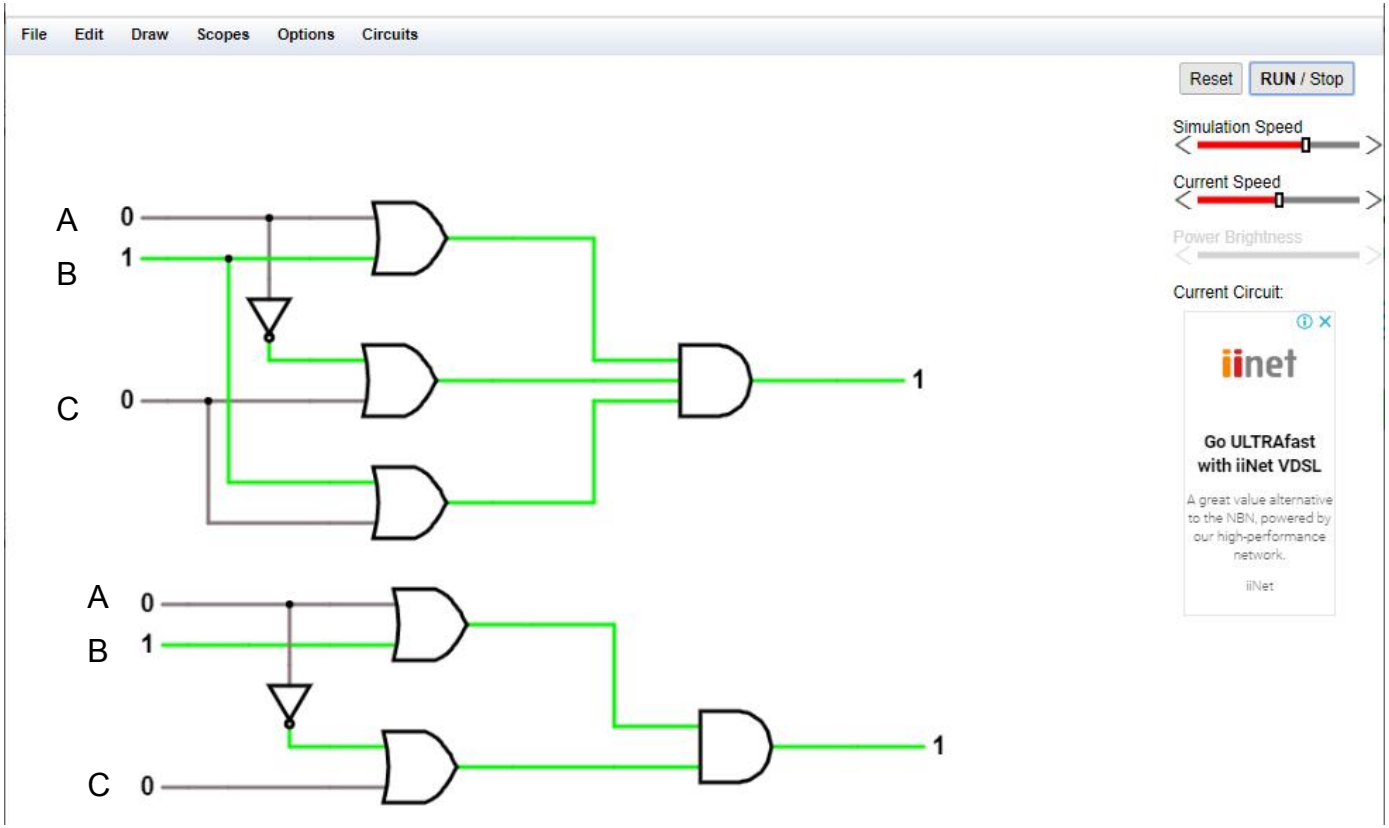

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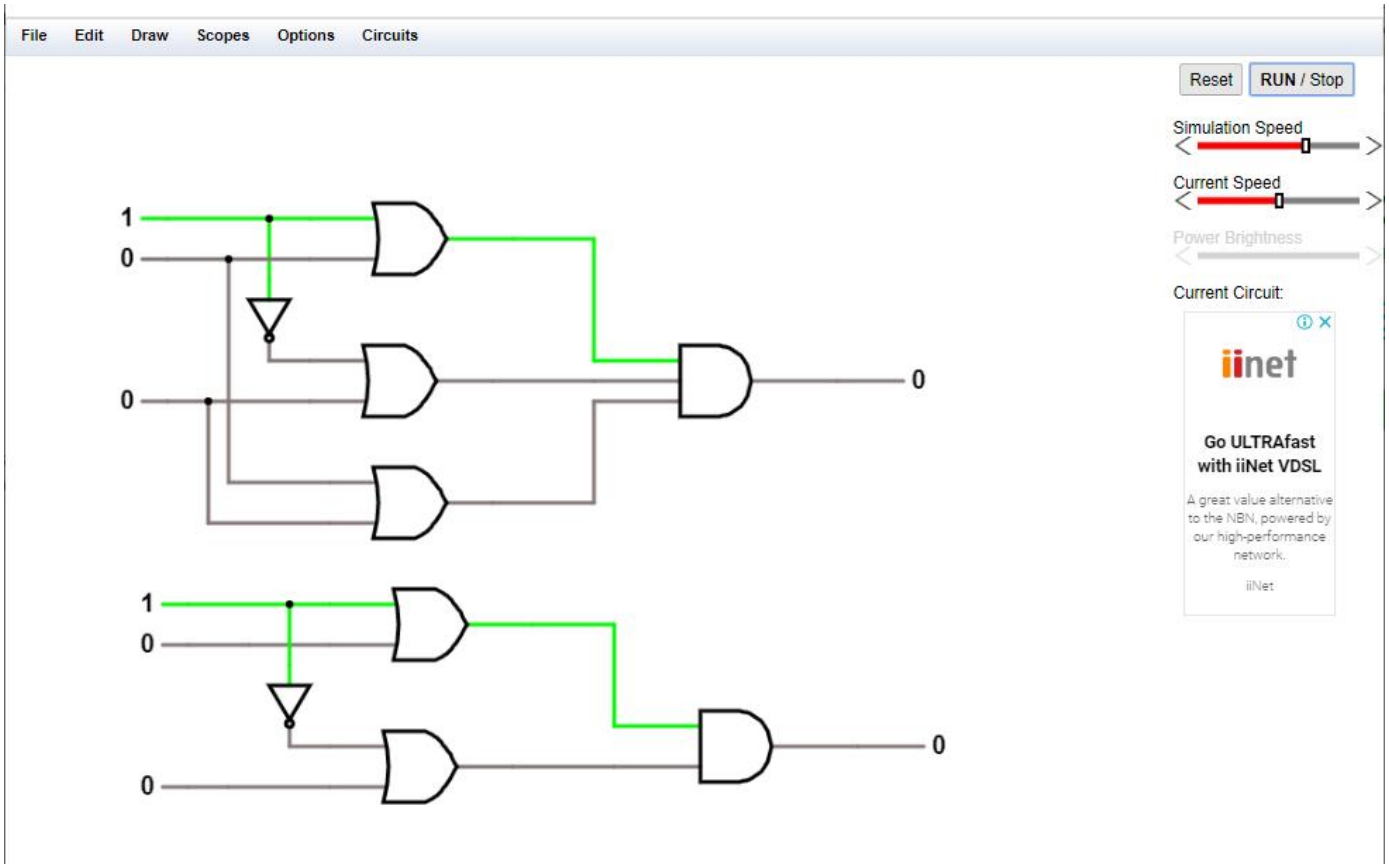

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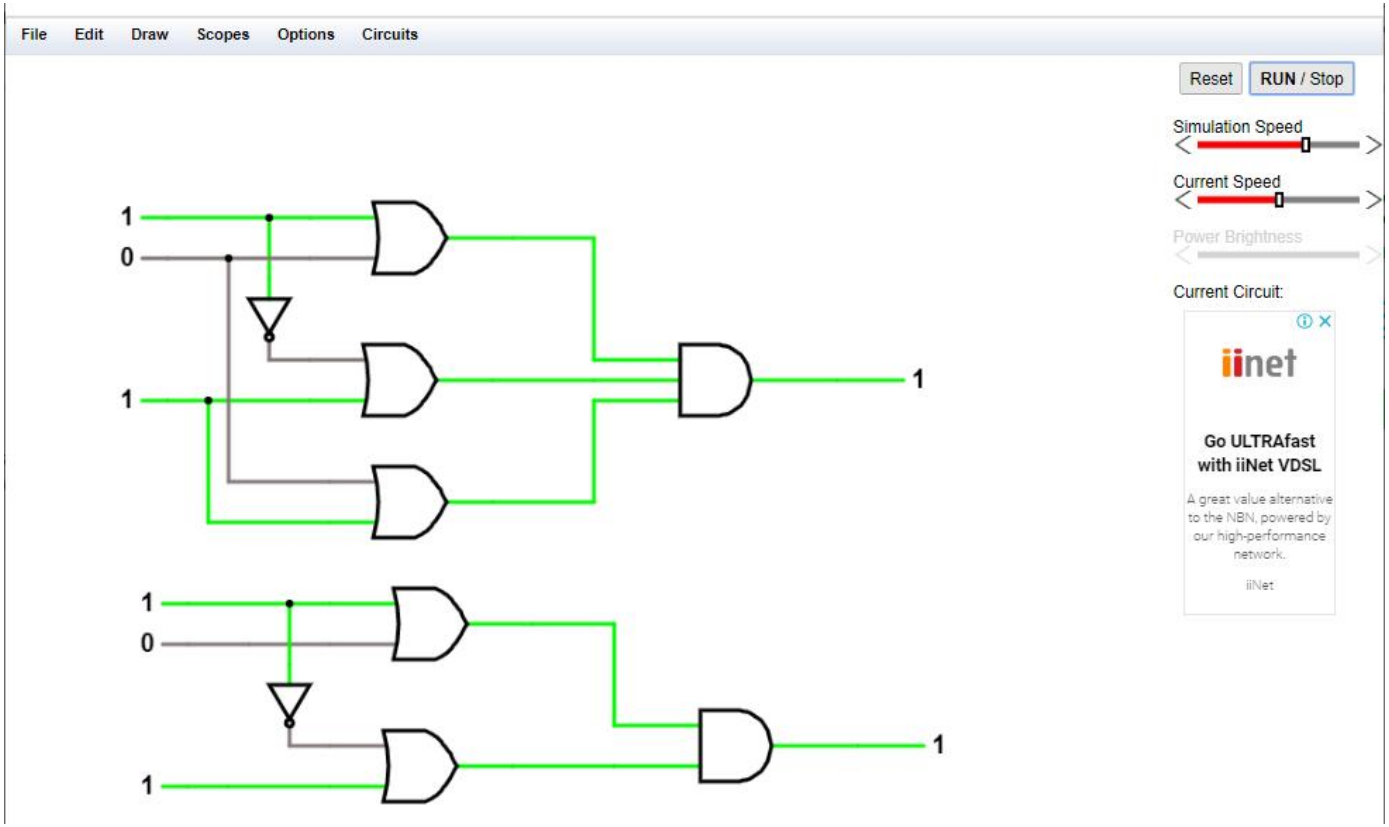

Exercises: Simulator

- C+(BC)’
- (AB)’(A’+B)(B’+B) = ? = A’
- AB+A’C+BC = ? = AB+A’
- 3 bit Even Parity Generator Circuit