ID Number: ……...…….

Full Name: ……..……..….

ECEN202

DIGITAL ELECTRONICS

Final Exam (22 June, 2021)

Time allowed: 2 hours

CLOSED BOOK

Permitted materials: No programmable calculators are allowed.

No electronic dictionaries are allowed.

Paper foreign to English language dictionaries are allowed.

Instructions: Attempt ALL questions.

There are 5 questions in this exam paper:

Space for working out your solutions is provided at the end of every section.

Question	Topic	Allocated Marks	Obtained Marks	
1	Microcontrollers and the 8051 Instruction Set	20		
2	Assembly Language	20		
3	Memory	20		
4	Counters/Timers	20		
5	Stack	20		
	TOTAL	**100**		

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Question 1 – 8051 Instruction Set **20 marks**

a) Read the four statements given below and determine whether the statement is applicable to either the microcontroller or the microprocessor. (4 marks).

Statement	**Microcontroller / Microprocessor**
It has more than one purpose.	
It cannot be expanded.	
I/O ports are external.	
Fixed ROM and RAM sizes.	

b) Name two common instruction sets that are used in microcontrollers. (2 marks)

c) How is Harvard architecture better than the Von Newmann's architecture? (2 marks)

d) How many internal and external interrupts does the standard 8051 have? (2 marks)

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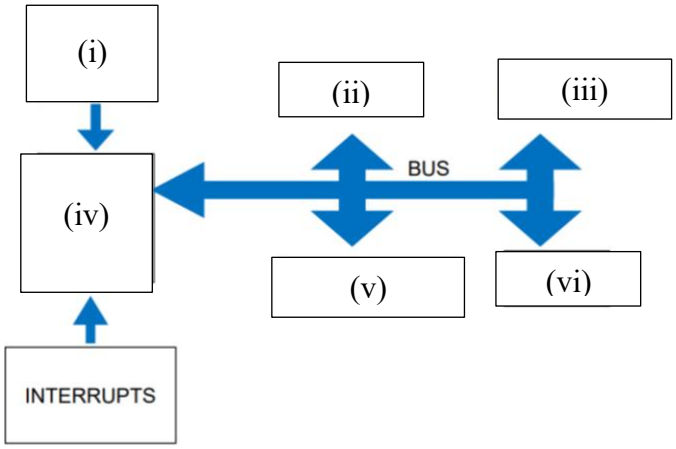
e) Shown below is the block diagram for the microcontroller. Write the name for the 6 blocks in the space provided below the diagram. (6 marks)



(i) _____ (iv) _____

(ii) _____ (v) _____

(iii) _____ (vi) _____

f) Name two examples of embedded systems? (2 marks)

_____

_____

_____

_____

g) If a microcontroller has a 60 MHz crystal, how long will it take for a machine cycle? (2 marks)

_____

_____

_____

_____

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Question 2 – Assembly Language **20 marks**

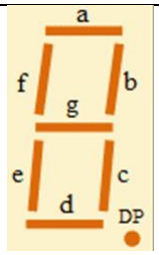

Fig 2.1 7-segment LED

Fig 2.3 Digit 3 is shown at display 1

```
show3:
   CLR P3.4        ; |
   SETB P3.3       ; | enable display 1
   MOV P1, #1Ø11ØØØØB  ; put pattern for 3 on display
   RET

delay:
     MOV RØ, #2ØØ
     DJNZ RØ, $
     RET
```

Fig 2.2 Assembly Language code

Fig 2.4 Digit 2 is shown at display 2

a) The Assembly Language (AL) code shown in Fig 2.2 will produce the output shown in Figure 2.3 when using the EdSim51 simulator. Write an AL program that will use a loop to first show the output shown in Fig 2.4, followed by a short delay before showing the output shown in Fig 2.3. Write a subroutine to display the output shown in Fig 2.4. This subroutine must be named **show3** and you must write the AL code in the start section to call the 3 subroutines and to perform the loop. Use the delay and show3 subroutines. (10 marks)

start:

show3:

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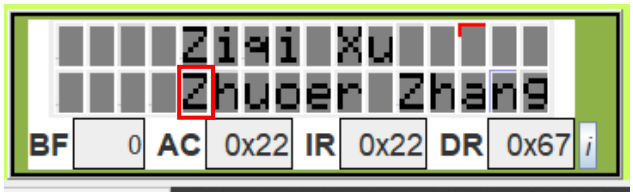
b) For Assignment 2, you were required to use the EdSim51 simulator to produce an output that looked like the one shown below.

Write the lines of Assembly Language code that will display the name Zhoer Zhang to start at the 5th block of the second line (as indicated by the red rectangle in the diagram below). The expected output is shown below. Refer to the Appendices provided to answer this question. Use the next page if you need more writing space.

(10 marks)



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Use this page to answer Question 2 if you need more writing space.

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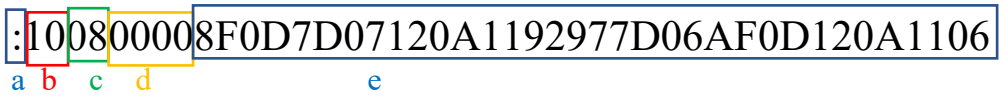
Question 3 – Memory **20 marks**

a) What is the role of data memory? (2 marks)

b) What is the Program Status Word (PSW) and explain the role of the carry flag (CY) and the auxiliary flag (AC) bits? (4 marks)

c) Shown below is a line from a Hex file. Name and explain the purpose of each block (5 marks)



a)

b)

c)

d)

e)

d) Name two electronic components that use the Harvard architecture. (2 marks)

e) How does Harvard architecture overcome the issue of volatile memory? (2 marks)

f) What type of addressing mode is used in the following instruction? MOV A, #02H (1 mark)

g) Write an example for indirect addressing mode (2 marks)

h) Where are the general purpose registers located on the 8051 internal RAM? (2 marks)

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Question 4 – Counters/Timers **20 marks**

a) How many and what type of counters/timers are available on the C8051F020 microcontroller? (2 marks)

b) What is the smallest and the largest number that a 16-bit counter will count? (2 marks)

c) Draw the block diagram of the TMOD indicating the location of the **M0** on **Timer 1** and the M1 bit for Timer 0. (2 marks)

d) Write the Assembly Language code to start Timer 1? (1 mark)

e) Write the Assembly Language code to clear the overflow flag? (1 mark)

f) Calculate the delay generated by Timer 0 in the following Assembly Language program. (12 marks)

EdSim51DI - Source Code Pane - close this window to lock source code in main window

```
    MOV TMOD, #Ø2H ; Choose Timer Ø Mode 1 (8-bit auto-reload timer)
again: MOV TLØ, #3EH  ; 3EH = 62 decimal
    MOV THØ, #ØB8H  ; B8H = 184 decimal
    SETB TRØ       ;  start Timer Ø

waitForOverflow:
    JNB TFØ, waitForOverflow ; if timer Ø overflow bit is not set,
                             ; repeat this instruction
    CLR TRØ                  ; stop Timer Ø
    CLR TFØ                  ;reset timer Ø overflow bit
    JMP again
```

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Question 5 – Stack **20 marks**

a) What is the initial value for the Stack Pointer (SP)? (1 mark).

b) How is stack accessed? (2 marks)

c) What is the size of stack in bits? (1 mark)

d) What is an issue that exists with Bank 1 and stack? (2 marks)

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a) Explain what the following lines of Assembly Language code will do? (2 marks).

```
SETB ETØ
SETB EA
```

```
MOV SP, #24H
MOV R2, #34H
MOV R3, #68H
MOV R1, #16H
PUSH 3
PUSH 1
PUSH 2
```

b) Write the value of SP and the after each PUSH statement. Use the table below to answer this question. (6 marks)

	Initial Memory Location	**Initial Values**	**After PUSH 3**		**After PUSH 1**		**After PUSH 2**	
			Memory	Value	Memory	Value	Memory	Value
	03	68H						
	02	34H						
	01	16H						
SP		24						

c) Following on from question 5, part e (above), what will the contents of stack after each POP instruction? (6 marks)

POP 2
POP 1
POP 3

	Memory Location	Initial Values	After POP 2	After POP 1	After POP 3
Stack Pointer (SP)					

- THE END -

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Appendix 1 – **HD44780 LCD Module Instruction Set**

Instruction	Code RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description	Execution Time (max) (when f_{cp} or f_{osc} is 270 kHz)
Clear display	0	0	0	0	0	0	0	0	0	1	Clears entire display and sets DDRAM address 0 in address counter.	1.52 ms
Return home	0	0	0	0	0	0	0	0	1	—	Sets DDRAM address 0 in address counter. Also returns display from being shifted to original position. DDRAM contents remain unchanged.	1.52 ms
Entry mode set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies display shift. These operations are performed during data write and read.	37 µs
Display on/off control	0	0	0	0	0	0	1	D	C	B	Sets entire display (D) on/off, cursor on/off (C), and blinking of cursor position character (B).	37 µs
Cursor or display shift	0	0	0	0	0	1	S/C	R/L	—	—	Moves cursor and shifts display without changing DDRAM contents.	37 µs
Function set	0	0	0	0	1	DL	N	F	—	—	Sets interface data length (DL), number of display lines (N), and character font (F).	37 µs
Set CGRAM address	0	0	0	1	ACG	ACG	ACG	ACG	ACG	ACG	Sets CGRAM address. CGRAM data is sent and received after this setting.	37 µs
Set DDRAM address	0	0	1	ADD	ADD	ADD	ADD	ADD	ADD	ADD	Sets DDRAM address. DDRAM data is sent and received after this setting.	37 µs
~~Read busy flag & address~~	0	1	BF	AC	AC	AC	AC	AC	AC	AC	Reads busy flag (BF) indicating internal operation is being performed and reads address counter contents.	~~0 µs~~
Write data to CG or DDRAM	1	0	Write data								Writes data into DDRAM or CGRAM.	37 µs
~~Read data from CG or DDRAM~~	1	1	Read data								~~Reads data from DDRAM or CGRAM.~~	~~37 µs~~

not implemented

RAM

not implemented

I/D = 1: Increment
I/D = 0: Decrement
S = 1: Accompanies display shift
S/C = 1: Display shift
S/C = 0: Cursor move
R/L = 1: Shift to the right
R/L = 0: Shift to the left
DL = 1: 8 bits, DL = 0: 4 bits
N = 1: 2 lines, N = 0: 1 line
F = 1: 5 × 10 dots, F = 0: 5 × 8 dots
BF = 1: Internally operating
BF = 0: Instructions acceptable

DDRAM: Display data RAM
CGRAM: Character generator RAM
ACG: CGRAM address
ADD: DDRAM address (corresponds to cursor address)
AC: Address counter used for both DD and CGRAM addresses

Note: — indicates no effect.

LCD Module Instruction Set

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Appendix 2 – **HD44780 LCD Module** (page 11)

- 2-line display (N = 1) (Figure 4)
  — Case 1: When the number of display characters is less than 40 × 2 lines, the two lines are displayed from the head. Note that the first line end address and the second line start address are not consecutive. For example, when just the HD44780 is used, 8 characters × 2 lines are displayed. See Figure 5.
  When display shift operation is performed, the DDRAM address shifts. See Figure 5.

Display position	1	2	3	4	5		39	40
DDRAM address (hexadecimal)	00	01	02	03	04	· · · · · · · · · · · · · · · · · ·	26	27
	40	41	42	43	44	· · · · · · · · · · · · · · · · · ·	66	67

Figure 4 2-Line Display

Display position	1	2	3	4	5	6	7	8
DDRAM address	00	01	02	03	04	05	06	07
	40	41	42	43	44	45	46	47
For shift left	01	02	03	04	05	06	07	08
	41	42	43	44	45	46	47	48
For shift right	27	00	01	02	03	04	05	06
	67	40	41	42	43	44	45	46

Figure 5 2-Line by 8-Character Display Example