VICTORIA UNIVERSITY OF WELLINGTON
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XMUT204 Electronic Design

Note 1b: Microfabrication of Semiconductor Devices

1. Introduction to Microfabrication of Semiconductor Devices

Design and manufacturing of semiconductor devices are very important to master before analysing their characteristics and designing their relevant applications.

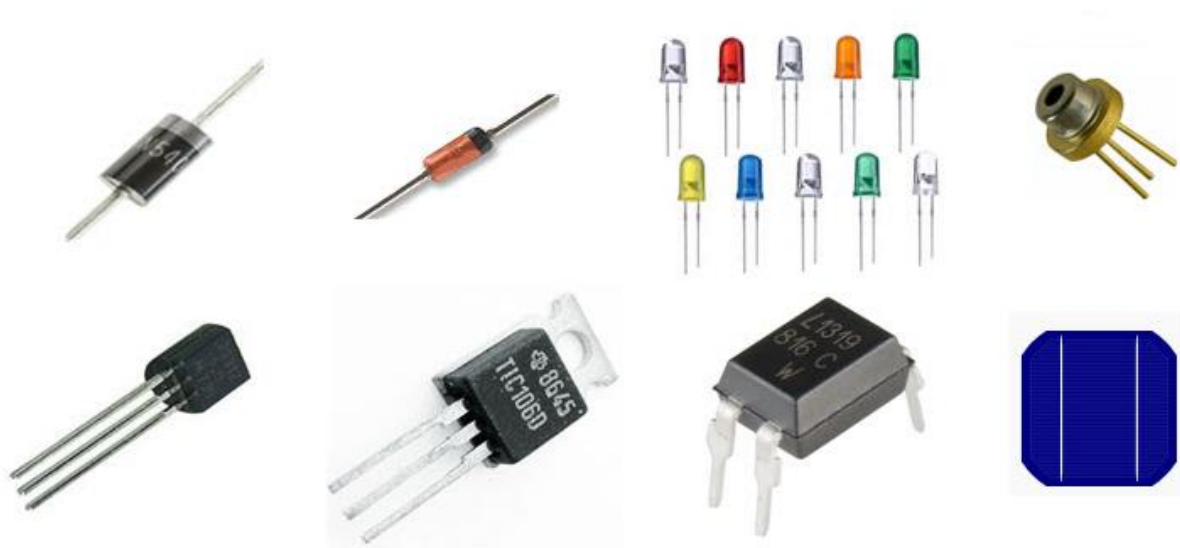


Figure 1: Various types of semiconductor devices

Shown in the diagram are some examples of semiconductor devices i.e. diodes, LED, solar cells, transistors, and integrated circuit (IC).

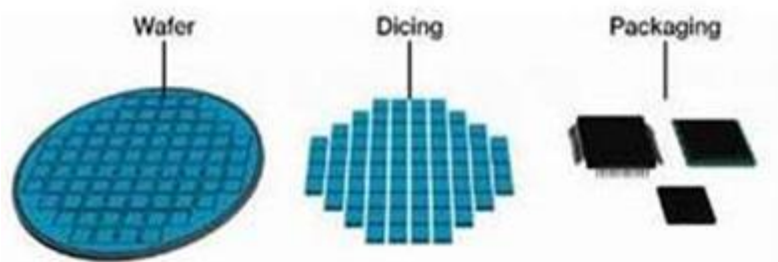


Figure 2: Chips of semiconductor devices

To produce various semiconductor devices as shown above, chips that host the characteristics and functionalities of the device are fabricated using set of chemical and elector-chemical processes typically called microfabrication.

1.1. Microfabrication of Semiconductor Devices

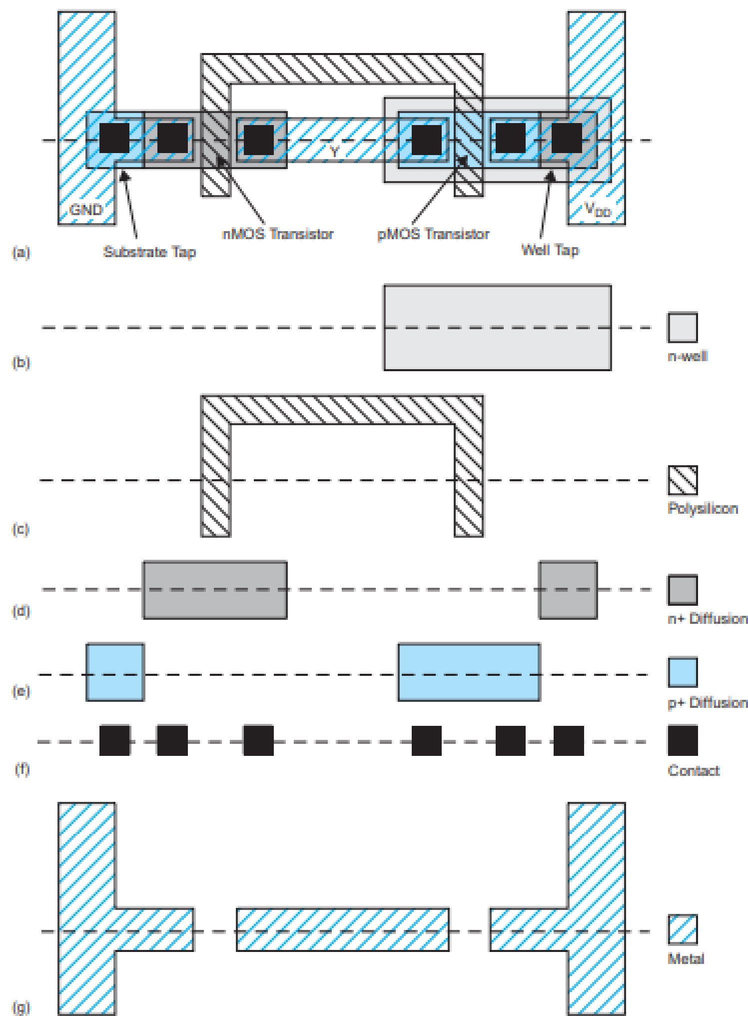


Figure 3: Microfabrication of semiconductor devices

As shown in the diagram given above, the basic steps in microfabrication of semiconductor devices involve the following:

a. Oxidize at high-temperature (typically 900–1200 °C) furnace that causes Si and O2 to react and become SiO2 on the wafer surface.

b. Apply photoresist that allows light to pass through only where the well should be.

c. Remove photoresist with mask.

d. HF acid eats oxide, but not photoresist.

e. Pirana acid eats photoresist.

f. Ion implantation (diffusion, wells of the required dopants).

g. Vapor deposition (to grow polysilicon layer).

h. Plasma etching (metal of contacts and bridges).

1.2. Masking in Manufacturing of Semiconductor Devices

All semiconductor devices are manufactured as a series of very thin, stacked layers on some substrate material (normally silicon dioxide). Each layer is created from a different mask, and different layers can be made of different materials. The masks used to create each layer are basically like a 1-bit bitmap: they have a grid of squares (similar to pixels) that are either "on" or "off".

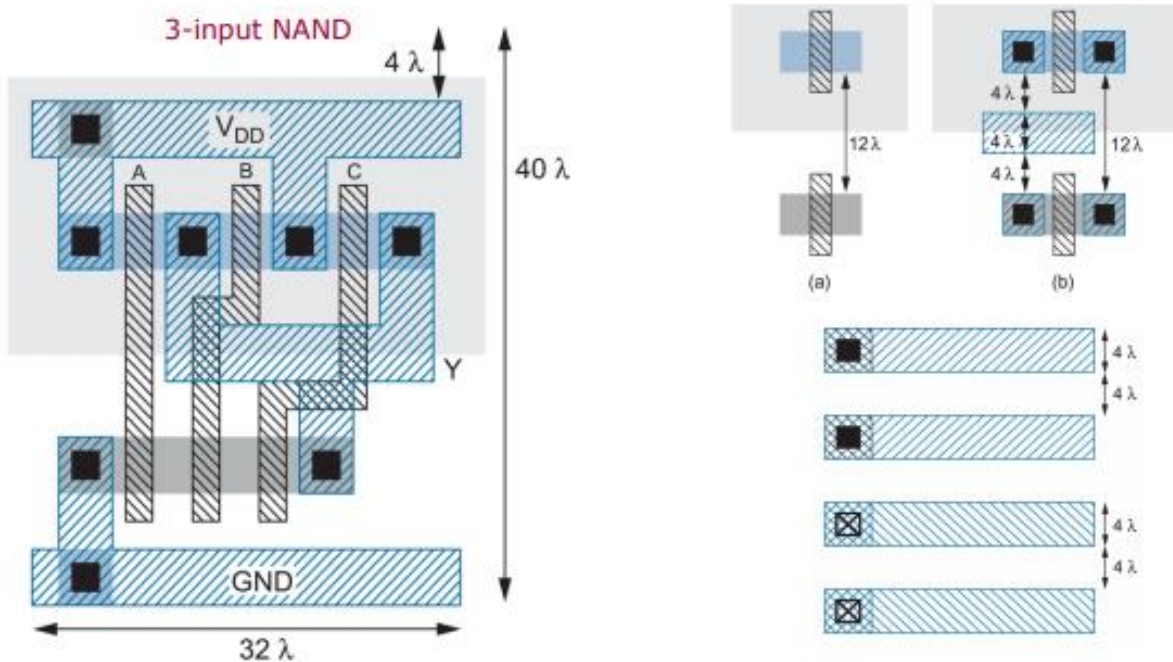


Figure 4: Layout of the mask of semiconductor devices.

The process size defines lambda, which is how large each of those squares will be on the chip. The properties of semiconductor devices, like other electronic devices, are based on the relative sizes of their dimensions. For example, a resistor that is made of a 4 lambda x 20 lambda rectangle will have essentially the same resistance for any value of lambda.

Functionalities, features and characteristics of the semiconductor device are built up from the smaller units on the chip i.e. a simple diode is made up of a unit made of p-n materials and a simple transistor is made up of pnp or npn materials. Larger or more complex functionalities are simply combinations of these smaller units.

As shown in the following diagram, smaller groups of functionalities are combined to make bigger/complex functionalities. As illustrated in the diagram, elements cell libraries i.e. gates, latch, etc. are made from a number of smaller structures.

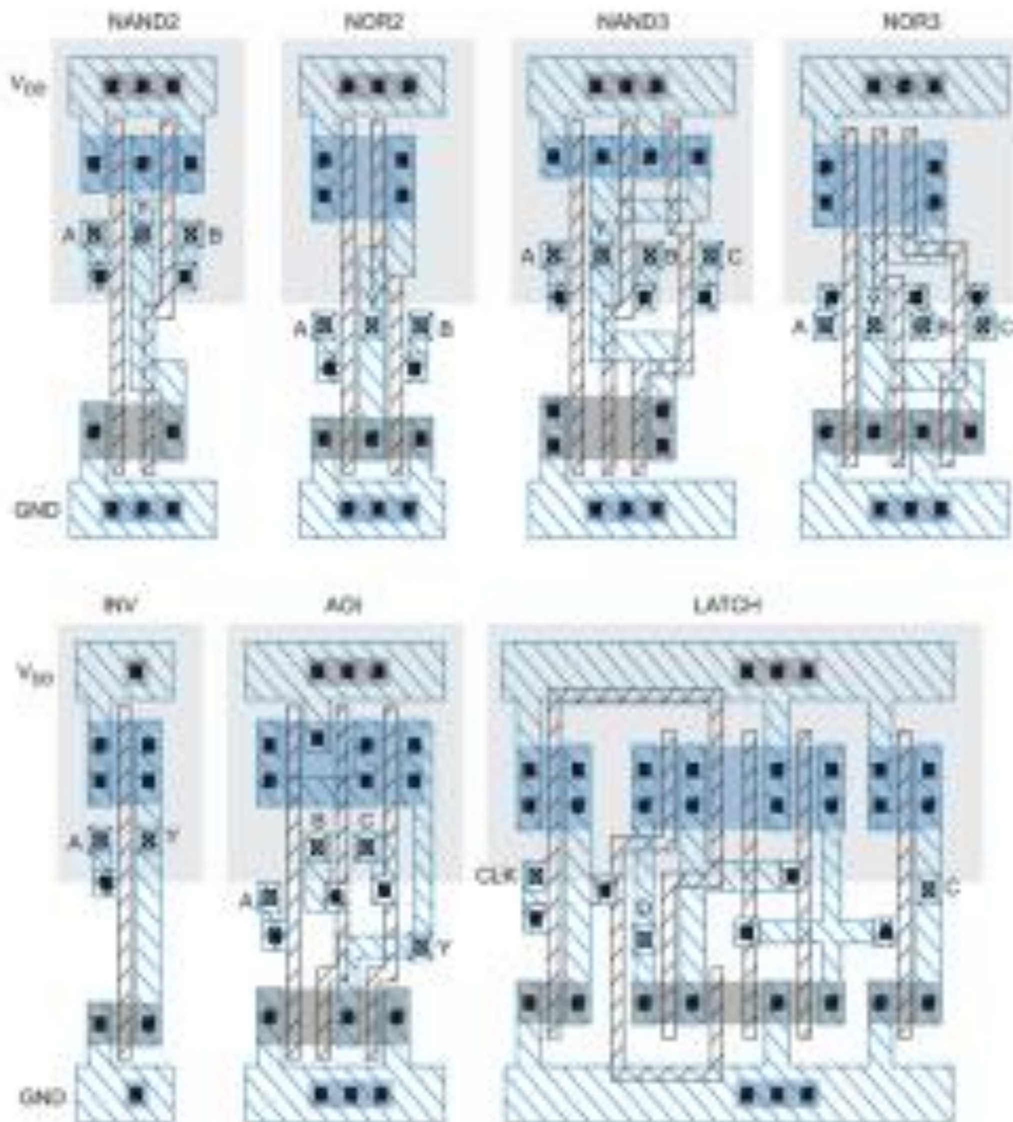


Figure 5: Elements cell libraries (snap together).

At a high-level abstraction, you can assume that each layer has zero thickness. However, layers have non-zero thickness, and their thickness doesn't scale to perfectly match when you change your value of lambda. If you move to a smaller value of lambda (a smaller process node), interesting things can happen. For example, the capacitance of a capacitor is directly proportional to the area of the plates, and inversely proportional to the distance between them. If you divide lambda in half, you divide the area of the plates by four. Unless you also divide the thickness of the layer(s) between the plates by four, you will end up with a capacitor with lower capacitance.

1.3. Trends in Manufacturing of Semiconductor Devices

This is good for making transistors because they have capacitance between their terminals which cuts back on increasing the switching frequency of those transistors. Also, the dynamic power a transistor consumes (when switching) is proportional to capacitance. So smaller transistors scale more easily to higher frequencies, and use less power. Smaller transistors have lower "turn on" voltages, which means they can be driven by lower voltages (core voltages). And dynamic power loss in a transistor is proportional to the square of that voltage; cut the voltage in half, cut power consumption by a factor of four.

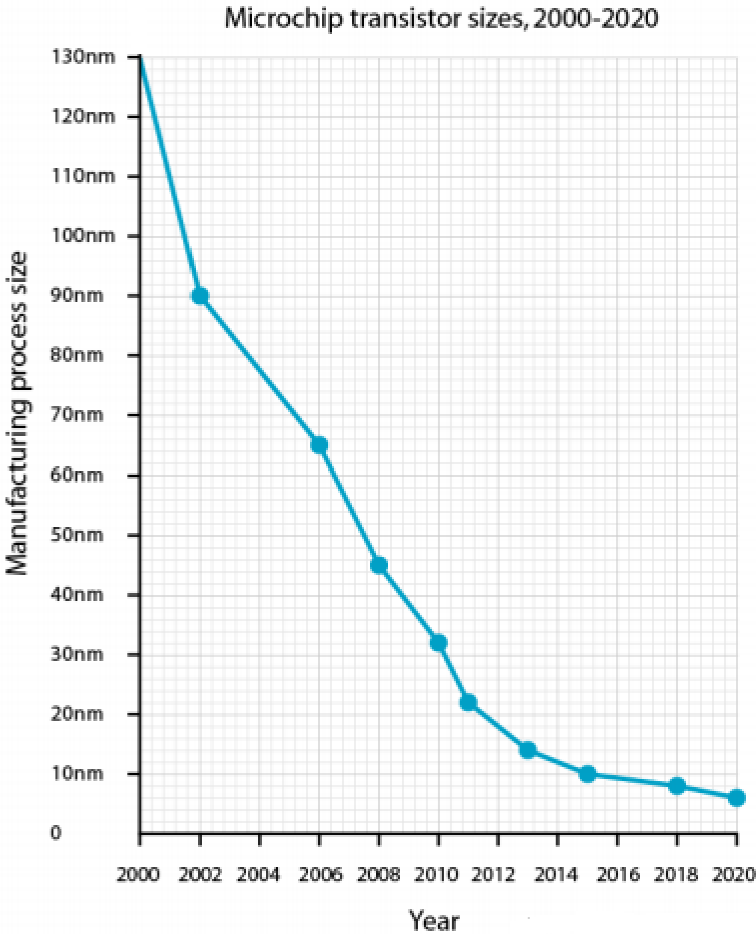


Figure 6: Trend of the sizes of manufacturing process of integrated circuit

The diagram given above gives a trend of the sizes of manufacturing process of integrated circuit. Note that in year 2000, the size of a transistor is 130 nm, but in year 2020, it is less than 10 nm.

2. Materials of Semiconductor Devices

Three types of materials are typically used for microfabrication or manufacturing of semiconductor devices.

Insulators – Materials which block or resist the flow of electric current. An example of an insulator would be Silicon Dioxide (SiO_2) which has a resistivity of 1014 - 1016 ohm-cm.

Conductors – Materials which readily support the flow of electric current. An example of a conductor would be aluminum which has a resistivity of 2.7 x 10-6 ohm-cm.

Semiconductors – A material which can be made to act as an insulator or act as a conductor. An example of a semiconductor would be silicon with an intrinsic resistivity of 2.3 x 105 ohm-cm and where doped silicon can have resistivities down to 1 x 10-4 ohm-cm.

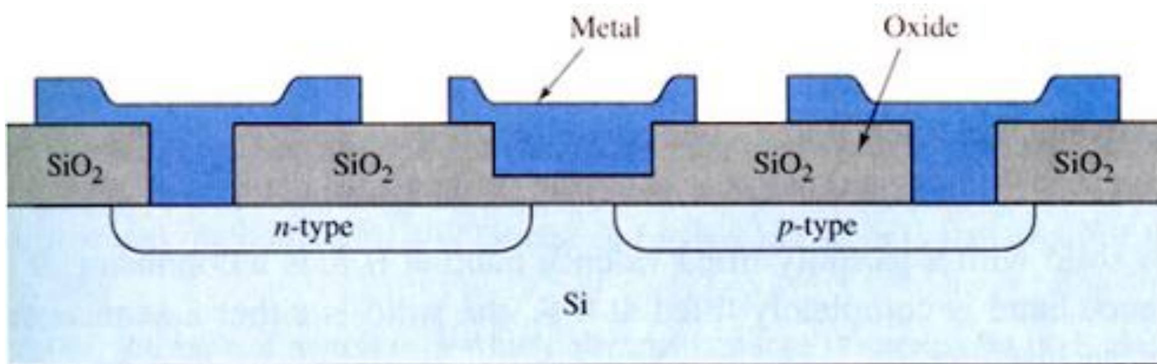


Figure 7: Materials in a typical semiconductor device (CMOS transistor)

Shown in the diagram given above is the materials in a given semiconductor device i.e. CMOS transistor. Note how the following materials are used in the device:

- Metal – Conductor material.
- SiO_2 – Insulator material.
- n-type and p-type doped Si - Active components material.

Insulators:

- Silicon Dioxide (SiO_2) – The most common insulator in Silicon Integrated Circuits. Silicon Dioxide is a good barrier materials with excellent electrical properties.
- Silicon Nitride (Ni_3N_4) – Frequently used as a barrier or final passivation layer for Silicon Integrated Circuits. Silicon Nitride is an excellent barrier, although Silicon Nitride exhibits too much stress to be in direct contact with Silicon.

Conductor:

- Aluminum – Most frequently used conductor for Silicon Integrated Circuits.
- Titanium, Cobalt, Nickel and Platinum – Metals commonly used to form silicide contacts to Silicon.
- Tungsten – Used for plug filling.
- Titanium Nitride – Used as a barrier layer to prevent metal from interacting or to prevent metals and silicon from interacting.
- Copper – Now used as a conductor.

Active Components:

- These are such as diodes and transistors can be used to control the direction of current flow.
- PN junction diodes are formed when there is a region of n-type semiconductor adjacent to a region of p-type semiconductor.
- A difference in charge at the PN junction creates a depletion region that results in a barrier voltage that must be overcome before a diode can be operated.
- A bias voltage can be configured to have a reverse bias, with little or no conduction through the diode, or with a forward bias, which permits current flow.

3. Types of Semiconductor Devices

In this section, we will have a look at the structures and characteristics of some of the available semiconductor devices in the market e.g. diodes, BJT, MOSFET and CMOS.

3.1. Diodes

As given below, a simple diode is formed when a p-type semiconductor material is integrated with a lightly doped n- type semiconductor material. We will see the characteristics and operation of this device in the subsequent topics in this course.

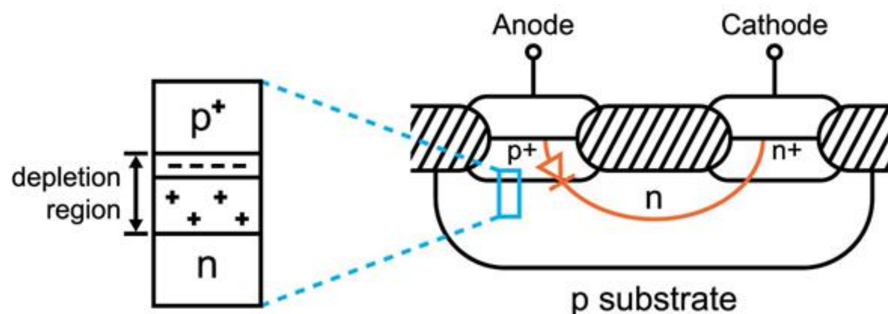


Figure 8: Semiconductor structure of a diode

On the other hand a type of high-speed diode i.e. Schottky diode is formed when metal is brought in contact with a lightly doped n- type semiconductor material. This diode is used in faster and more power efficient analogue electronic circuits. As shown in the diagram given below Al or PT is the metal material used in the structure.

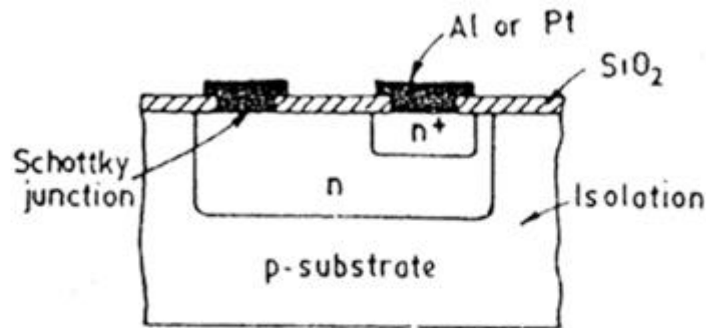


Figure 9: Semiconductor structure of a Schottky diode

3.2. BJT

As illustrated in the following figure, transistors like the bipolar junction transistor (BJT) has three electrodes and two PN junctions. A BJT is configured as an NPN or PNP transistor and biased for conduction mode. It is a current amplifying device, and just like diodes, we will study its characteristics and operation later.

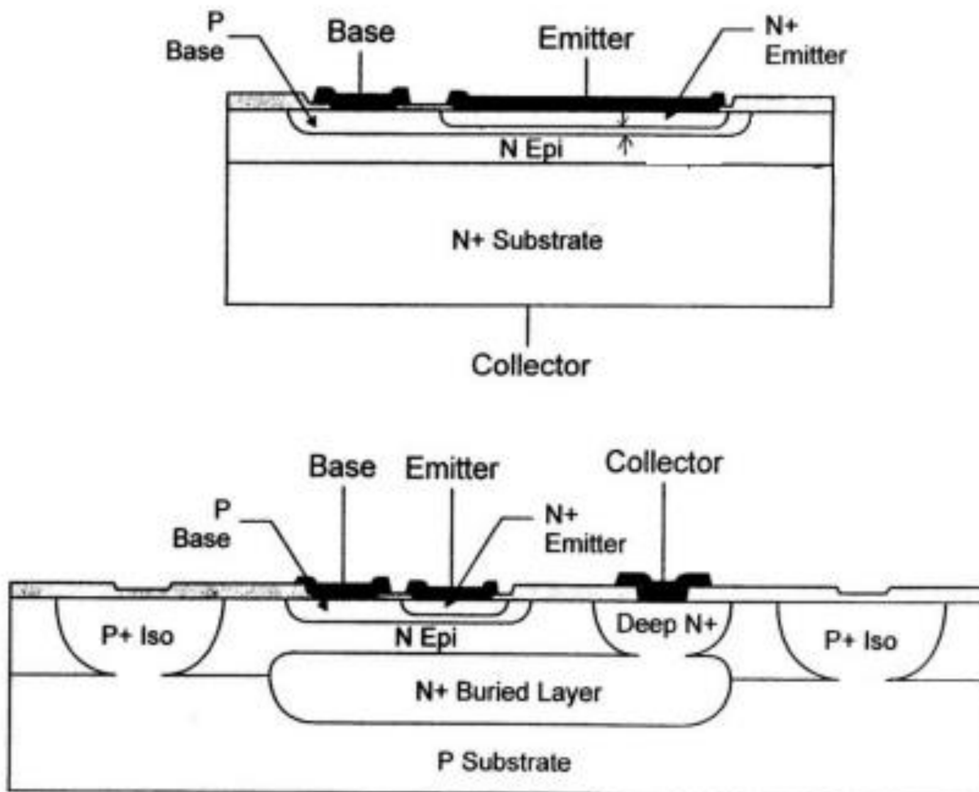


Figure 10: Semiconductor structures of BJT (above–discrete and bottom-integrated)

3.3. MOSFET

The field-effect transistor (FET), a voltage-amplifying device, is more compact and power efficient than BJT devices. A thin gate oxide located between the other two electrodes of the transistor insulates the gate on the MOSFET.

There are two categories of MOSFETs, nMOS (n-channel) and pMOS (p-channel), each which is defined by its majority current carriers. There is a biasing scheme for operating each type of MOSFET in conduction mode. Biasing will provide current or voltage (depending on the type of transistor) to sufficiently turn on and off the transistor. We will see these matters in subsequent topics in the course for BJT and FET types transistor.

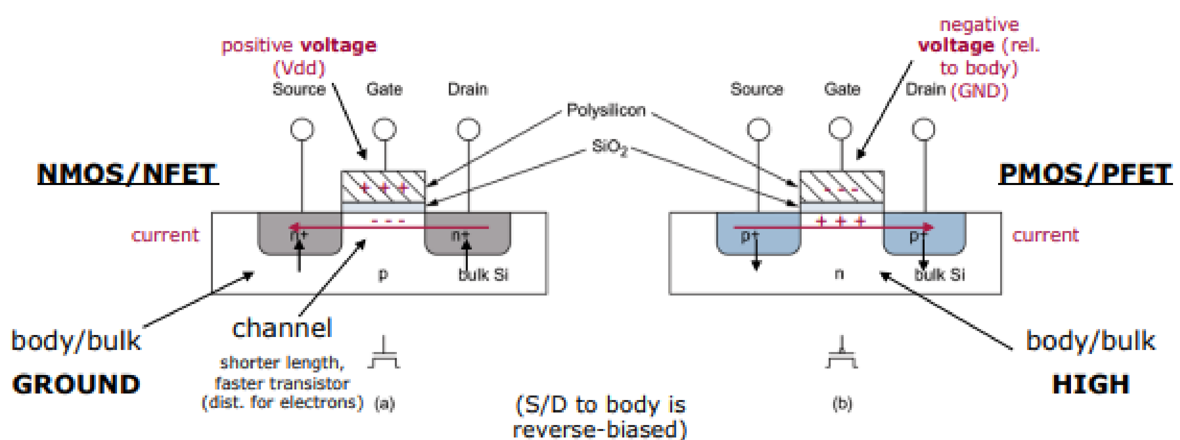


Figure 11: Semiconductor structure of MOSFET

3.4. BJT vs MOSFET

- MOS is simpler to produce than Bipolar. The minimum number of masks to make Bipolar is seven, and the minimum number of masks to make MOS is five.
- MOS requires less drive current. MOS devices are voltage controlled with high impedance inputs. Bipolar devices are current controlled with low impedance input.
- MOS dissipates less power. This is particularly true of CMOS logic which only draws power when switching states.
- MOS devices are simpler to isolate and can be packed more tightly. As we have seen, MOS has become the dominant technology.

3.5. CMOS

CMOS is a type of MOSFET (metal–oxide–semiconductor field-effect transistor) fabrication process that uses complementary and symmetrical pairs of p-type and n-type MOSFETs for logic functions (see the following diagram for the structure of this device). CMOS technology is used for constructing integrated circuit (IC) chips.

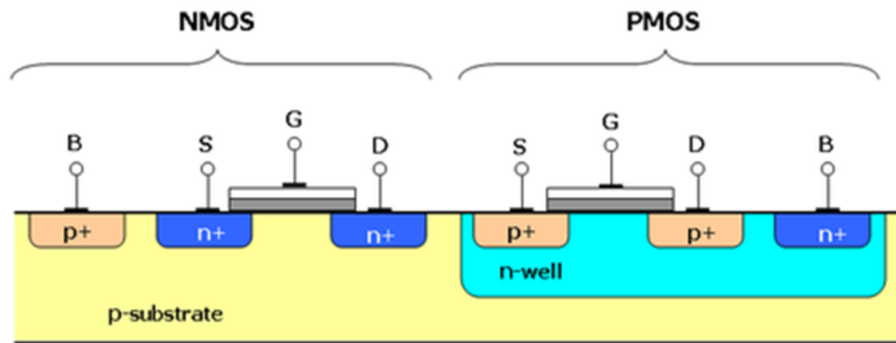


Figure 12: Semiconductor structure of a CMOS

4. Manufacturing of Semiconductor Devices

Microfabrication and hence manufacturing of semiconductor devices involves a substantial number of complex chemical and electro-chemical processes.

4.1. Processes in Manufacturing of Semiconductor Devices

The following diagram shows how these processes are performed in the factories i.e. from silicon ingot until the delivery of the device to the customers.

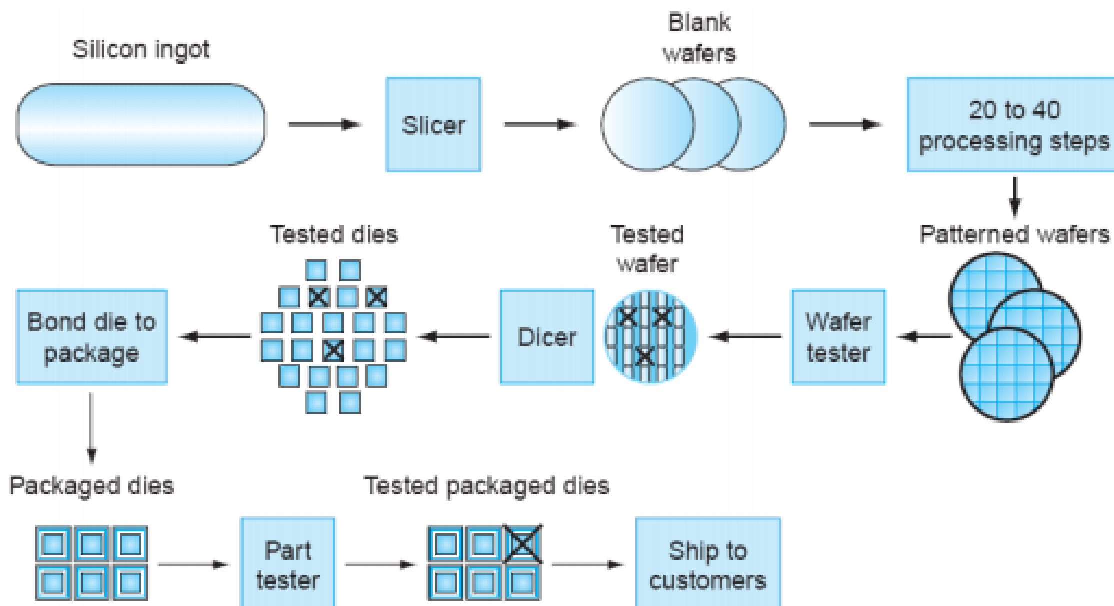
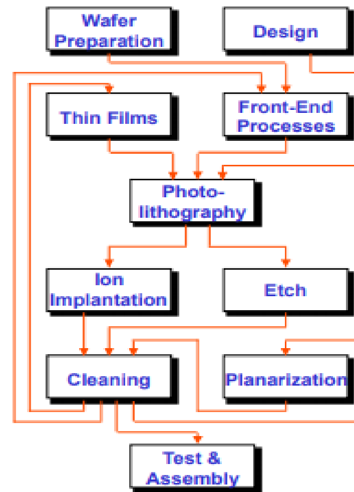


Figure 13: Processes in manufacturing of the semiconductor devices

In the industry, semiconductor-manufacturing process typically requires the following steps to be carried out:

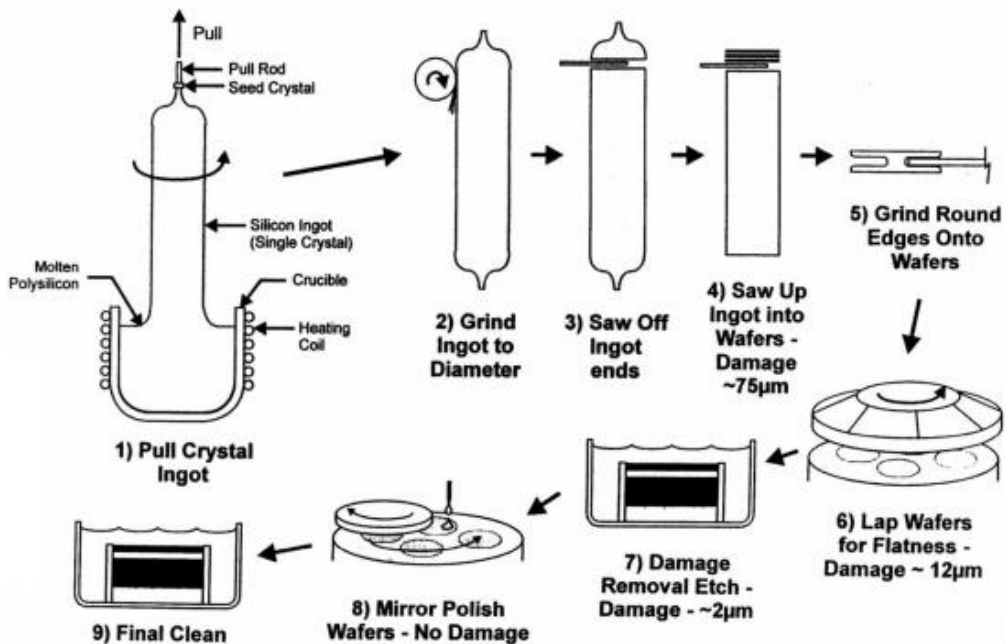
a. Design
b. Wafer preparation
c. Front-end processes
d. Photolithography
e. Etch
f. Cleaning
g. Thin films
h. Ion implantation
i. Planarization
j. Test and assembly



4.2. Details of Semiconductor Device Manufacturing Process

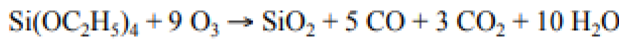
This section of the note describes some of these processes which are carried in the manufacturing of the semiconductor devices.

a. Wafer manufacturing process.



b. Chemical Vapor Deposition (CVD) Dielectric.

Chemical Reactions



$Si(OC_2H_5)_4 + 9\ O_3 \rightarrow SiO_2 + 5\ CO + 3\ CO_2 + 10\ H_2O$

Process Conditions (ILD)

Flow Rate: 100 to 300 sccm

Pressure: 50 Torr to Atmospheric

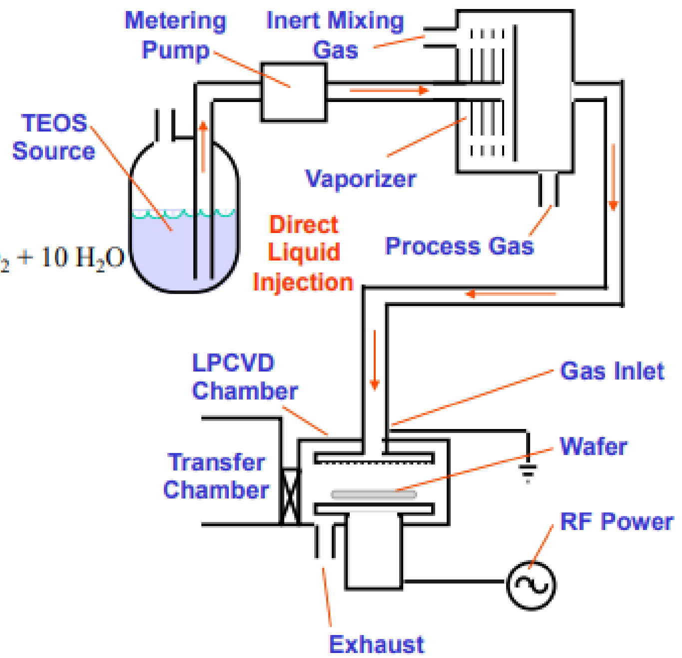
CVD Dielectric

O_2

O_3

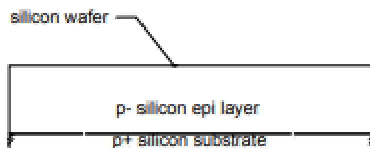
TEOS *

TMP *



* High proportion of the total product use

c. Thin films - Epitaxial Silicon Deposition.



Chemical Reactions

Silicon Deposition: $HSiCl_3 + H_2 \rightarrow Si + 3\ HCl$

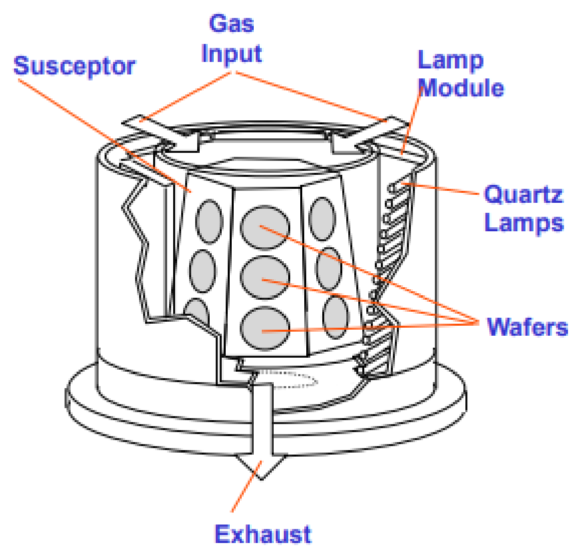
Process Conditions

Flow Rates: 5 to 50 liters/min

Temperature: 900 to 1,100 degrees C.

Pressure: 100 Torr to Atmospheric

Silicon Sources	Dopants	Etchant
SiH_4	AsH_3	HCl
H_2SiCl_2	B_2H_6	**Carriers**
$HSiCl_3$ *	PH_3	Ar
$SiCl_4$ *		H_2 *
		N_2



* High proportion of the total product use

d. Front-End Processes.

Chemical Reactions

Thermal Oxidation: $Si + O_2 \rightarrow SiO_2$

Nitride Deposition: $3\ SiH_4 + 4\ NH_3 \rightarrow Si_3N_4 + 12\ H_2$

Polysilicon Deposition: $SiH_4 \rightarrow Si + 2\ H_2$

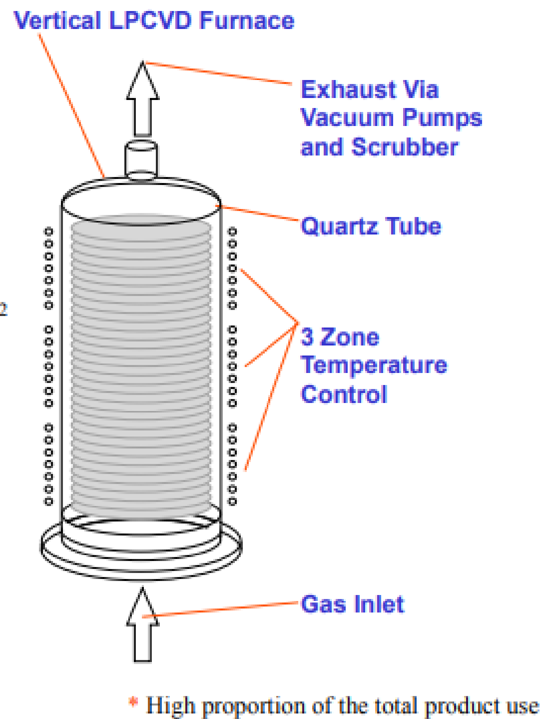
Process Conditions (Silicon Nitride LPCVD)

Flow Rates: 10 - 300 sccm

Temperature: 600 degrees C.

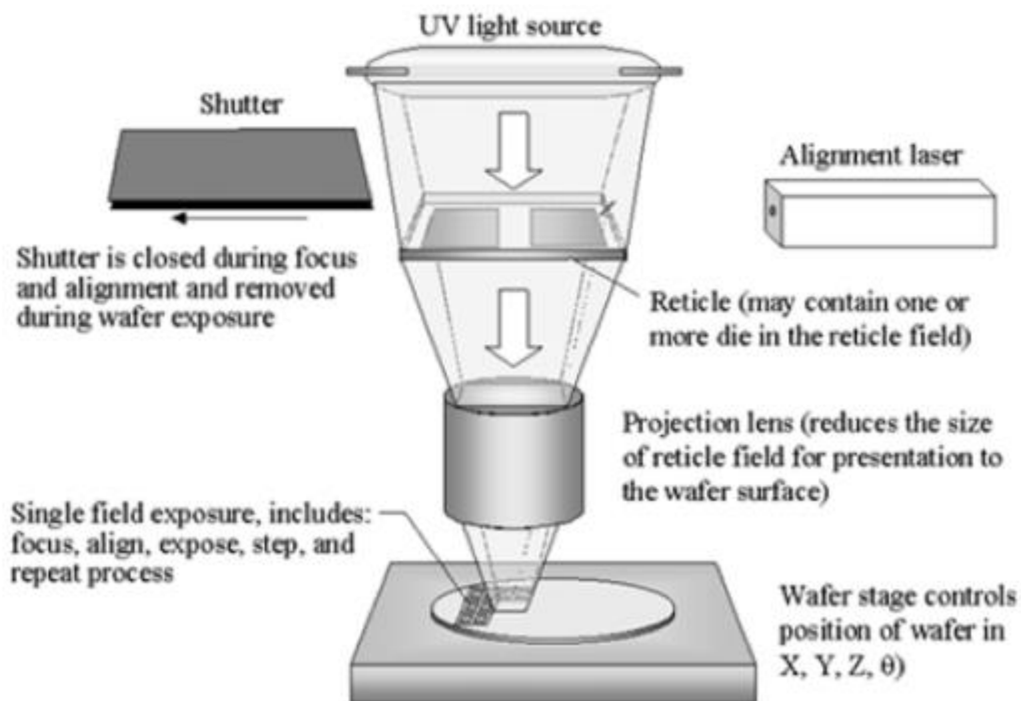
Pressure: 100 mTorr

Oxidation	Polysilicon	Nitride	Annealing
Ar	H_2	NH_3 *	Ar
N_2	N_2	H_2SiCl_2 *	He
H_2O	SiH_4 *	N_2	H_2
Cl_2	AsH_3	SiH_4 *	N_2
H_2	B_2H_6	$SiCl_4$	
HCl *	PH_3		
O_2 *			
Dichloroethene *			

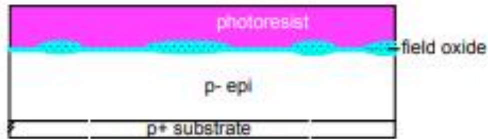


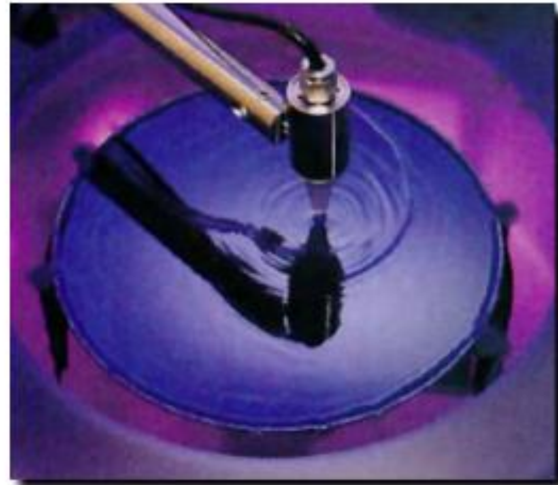
* High proportion of the total product use

e. Photolithography – Alignment & exposure.



f. Photoresist Coating Processes.





Photoresists

- Negative Photoresist *
- Positive Photoresist *

Other Ancillary Materials (Liquids)

- Edge Bead Removers *
- Anti-Reflective Coatings *
- Adhesion Promoters/Primers (HMDS) *
- Rinsers/Thinners/Corrosion Inhibitors *
- Contrast Enhancement Materials *

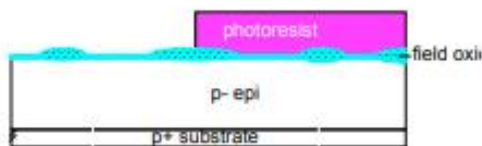
Developers

- TMAH *
- Specialty Developers *

Inert Gases

- Ar
- N_2

g. Exposure Processes.



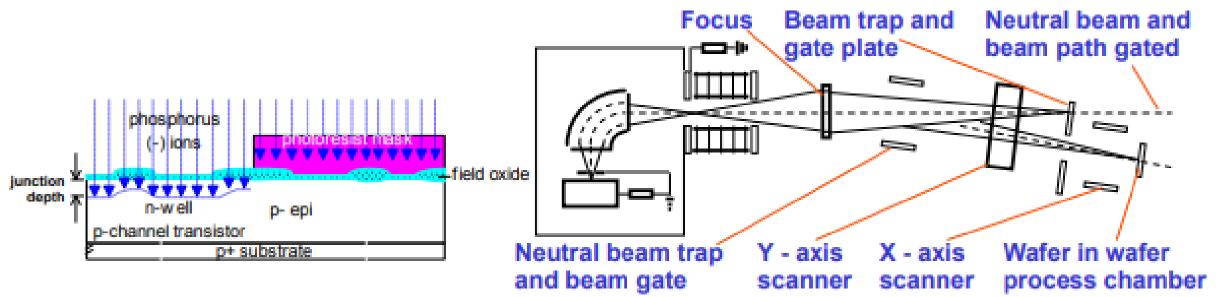
Expose

- $Kr + F_2$ (gas) *

Inert Gases

- N_2

h. Ion Implantation.



Process Conditions

Flow Rate: 5 sccm

Pressure: 10^{-5} Torr

Accelerating Voltage: 5 to 200 keV

Gases

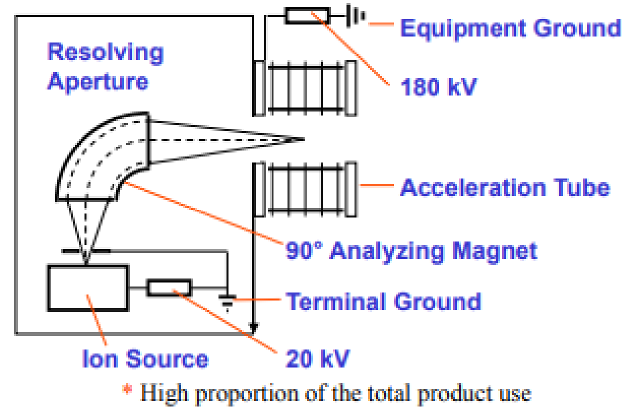
- Ar
- AsH_3
- $B^{11}F_3$ *
- He
- N_2
- PH_3
- SiH_4
- SiF_4
- GeH_4

Solids

- Ga
- In
- Sb

Liquids

- $Al(CH_3)_3$

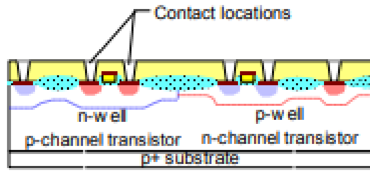


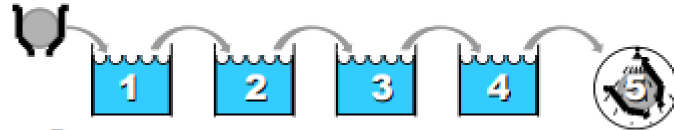
* High proportion of the total product use

i. Etching of the layers.

j. Cleaning process.

Critical Cleaning





Process Conditions
Temperature: Piranha Strip is 180 degrees C.

1 Organics
H_2SO_4 +
H_2O_2
H_2O Rinse

2 Oxides
HF +
H_2O
H_2O Rinse

3 Particles
NH_4OH +
H_2O_2 + H_2O
H_2O Rinse

4 Metals
HCl +
H_2O_2 + H_2O
H_2O Rinse

5 Dry
H_2O or IPA +
N_2

RCA Clean
SC1 Clean ($H_2O + NH_4OH + H_2O_2$) *
* SC2 Clean ($H_2O + HCl + H_2O_2$) *

Piranha Strip
* $H_2SO_4 + H_2O_2$ *

Nitride Strip
H_3PO_4 *

Oxide Strip
HF + H_2O *

Dry Strip
N_2O
O_2
$CF_4 + O_2$
O_3

Solvent Cleans
NMP
Proprietary Amines (liquid)

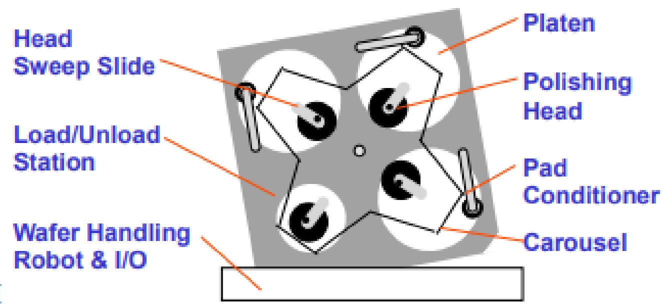
Dry Cleans
HF
O_2 Plasma
Alcohol + O_3

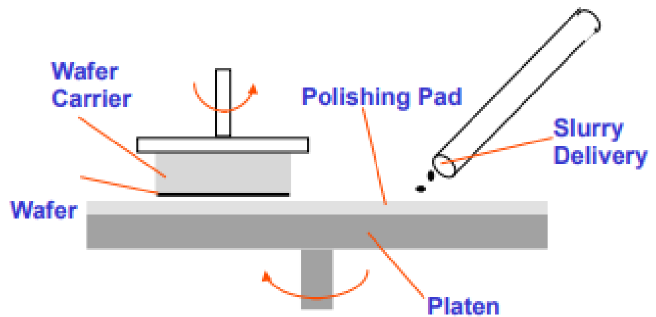
k. Planarization process.

Process Conditions (Oxide)
Flow: 250 to 1000 ml/min
Particle Size: 100 to 250 nm
Concentration: 10 to 15%, 10.5 to 11.3 pH
Process Conditions (Metal)
Flow: 50 to 100 ml/min
Particle Size: 180 to 280 nm
Concentration: 3 to 7%, 4.1 - 4.4 pH

Backing (Carrier) Film
Polyurethane
Pad
Polyurethane
Pad Conditioner
Abrasive

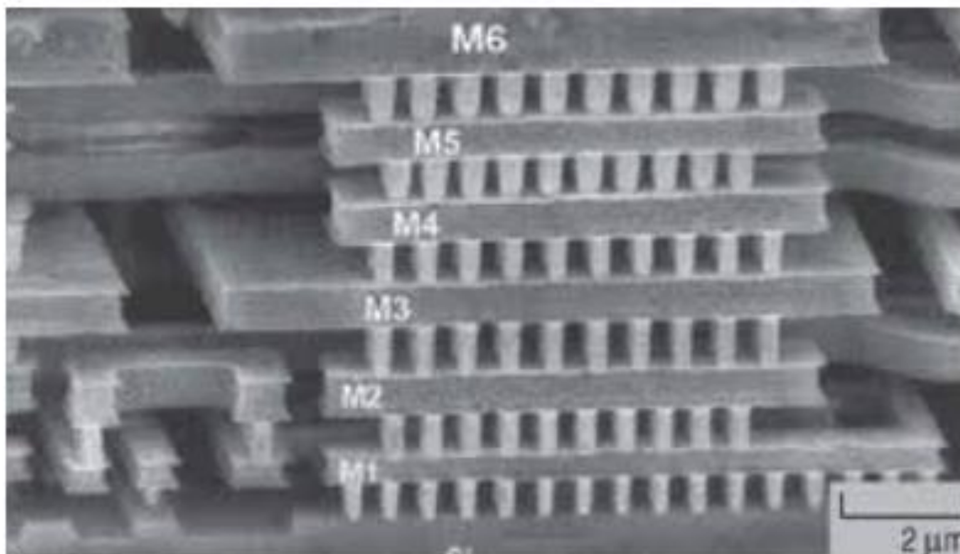
CMP (Oxide)
Silica Slurry *
KOH *
NH_4OH
H_2O
CMP (Metal)
Alumina *
$FeNO_3$

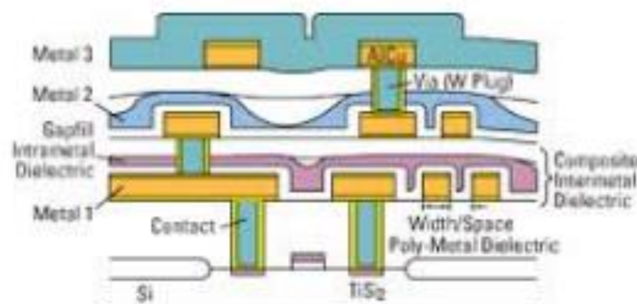




* High proportion of the total product use.

l. Metallization process.





m. Test and assembly process.

- Wafer inspection.
- Wafer probe / bumped wafer probe:
    - 300mm wafer probe / bumped wafer probe.
    - Vertical wafer / bumped wafer probe.
    - Laser trim.
- Final test.
- Dry-bake, packing, tape and reel.

Example for Tutorial

1. Describe the processes involved in the silicon wafer manufacturing. [2 marks]

   Answer

   Semiconductor manufacturing begins with production of the wafer, i.e., a thin, round slice of a semiconductor material varying in size 6 inches to 12 inches in diameter. The finished wafer is approximately 15 mil thick. The materials are primarily silicon; however, gallium arsenide, silicon carbide, germanium, and others undergo similar processes. Purified polycrystalline silicon is created from sand, one of the most abundant materials available on our planet, is heated to a molten liquid. In a process similar to repeatedly dipping a wick in wax to make a candle, a small piece of solid silicon (seed) is dipped in molten liquid. As the seed is slowly withdrawn (by mechanical means) from the melt, the liquid quickly cools to form a single crystal ingot.

   This cylindrical crystal ingot is then ground to a uniform diameter. A diamond saw blade slices the ingot into thin wafers. The cut wafers are then processed through a series of machines where they are ground (optically) smooth and chemically polished.

   The wafers are now ready to be sent to the wafer fabrication area fab, where they are used as the foundation for manufacturing integrated circuits (ICs).

2. Describe the commonly found steps for manufacturing typical semiconductor devices. [5 marks]

   Answer

   The process of manufacturing semiconductors or integrated circuits (commonly called ICs or chips) typically consists of hundreds of steps, during which hundreds of copies of an integrated circuit are formed on a single wafer.

   Generally, the process involves the creation of 8 to 20, and frequently more, patterned layers on (and into) the wafer, ultimately forming the complete integrated circuit. This

layering process creates (interconnected) electrically active regions on the semiconductor wafer surface.

The heart of any semiconductor manufacturing business is the fab, where the integrated circuit is formed on the wafer. The fabrication process, which takes place in an environmentally controlled clean room, involves a series of principle repetitive steps described below. Typically, it takes from 10-30 days, but frequently much longer, to complete the fabrication process.

Thermal oxidation–wafers are pre-cleaned using high-purity deionized water and various low-particulate chemicals, a must for high-yield production. The silicon wafers are heated to approximately 1000 c and exposed to ultra-pure oxygen in the oxidation furnace. Under carefully controlled conditions, a silicon dioxide insulator film of uniform thickness is formed on the surface of the wafer.

Patterning–masking is used to protect one area of the wafer while working on another. This process is referred to as photolithography. A photo resist, light-sensitive film is spin-coated onto the wafer, giving it characteristics similar to a photographic film. A (micro) aligner aligns the wafer to a glass mask and then projects an intense ultraviolet light through the mask, exposing the photo resist with the mask pattern, thereby transferring the image from the mask into the light-sensitive film.

Etching–the wafer image is then developed (like a photo negative). The exposed photo resist is chemically removed and baked to harden the remaining photo resist pattern, which now is no longer light sensitive. It is then exposed to a chemical wet solution or plasma (gas discharge) so that areas not covered by the hardened photo resist are etched away. The remaining photo resist is now removed using either wet or plasma chemistry. The wafer is optically inspected to assure that the image transfer from the mask to the top silicon layer is correct, and then goes on to the next step.

Doping/diffusion–atoms with one less electron than silicon (such as boron) or one more electron than silicon (such as phosphorus) are introduced into the area exposed by the etch process, to alter the electrical character (conductivity) of the silicon. These areas are called p type or n type, respectively, which reflects their conducting characteristics.

Complete front end layer— Repeating the above steps: the thermal oxidation, masking, etching, and doping steps are repeated many times until the last “Front end” layer is completed (all active devices have been formed).

Dielectric deposition and metallization–following completion of the “Front end,” the individual devices are interconnected “Backend” (like on a pc board) using a series of alternating metal depositions, dielectric films, with their respective patterning. Current semiconductor fabrication includes as many as 5 to 7 metal layers for logic, and fewer for memory, separated by dielectric layers (insulators).

Passivation–after the last metal is patterned, a final insulating layer (passivation) is deposited to protect the circuit from damage and contamination. Openings are etched in this film to allow access to the top metal later by electrical probes and subsequent wire bonds.

Electrical test–an automatic, computer-driven test system checks for functionality of each chip on the wafer. Chips that do not pass the test are marked for automatic rejection. For simpler devices a mechanical probe is used.

Assembly–a diamond saw slices the wafer into single chips. Sizes can vary from 1 x 1 mm to 10 x 10 mm. The rejected chips are discarded and the remaining chips are visually inspected under a high-power microscope before packaging.

Each chip is then assembled into an appropriate package that provides the contact leads for the chip. In one type of interconnect a wire bonding machine attaches wires, a fraction of the width of a human hair, to the leads of the package. The packaged chip is tested again prior to delivery to the customer. Alternatively, the chip can be assembled in a ceramic package for certain high-performance applications.

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