Demo 7 – BJT Amplifier Simulation in LTspice

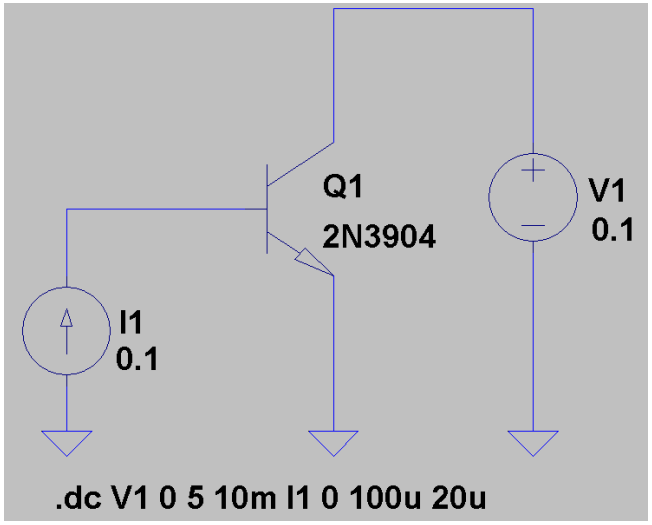
XMUT204 Electronic Design

Overview

- Current to voltage characteristics of BJT.
- Common emitter amplifier:
  - Picking a Q-point for the transistor.
  - Designing the bias network.
  - Adding the source and decoupling capacitors.
- BJT amplifier bandwidth.

A. Current to Voltage (V-I) Curve Graph of BJT Transistor

Create the schematic of the following common emitter BJT transistor circuit in LTspice.

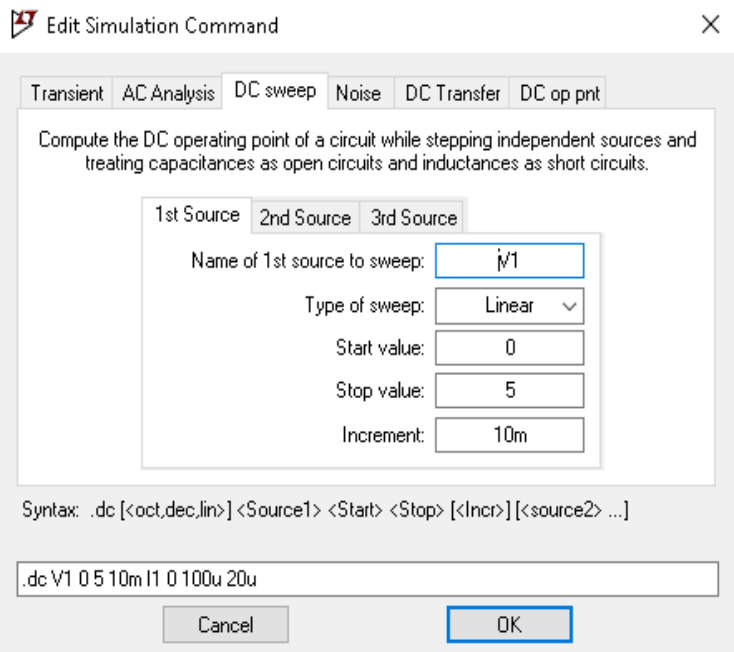


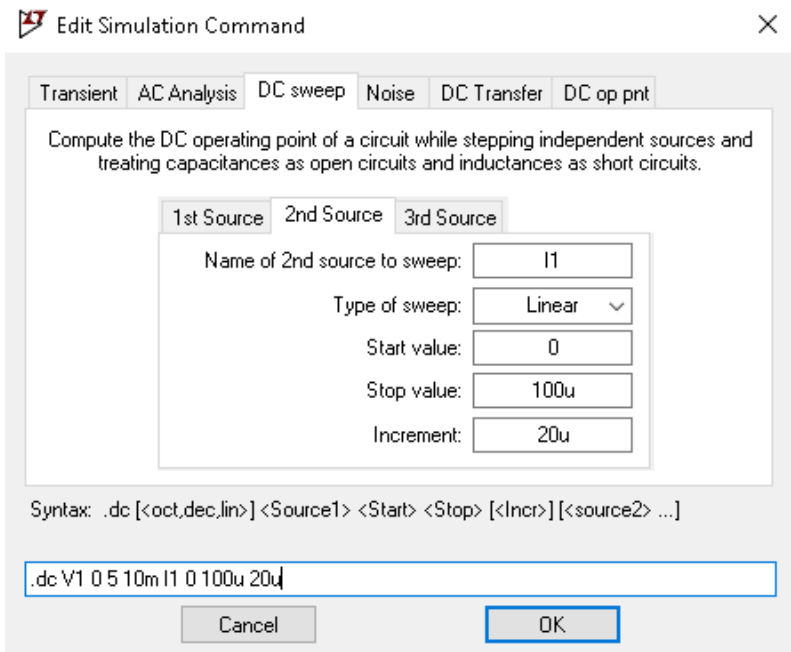
The transistor is chosen as 2N3904 and its collector is biased by voltage source V1 and on the other hand its base is biased by current source I1.

In the edit simulation command, from the main menu in LTspice, set up two DC sweeps i.e. one for collector voltage, the other for base current.

In the DC sweep configuration, set the first source to be voltage source V1 for linear sweeping, start value at 0 V to stop value at 5 V with increment of 10 mV.

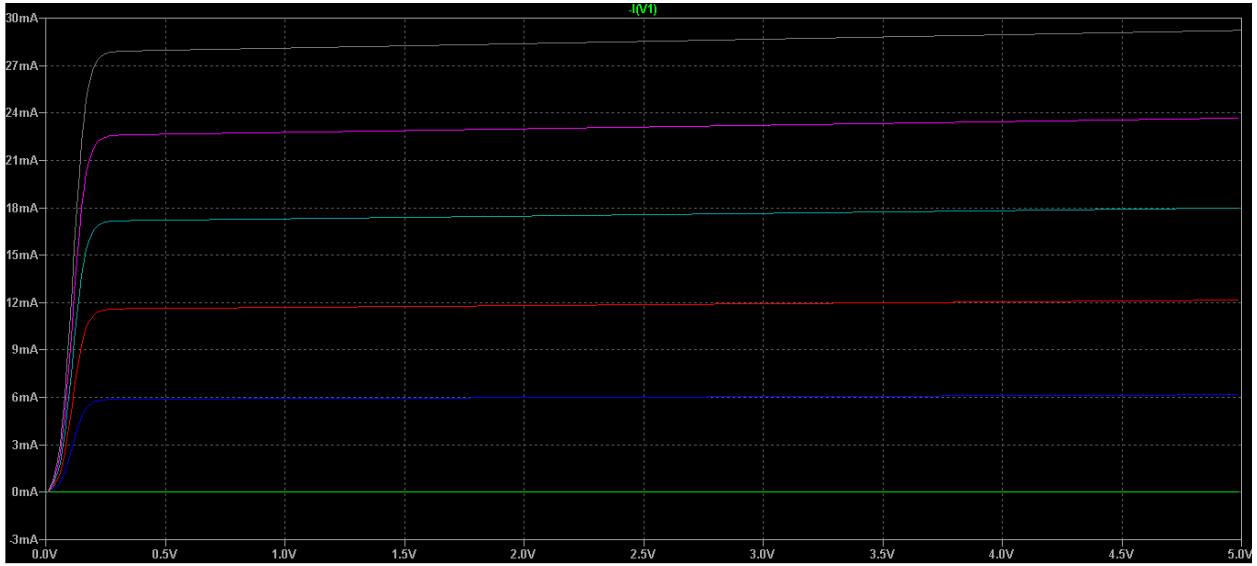
Set the second source for current source I1 for linear sweeping, start at 0 and stop at 100 uA for increment of 20 uA.





Then run the simulation. Pick the current that flows in the collector (I(V1)) of the circuit for plotting.

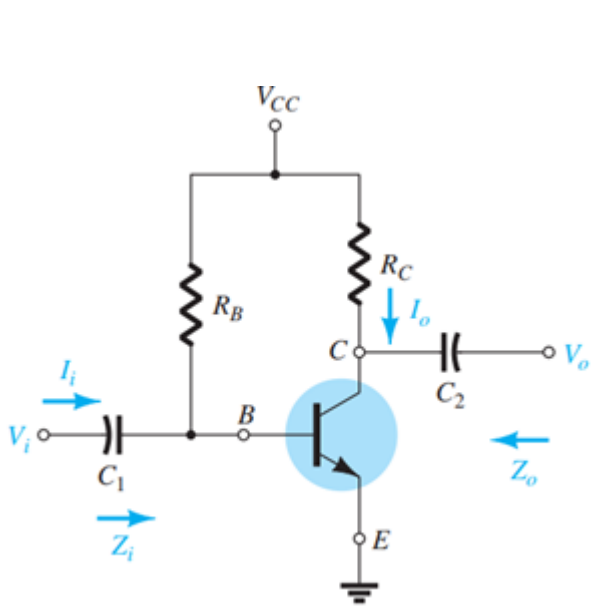
The outcome of the simulation is given in the following figure. Notice that the plots are shown for different set values of base currents (Ib) in the circuit.

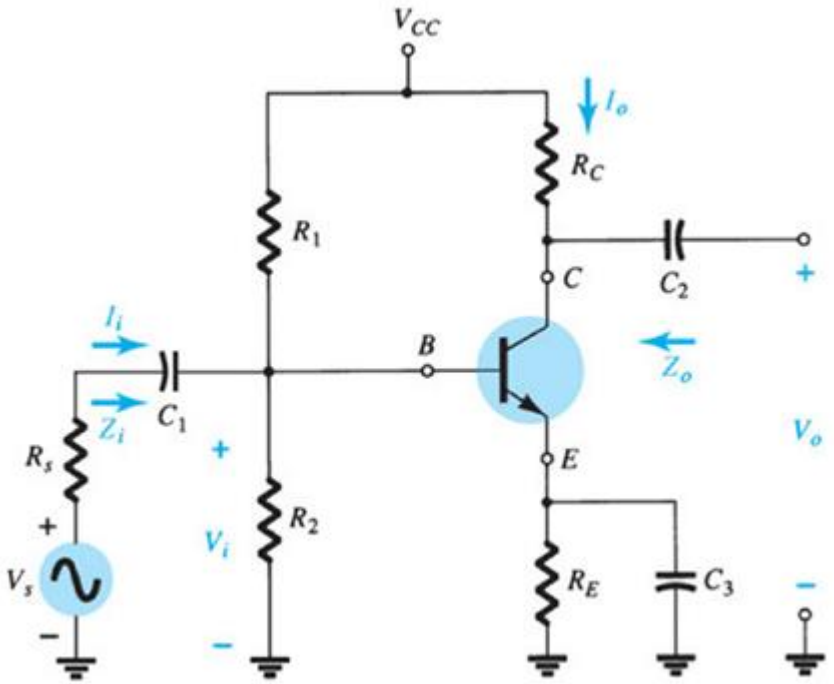


B. Common Emitter Amplifier

In this exercise, we try to design a run-of-the-mill common emitter amplifier from the ground up.

We certainly left some aspects out e.g. like gain, input and output impedance, but here is a brief overview of how the design went.



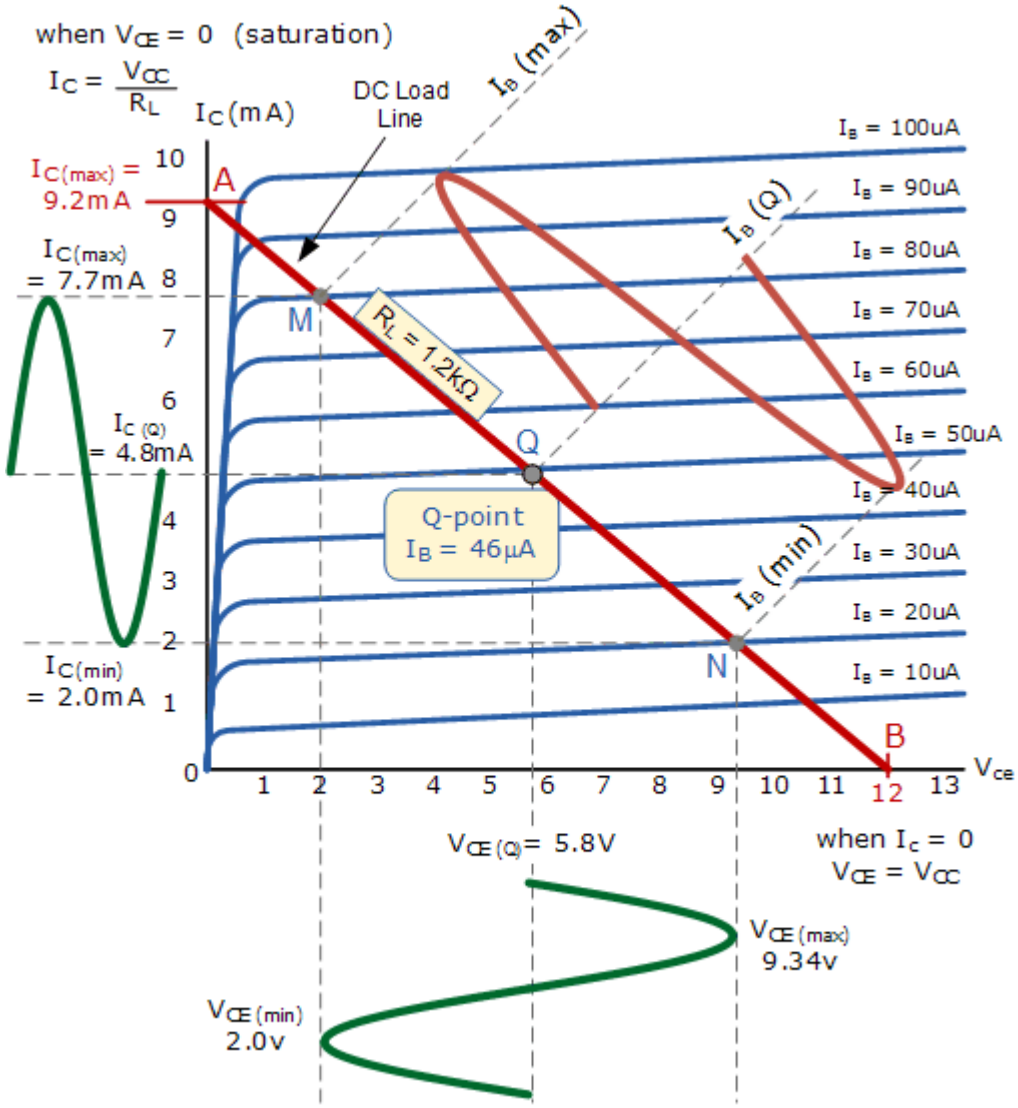


B.1. Picking a Q-Point for the Transistor

The first order of business is to decide on the DC operating characteristics for the transistor.

There are some considerations taken into account in this case e.g. choice of Q point can give an impact towards power consumption, linearity, and noise of your amplifier, among other things.

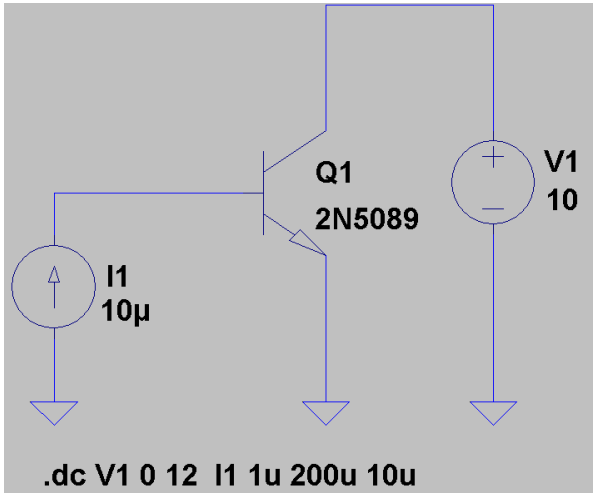
As a first guess, it is good to pick a Q point away from saturation, so your amplifier remains in the active state for all input voltages.

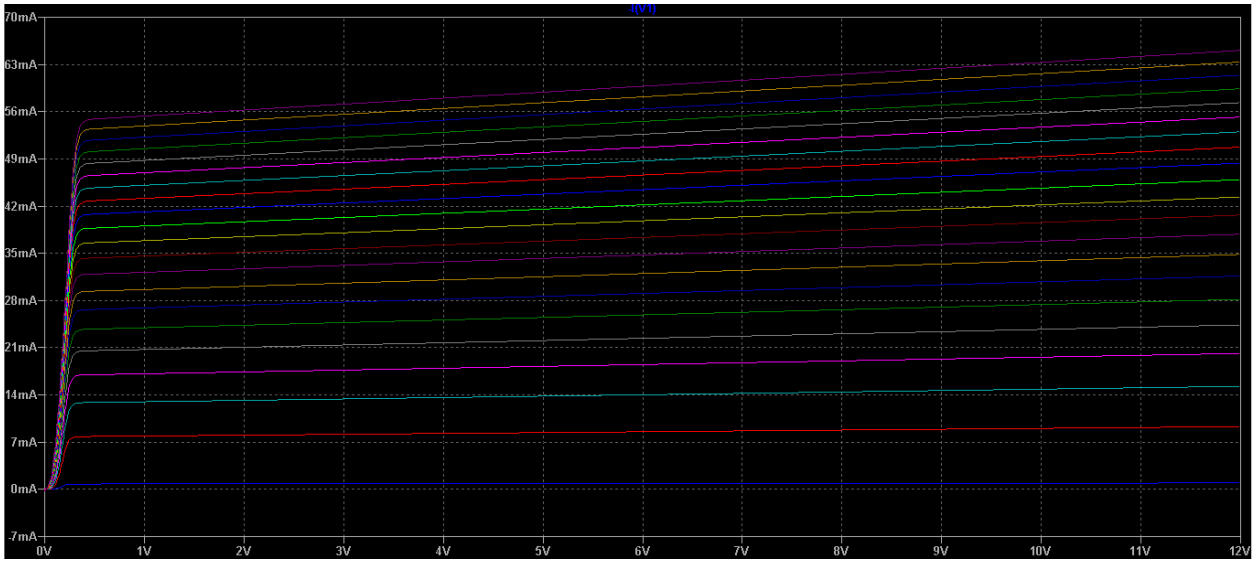


Create and simulate the following common emitter amplifier in LTspice.

In the LTspice, set up a curve trace in LTspice, perform a double-DC sweep, and pick out a good Q-point.

The result of the simulation is given in the following figure.





By referring to the result of the simulation given above, select Q point for common emitter amplifier i.e. Ic = about 30 mA, Vce = 6 V.

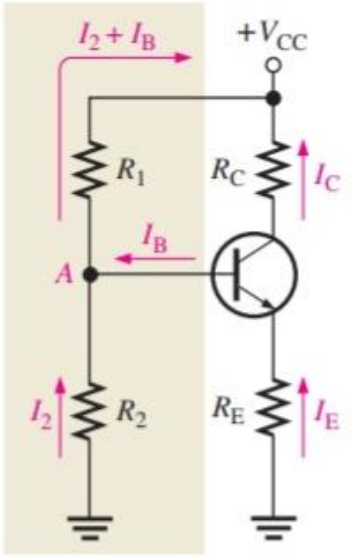
B.2. Designing the Bias Network

Design a bias network that provides biasing to the transistor at the Q-point we chose earlier.

From out last simulation, our Q point is Vce = 6 V, Ic = 30 mA.

Try to compute R1, using a voltage divider:

$$Vbb = (Vcc*(R2/(R1+R2))$$



Pick Vbb = 2 V and R1 = 1kΩ, rearranging the equation given above:

$$R1 = R2*(Vcc-Vbb)/Vbb = 4\ k\Omega$$

For computing the resistor at the emitter in the circuit R3, the voltage across R3 is given as follows:

$$Ve = Vbb – Vbe = 2\ V - 0.7\ V = 1.3\ V$$

Remember Ic = Ie = 30 mA, the value of resistor at the emitter, R3:

$$R3 = Ve/Ie = 1.3\ V/30\ mA = \text{about } 40\ \Omega$$

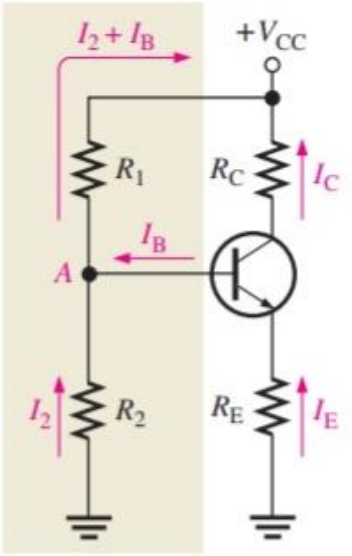
Computing the resistor at the collector in the circuit R4, the voltage across R4 is determined from the Vcc, Vce (from the Q point) and Ve (across R3):

$$V4 = 10 - (6) - (1.3) = 2.7\ V$$

Work out the value of R4:

$$R4 = Vc/Ic = 2.7/30\ mA = 90\ \Omega$$

So, the value of the resistor at the collector, R4 = 90 Ω.

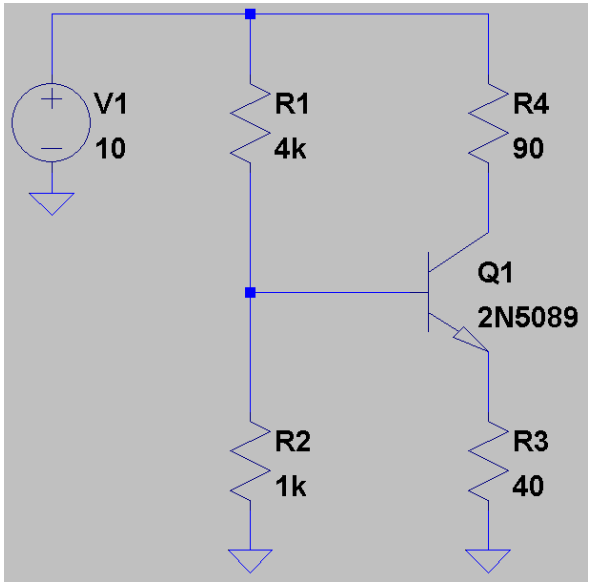


The following diagram outlines the resulting overall design parameters of the DC biasing of the amplifier.

By simulating DC point of the circuit, the actual results was found to be:

$$Vbb = 1.95\ V,\ Ic = 29.3\ mA$$

There are other design considerations here i.e. the design of the bias network impact gain and output impedance of the amplifier.

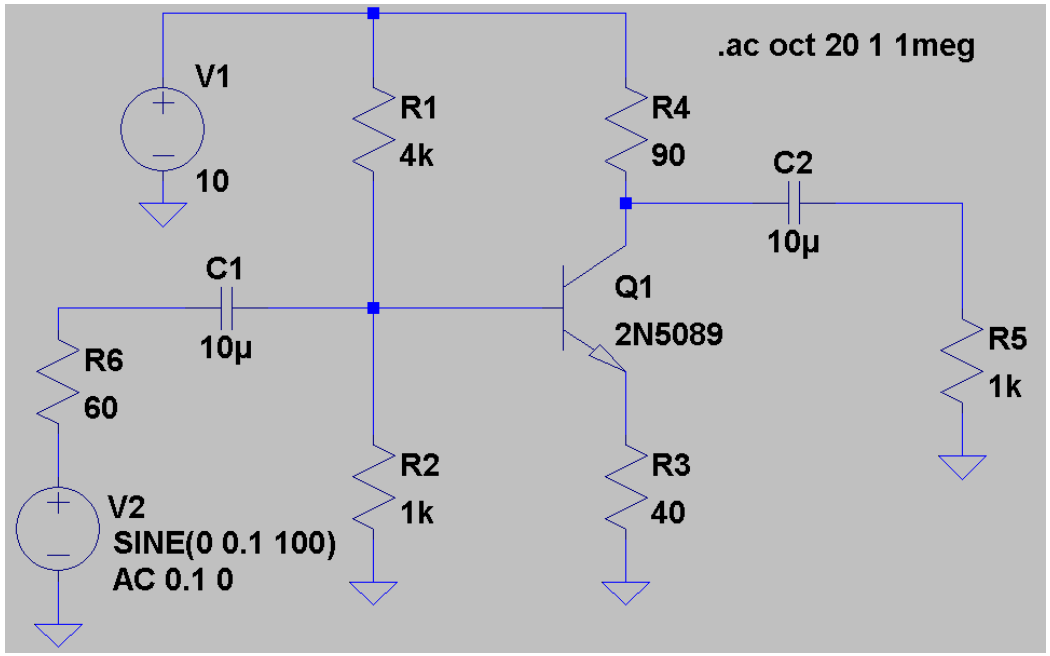


B.3. Adding the Source and De-Coupling Capacitors

Add the source and load, and add the decoupling capacitors.

Remember, the decoupling capacitors exist so that any DC from the source does not upset your bias point for your transistor.

The input and output decoupling capacitors block DC offsets from the input and output.

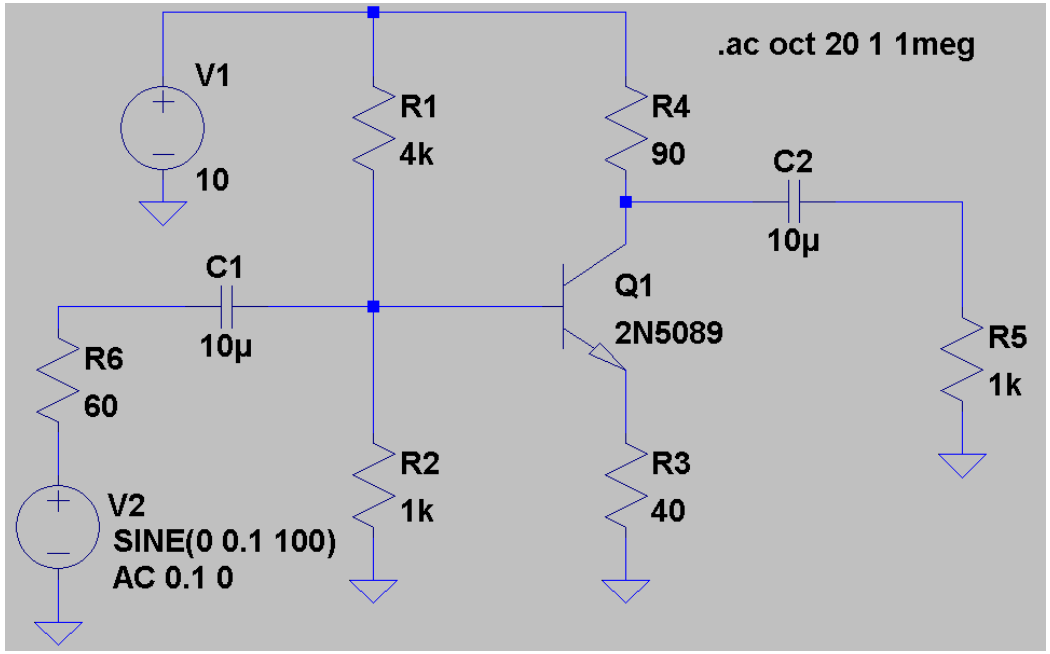


Assign the values of these capacitors i.e. C1 and C2 to be both equal to 10 uF.

Notice also addition of the internal resistance of the voltage source 60 Ω and load resistor which is equal to 1 kΩ.

Set the voltage course at the input to be AC sinewave signal at 10 mV peak-to-peak with frequency of 100 Hz.

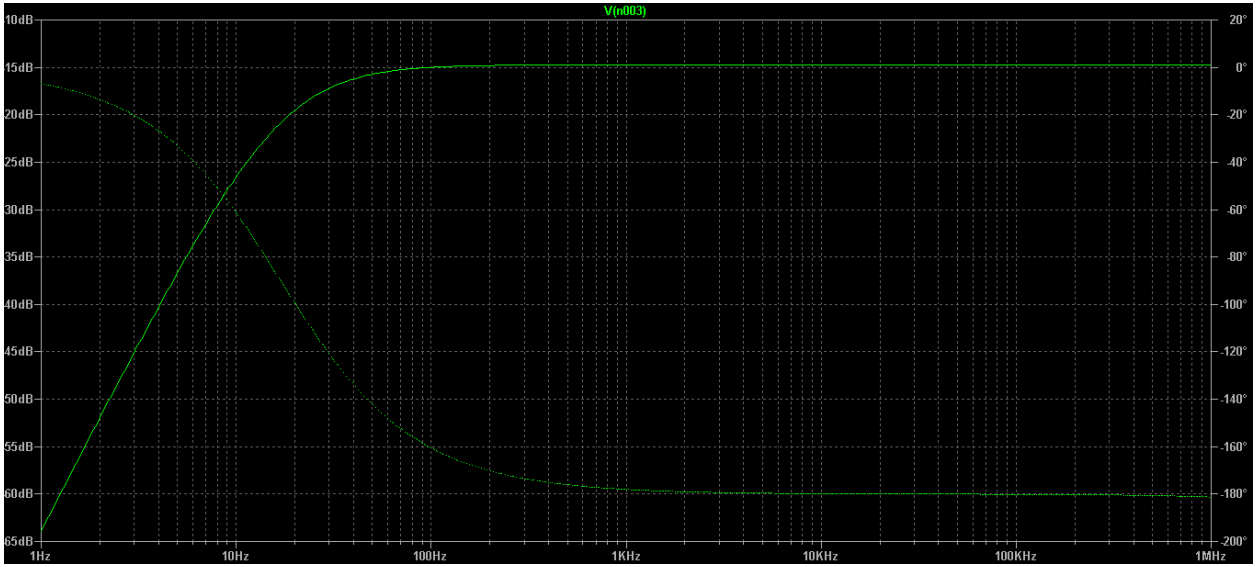
Include also definition of the small signal AC analysis values of 0.1 for AC Amplitude at 0 for AC Phase.



Adjusted the bias network a little bit to get more gain.

View the amplifier frequency response through the following SPICE directive:

```
.ac oct 20 1 1meg
```

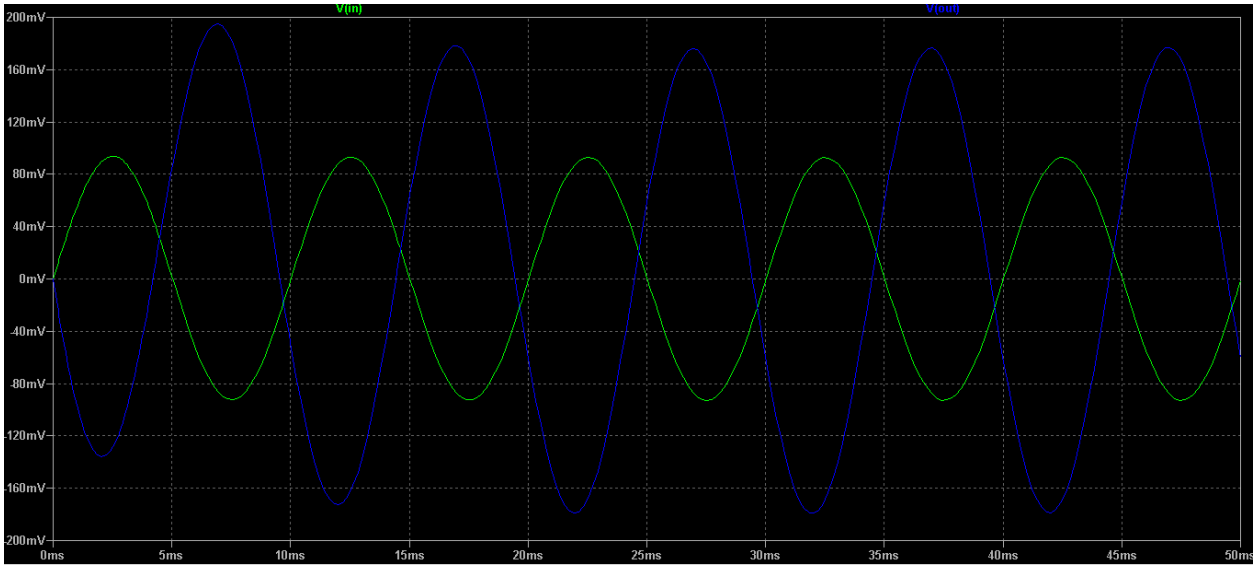


From the frequency response of the amplifier as given in the figure above, the gain is found to be about 15 dB with the frequency range measured from 100 Hz to 1 MHz.

Note that the phase shift at this range of the frequency is found to be 180°.

View the amplifier transient response through the following SPICE directive:

```
.tran 0 .05 0 0.1m
```



From the result of the simulation given above, the gain of the amplifier is given as:

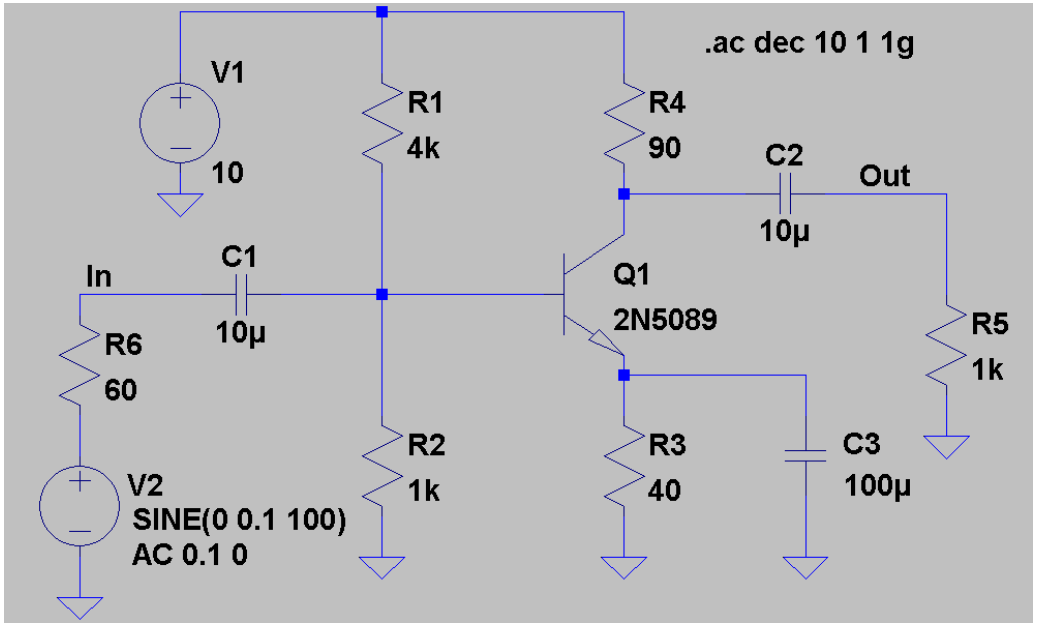
$$A = \frac{V_{out}}{V_{in}} = \frac{200\ mV}{90\ mV} = 2.25$$

The steps that we carried out is certainly not the most thorough design, but a starting point nonetheless.

C. BJT Amplifier Bandwidth

This exercise is an example for measuring BJT bandwidth in LTspice.

Create and simulate the common emitter BJT transistor amplifier given in the figure below.

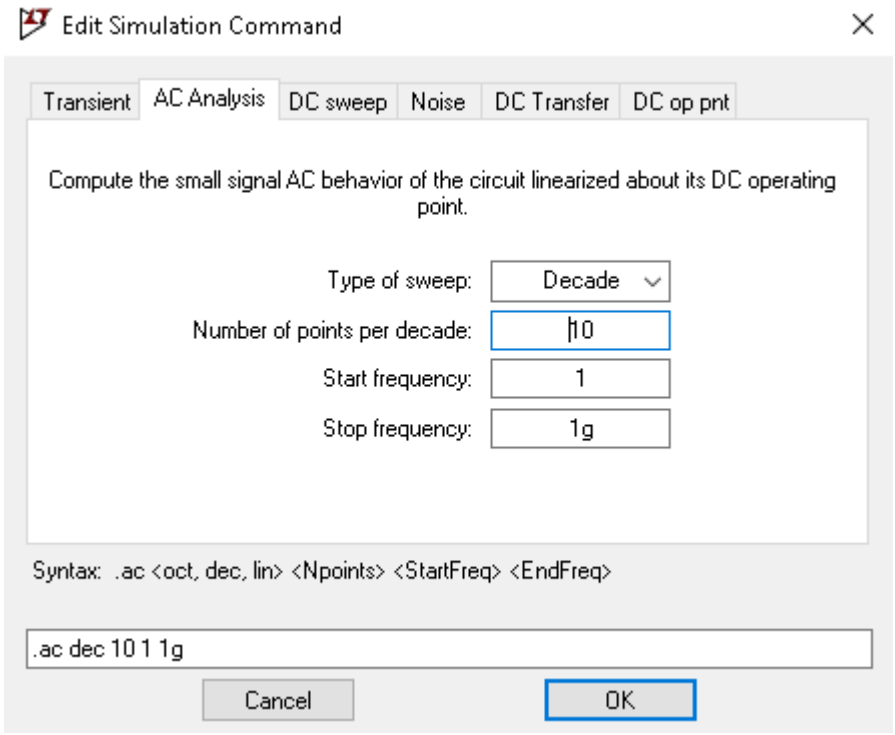


Note that from the circuit given in the previous section, we add C3 which is the emitter bypass capacitor with value of 100 uF.

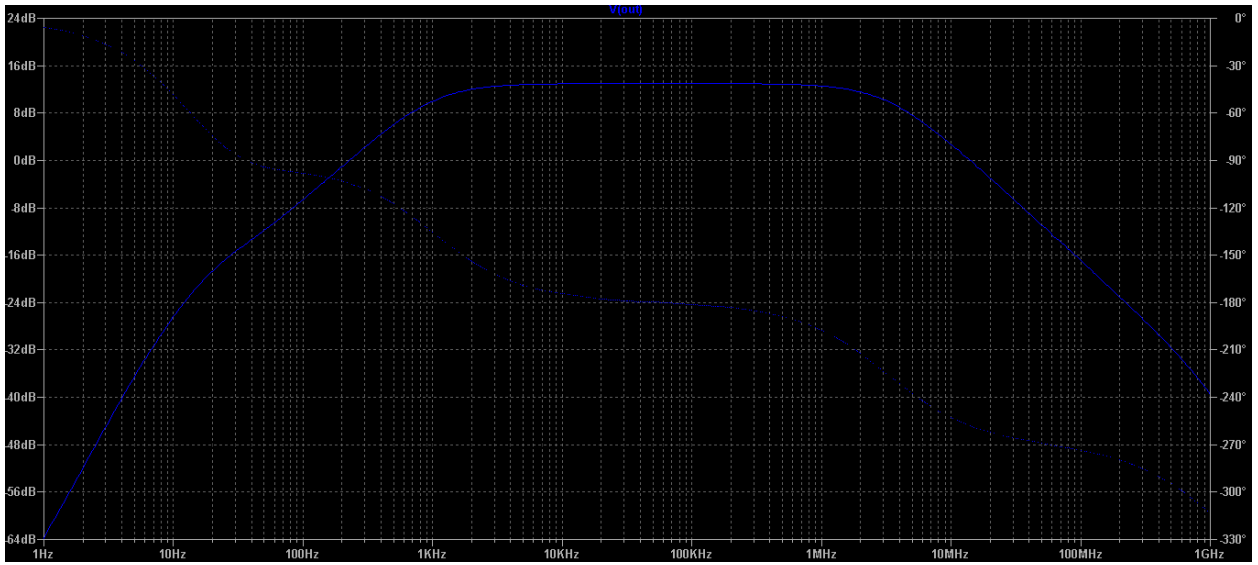
The addition of this capacitor is to stabilise and increase the gain of the amplifier.

Once circuit is completed, pick the AC Analysis tab of the Edit Simulation Command, which is found in the Simulate menu.

Set up the simulation for decade sweep with frequency from 1 Hz to 1 GHz with 10 number of points per decade.



Run simulation. The outcome of the simulation is given in the following figure.



In the frequency response plot of the amplifier as given above it is shown that at operating frequency bandwidth from 1 kHz to 1 MHz, the gain of the amplifier is measured at around 13 dB and the phase shift is around 180° centred at frequency around 50 kHz.