XMUT204 Electronic Design

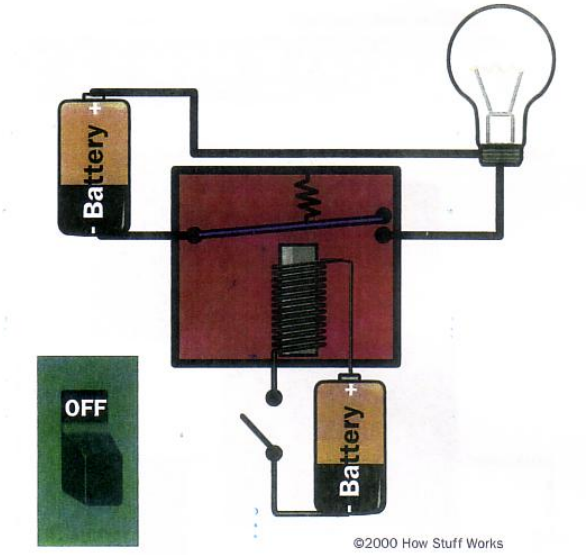
Lecture 3c – BJT Switching Applications

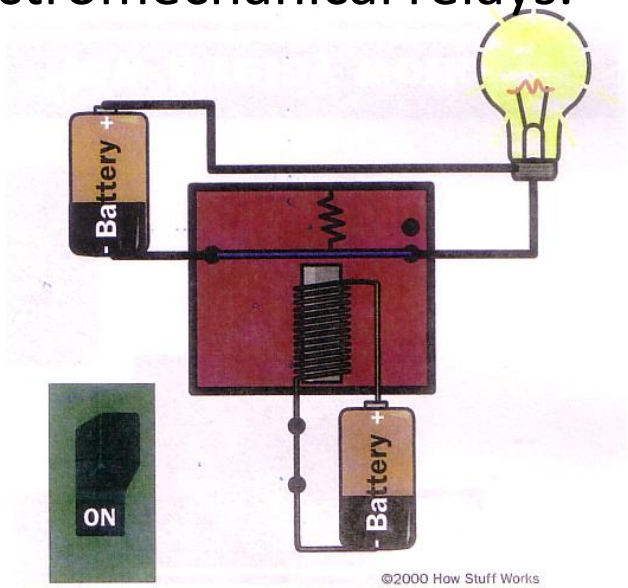
Overview

1. The Use of Electrical/Electronic Switch in Circuit.
2. Using the Transistor as Switch.
3. The Output Current-Voltage Characteristics.
4. BJT Switching Operation.
5. DC Gain (β_{DC}) to Use.
6. Load Line of BJT Switching Circuit.
7. Design with Common Emitter Configuration.
8. Logic Device Families.

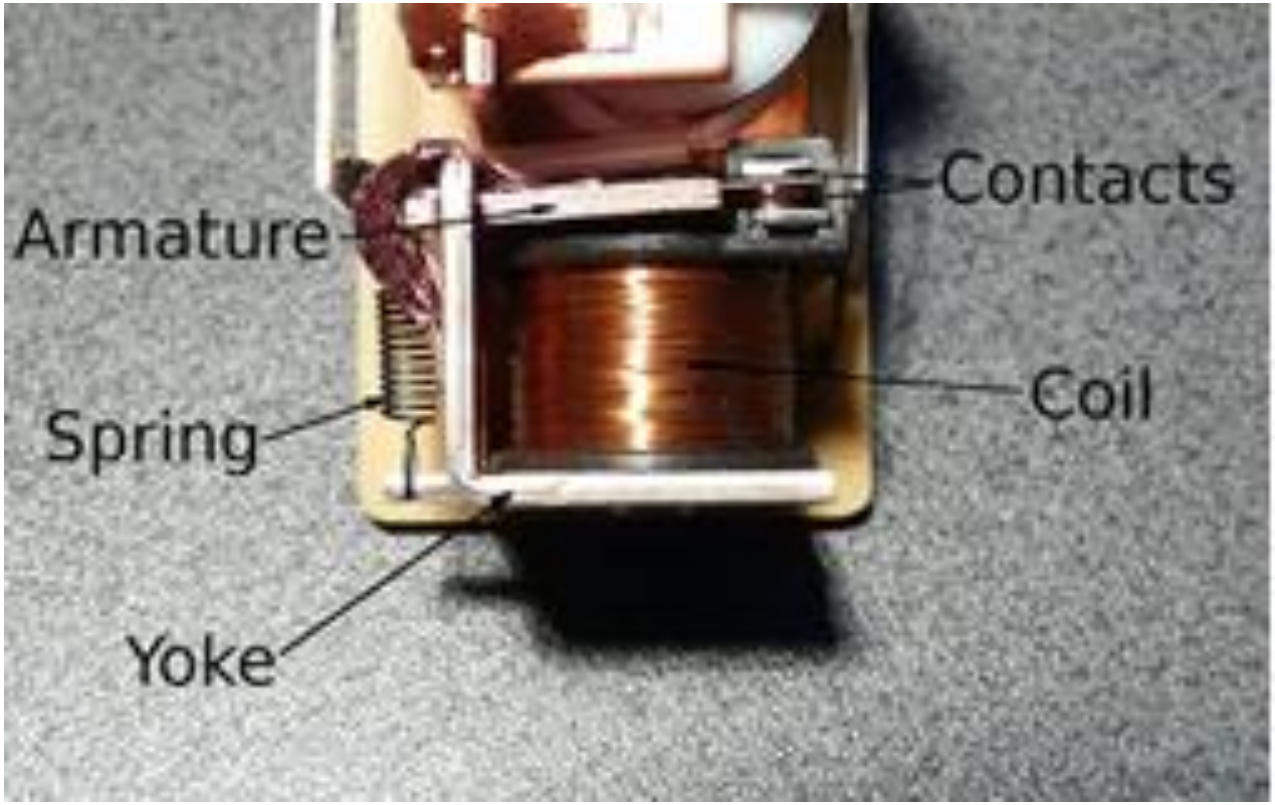
1. The Use of Electrical/Electronic Switches in Circuits

- Familiar with the use of mechanical ON/OFF switches in circuits which will make/break a circuit.
- Often need for one part of a circuit to be able to switch ON/OFF a secondary circuit.
- Status of the secondary circuit depends on the status of the primary circuit(s).
- One method to do this is by electromechanical relays.





1. The Use of Electrical/Electronic Switches in Circuits



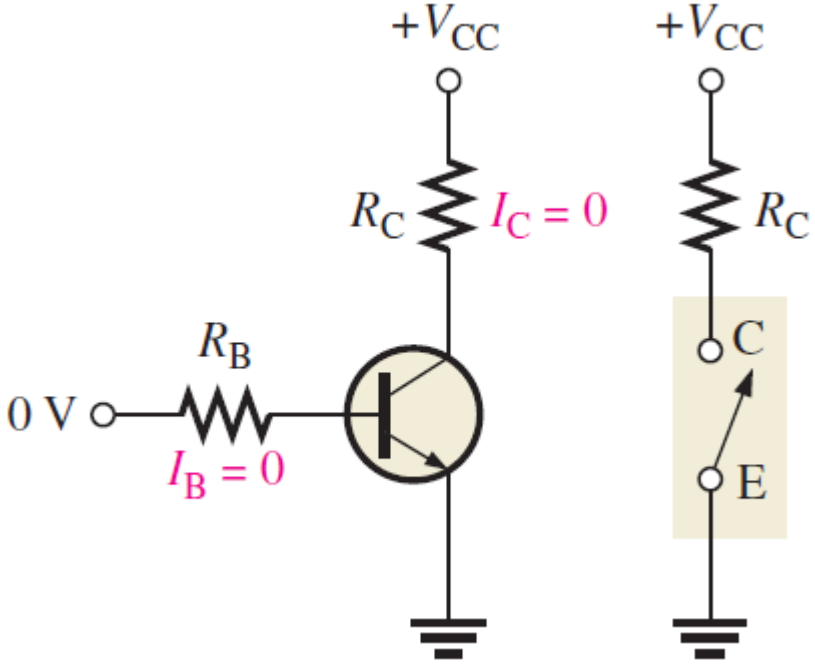
- Parts of a typical relay – contact is on/off depends on states of coil.

1. The Use of Electrical/Electronic Switches in Circuits

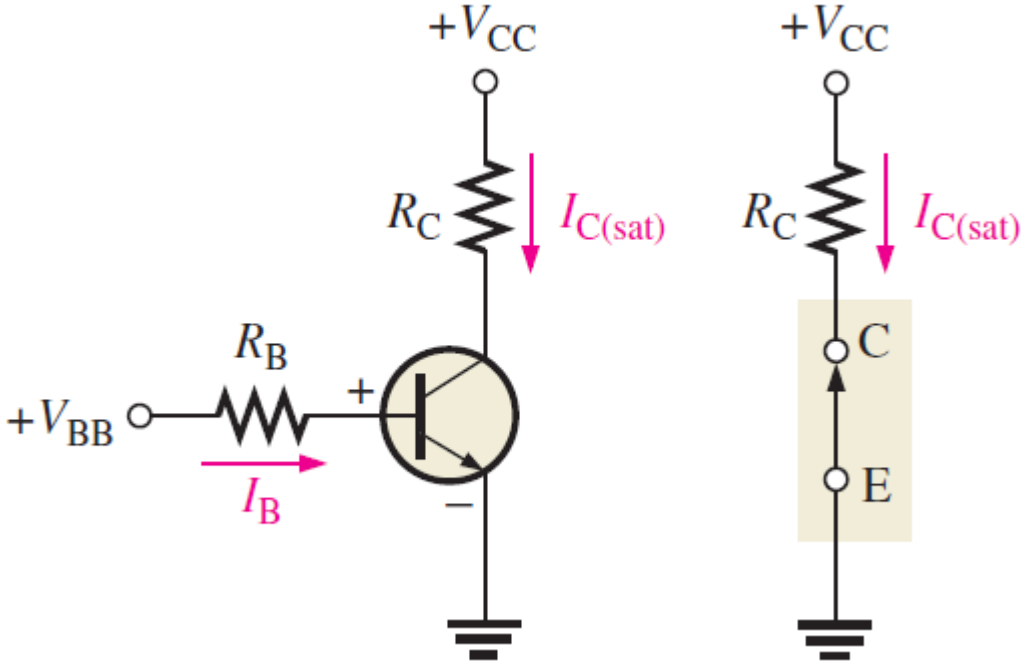
- However, for a number of reasons, the transistors has totally replaced relays as switching elements.
- This is particularly true in low current applications.

2. Using the Transistor as a Switch

- We can use the transistor as an ON – OFF switch by switching it between the cut-off region (transistor OFF and I_C = 0) and the saturation region (transistor ON and I_C = max)



- Transistor OFF
- Open switch
- Cut-off mode

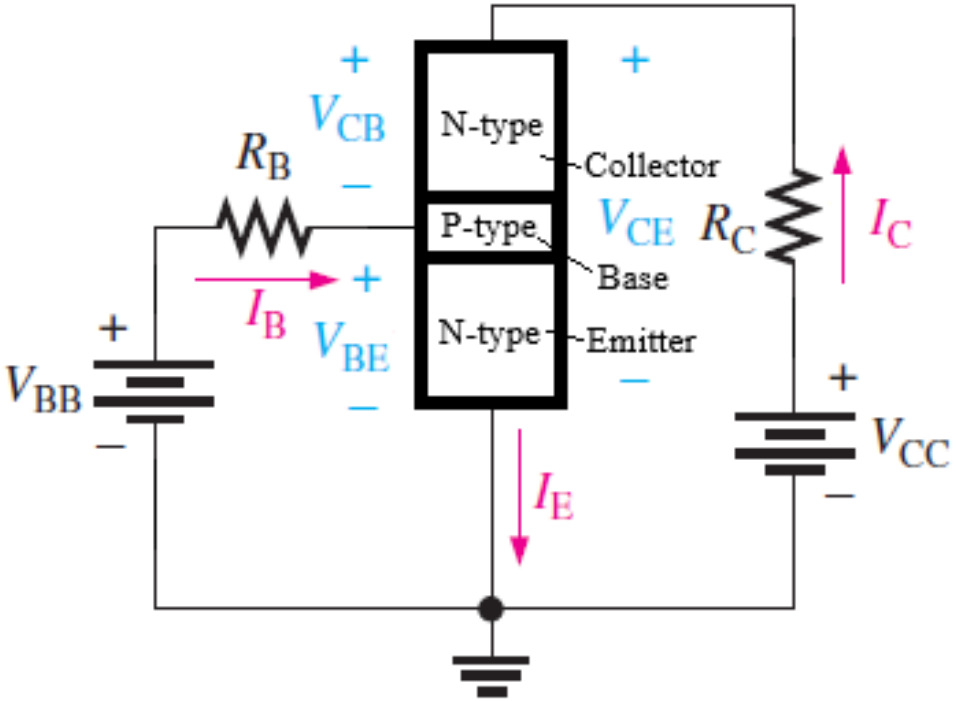


- Transistor ON
- Closed switch
- Saturation mode

2. Using the Transistor as a Switch (cont.)

- NPN transistor in the common emitter configuration.

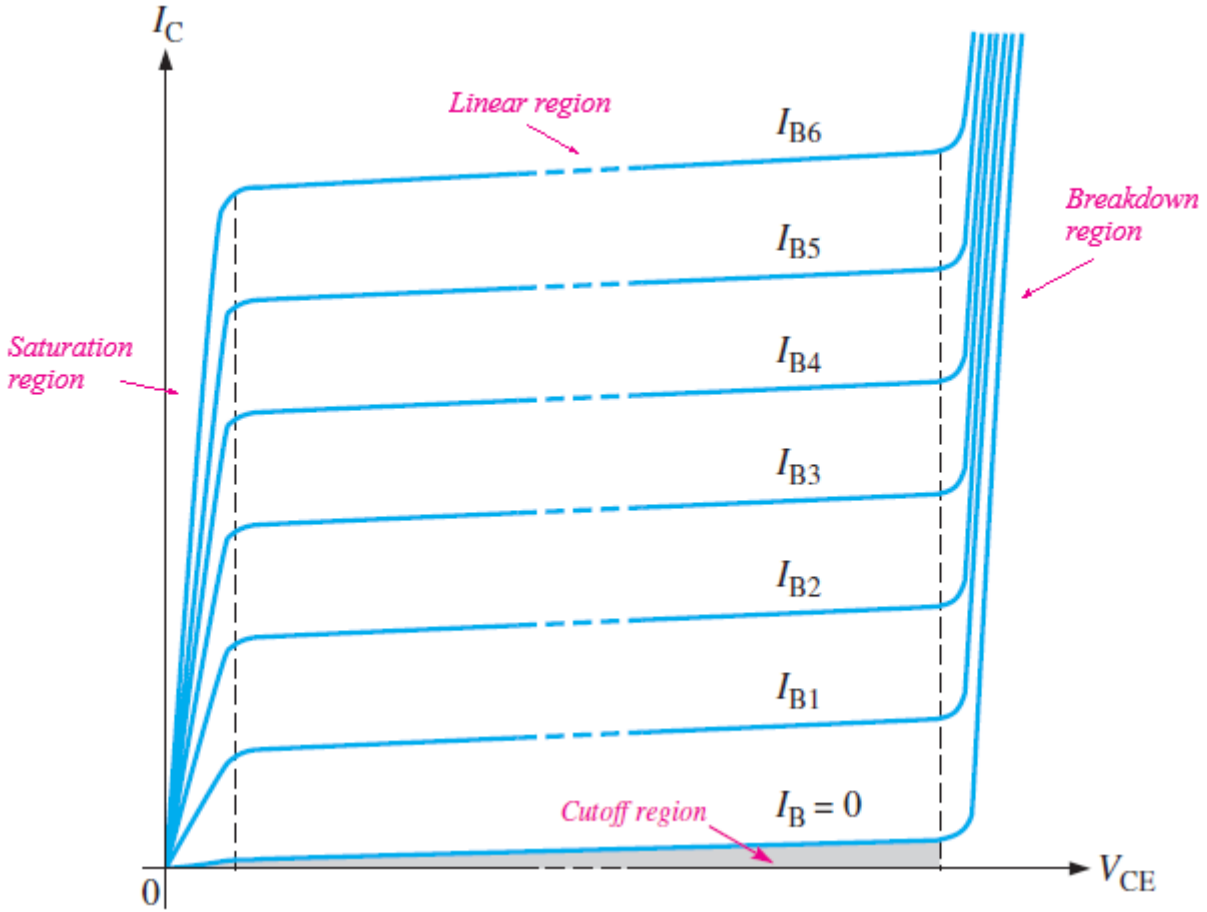
- V_{BB} and R_B provide biasing current to turn on the BJT.
- With I_C and emitter, I_E (as set by V_{CC} and R_C), we observe a voltage drop across CE (V_{CE}).



- To be able to do this efficiently, let's have another look at the output characteristic curves of a common emitter NPN transistor.

3. The Output Current–Voltage Characteristics

- We need to determine the appropriate region for the switching operation of the BJT transistor.
- We look at the graph of the collector-emitter voltage vs. collector current.



3. The Output Current–Voltage Characteristics

For the **cut-off region**, we have:

- I_B = 0, thus I_C = 0 and the whole transistor is OFF.
- V_{BE} < 0.7 V.
- BE junction then essentially reverse biased, i.e. open circuit.

For the **active region**, we have:

- V_{BE} = 0.7 V, so the BE junction is forward biased.
- The CB junction is reverse biased.
- I_B > 0 and we have $I_C = \beta I_B$.
- The transistor is ON in the mode typically used for amplification.

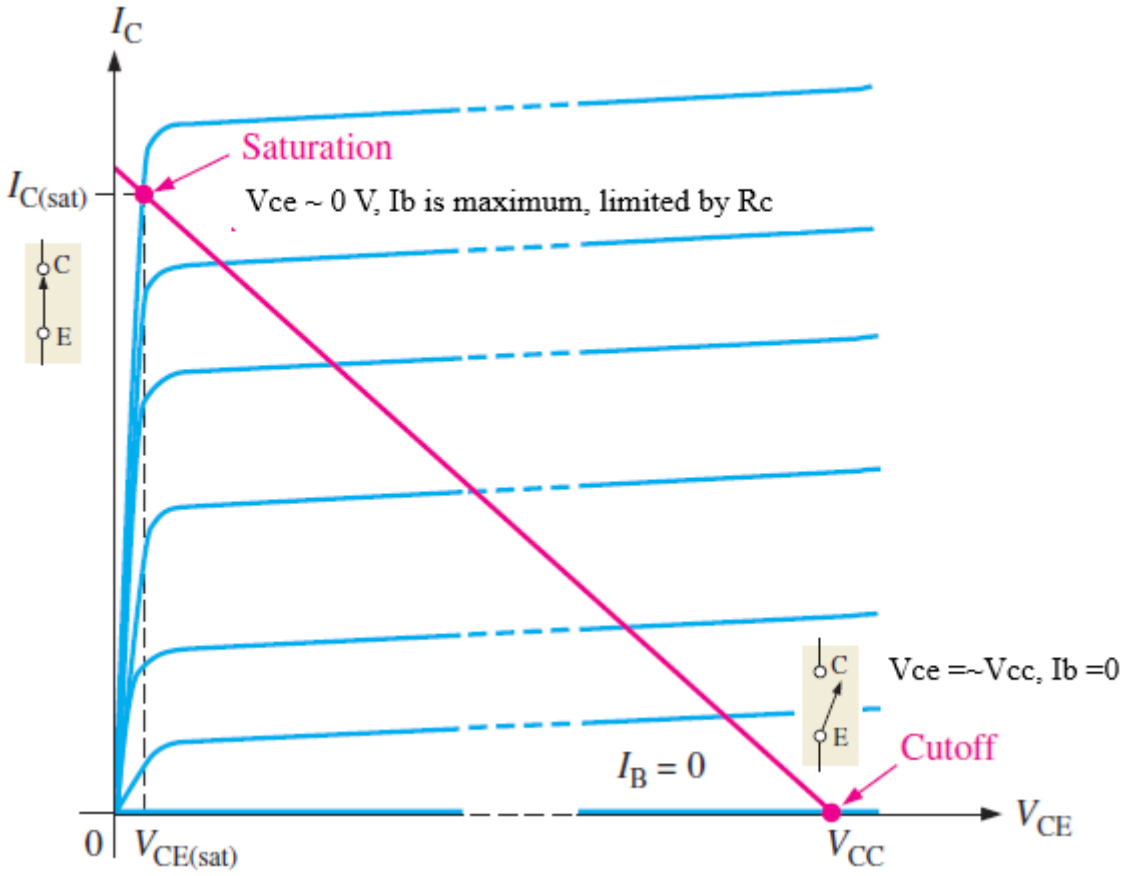
3. The Output Current–Voltage Characteristics

But what is the reason for transistor behaviour in the **saturation region** ? In this region, we would have:

- V_{BE} = 0.7 V so the BE junction is forward biased.
- V_{CE} would be very small i.e. if this is the case, we have V_{CE} ~ 0 V.
- The BC junction will thus be forward biased i.e. both the junctions are forward biased, and transistor appears as a short.
- Region modelled as a constant voltage drop of V_{CE} = 0.2 V.
- The β is smaller than the β value in the active region.

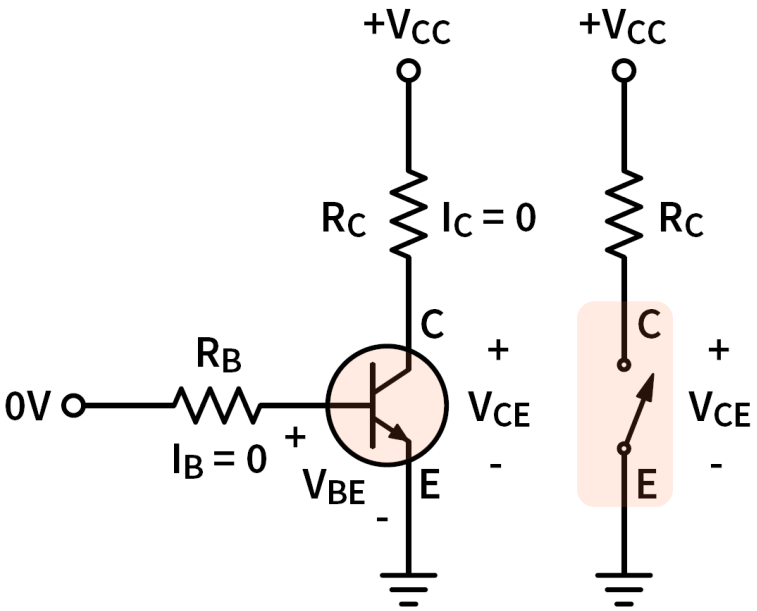
3. The Output Current–Voltage Characteristics

- We need to switch efficiently between the cut-off point and saturation point of operation.
- Saturation point: V_{CE} ~ 0 and I_B is maximum – limited by R_C.



4. BJT Switching Operation

- When BJT as switch is off, considering no leakage current, all of the currents, I_B and I_C are zero.
- Since I_C is zero, the $V_{CE(\text{cutoff})}$, is equal to V_{CC}.



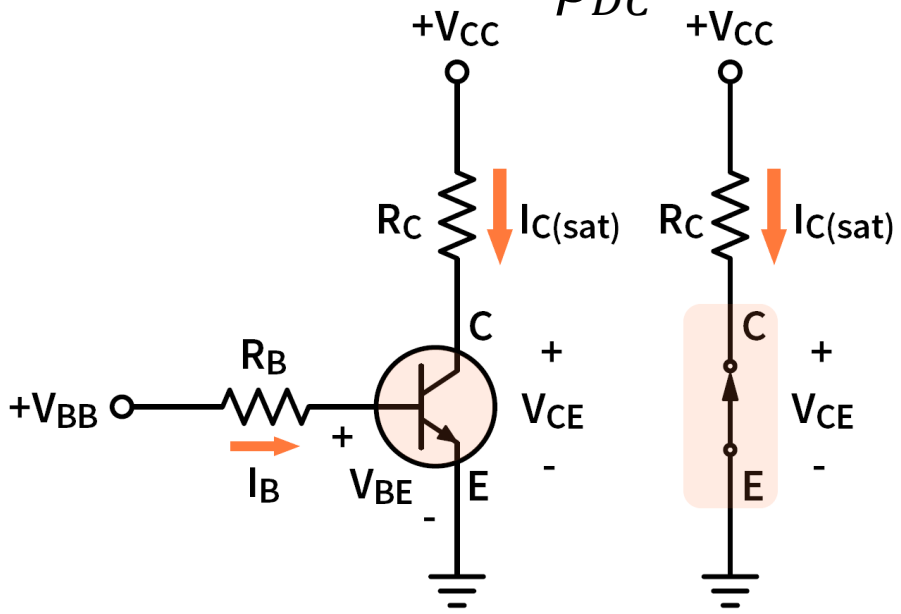
4. BJT Switching Operation (cont.)

- When the BJT switch is on, the saturated collector current is:

$$I_{C(\text{sat})} = \frac{V_{CC} - V_{CE(\text{sat})}}{R_C}$$

- Maintaining saturation, the minimum base current is:

$$I_{B(\text{min})} = \frac{I_{C(\text{sat})}}{\beta_{DC}}$$

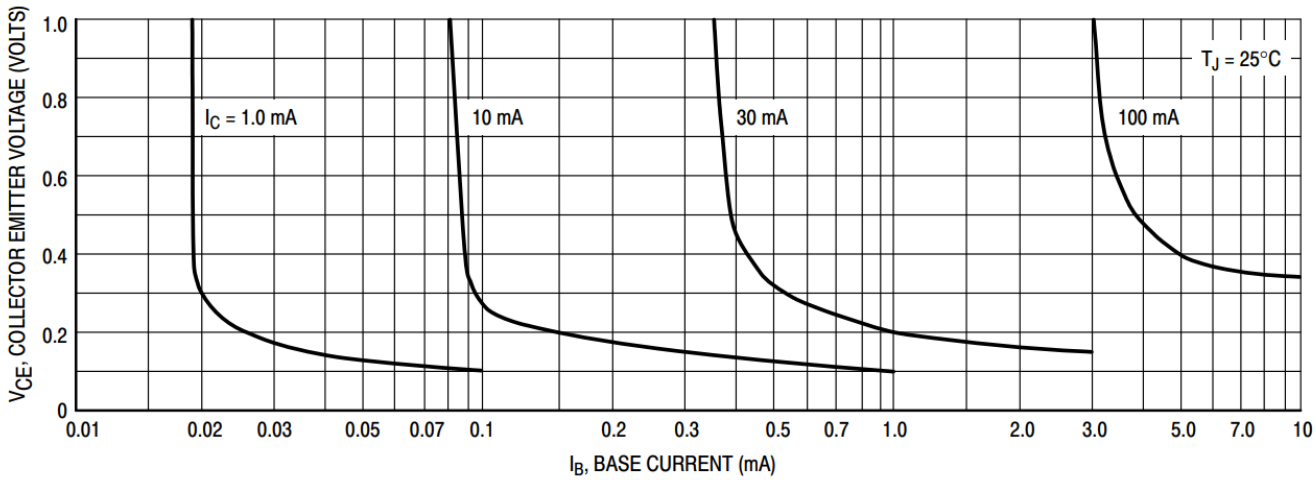


5. What DC Beta (β_{DC}) to Use?

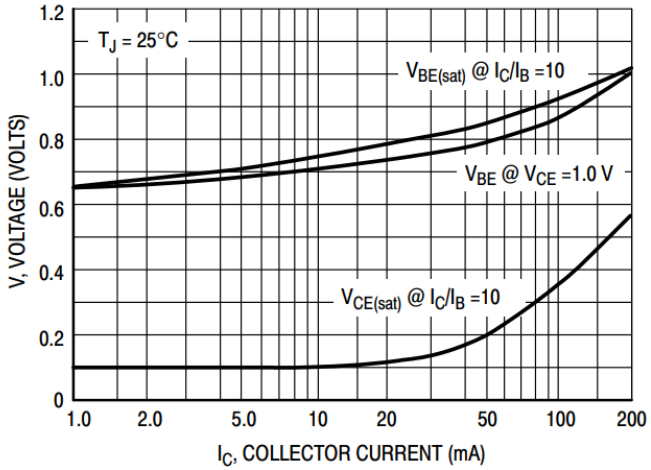
- Knowing $V_{CE(\text{sat})}$, we can calculate $I_{C(\text{sat})}$ then $I_{B(\text{min})}$.
- However, you may wonder, what is the value of β_{DC}?
- To make it easier for you to find out, the clue is you can find β_{DC} on the BJT datasheet.

ON CHARACTERISTICS		Symbol	Min	Max	Unit
DC Current Gain (Note 2)		h_{FE}			–
(I_C = 0.1 mAdc, V_{CE} = 1.0 Vdc)	2N3903		20	–	
	2N3904		40	–	
(I_C = 1.0 mAdc, V_{CE} = 1.0 Vdc)	2N3903		35	–	
	2N3904		70	–	
(I_C = 10 mAdc, V_{CE} = 1.0 Vdc)	2N3903		50	150	
	2N3904		100	300	
(I_C = 50 mAdc, V_{CE} = 1.0 Vdc)	2N3903		30	–	
	2N3904		60	–	
(I_C = 100 mAdc, V_{CE} = 1.0 Vdc)	2N3903		15	–	
	2N3904		30	–	

Characteristic	Symbol	Min	Max	Unit
Collector – Emitter Saturation Voltage (Note 2) (I_C = 10 mAdc, I_B = 1.0 mAdc) (I_C = 50 mAdc, I_B = 5.0 mAdc	$V_{CE(sat)}$	 – –	 0.2 0.3	Vdc
Base – Emitter Saturation Voltage (Note 2) (I_C = 10 mAdc, I_B = 1.0 mAdc) (I_C = 50 mAdc, I_B = 5.0 mAdc)	$V_{BE(sat)}$	 0.65 –	 0.85 0.95	Vdc



Collector Saturation Region



“ON” Voltages

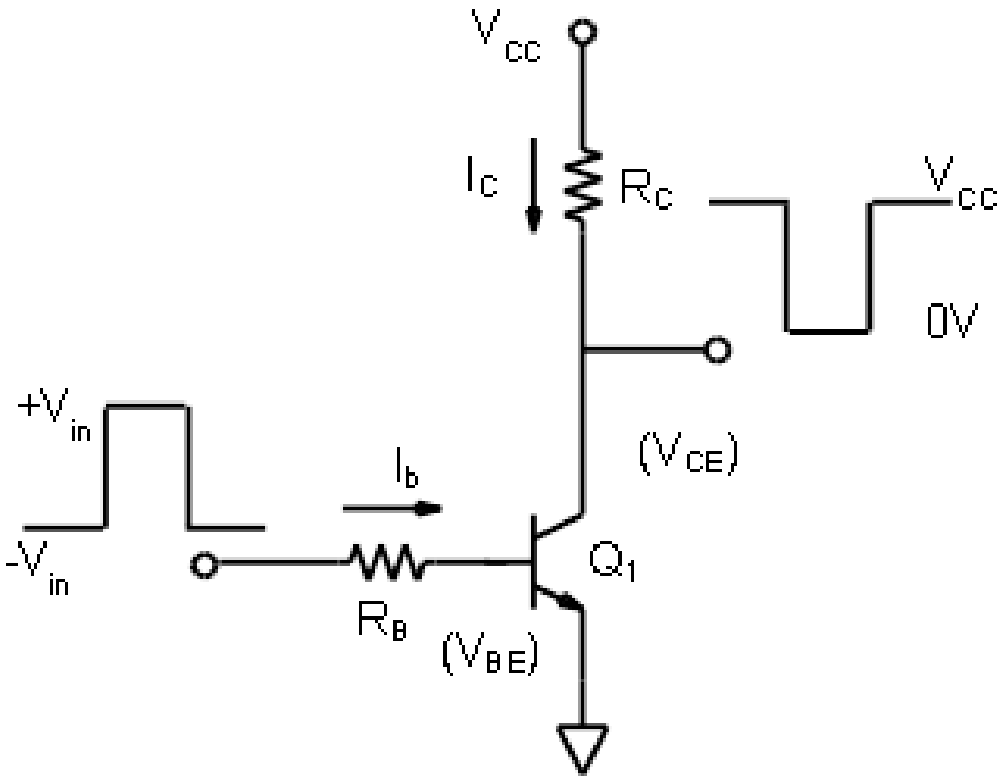
5. What DC Beta to Use? (cont.)

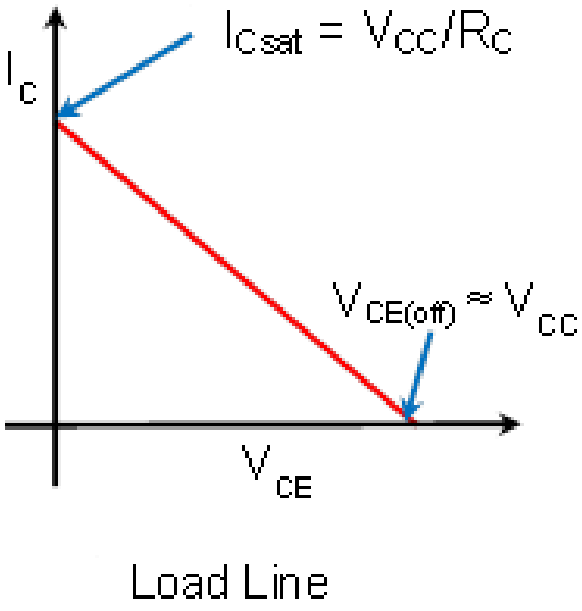
- Since DC beta (β_{DC}) is equivalent to the hybrid parameter (h_{FE}), we look it up in the datasheet.
- But, h_{FE} in the datasheet is the current gain of a BJT that is operating as an amplifier or in the active region.
- We require the gain of the BJT for the switching circuit.
- The β_{DC} used in the saturation region for the 2N3904 is 10. Notice that the I_C/I_B ratio is always 10.
- The guaranteed value of β_{DC} is 10 for it to operate in the saturation region.
- Some may use 20 but β_{DC} is not constant, and it changes with the junction temperature. So, it's better to set β_{DC} at 10.

6. Load Line of BJT Switching Circuit

- When the BJT is in cut-off, this state is like an open switch.

$$V_{CE} = V_{CC} \quad \text{and} \quad I_C = 0\ \text{A}$$

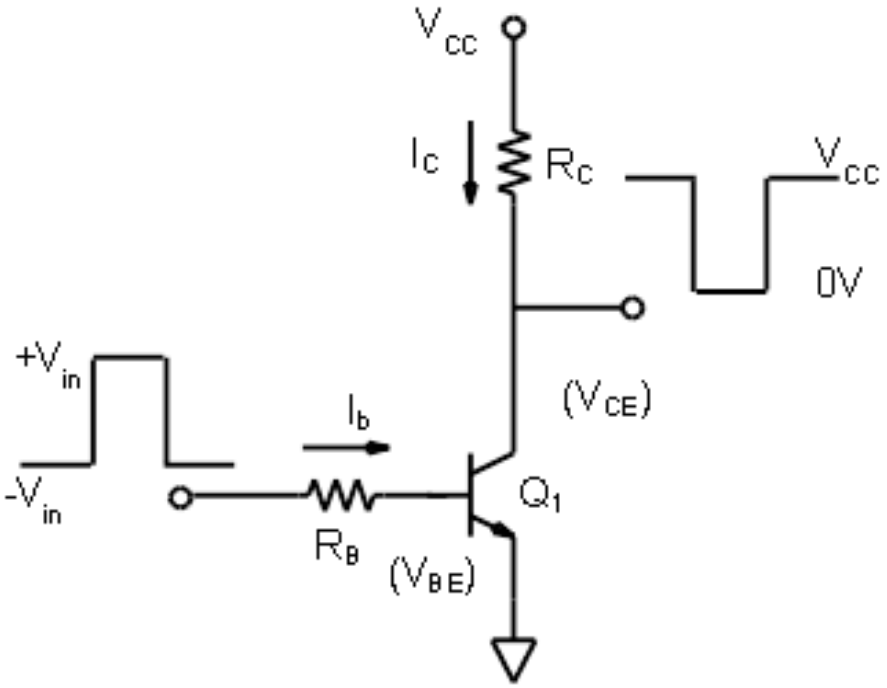


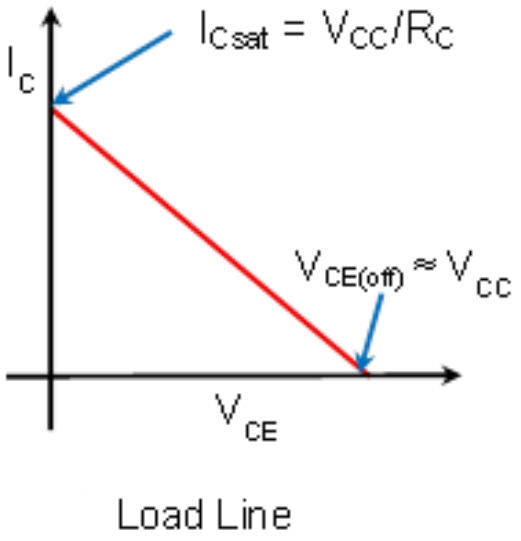


6. Load Line of BJT Switching

- When the input equals $+V_{in}$, the transistor is driven into saturation, and this state is like a closed switch connecting the bottom of R_C to ground.

$$V_{CE} \sim 0\ \text{V} \quad \text{and} \quad I_{C(\text{sat})} = V_{CC}/R_C$$





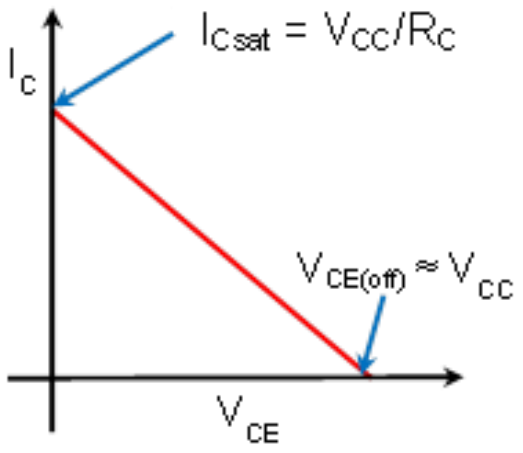
6. Load Line of BJT Switching Circuit (cont.)

The characteristics for a BJT switch assume that:

- The V_{in} is low enough to drive the transistor into cut-off.
- The $+V_{in}$ must produce enough base current through R_B to drive the transistor into saturation.
- The transistor is an ideal component.

These conditions can be assured by designing the circuit so that:

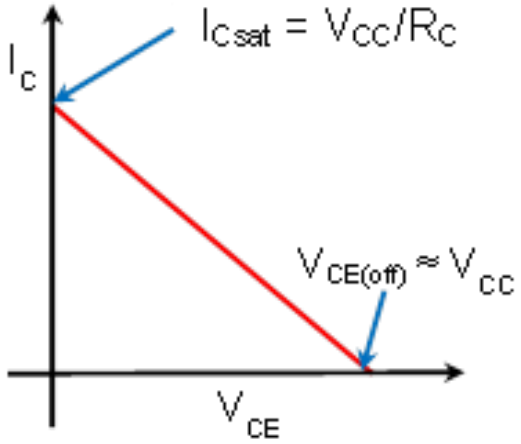
1. The input voltage, $V_{in} = V_{BE}$.
2. The voltages at the input: $+V_{in} = V_{BE} + I_B R_B$ (V_{CC} is a good maximum).
3. The currents, $I_B > I_{C(\text{sat})}/\beta$.



Load Line

6. Load Line of BJT Switching Circuit (cont.)

- Condition 1 guarantees that the circuit is driven into the cut-off region by the input.
- Conditions 2 and 3 assure that the transistor will be driven into the saturation region.

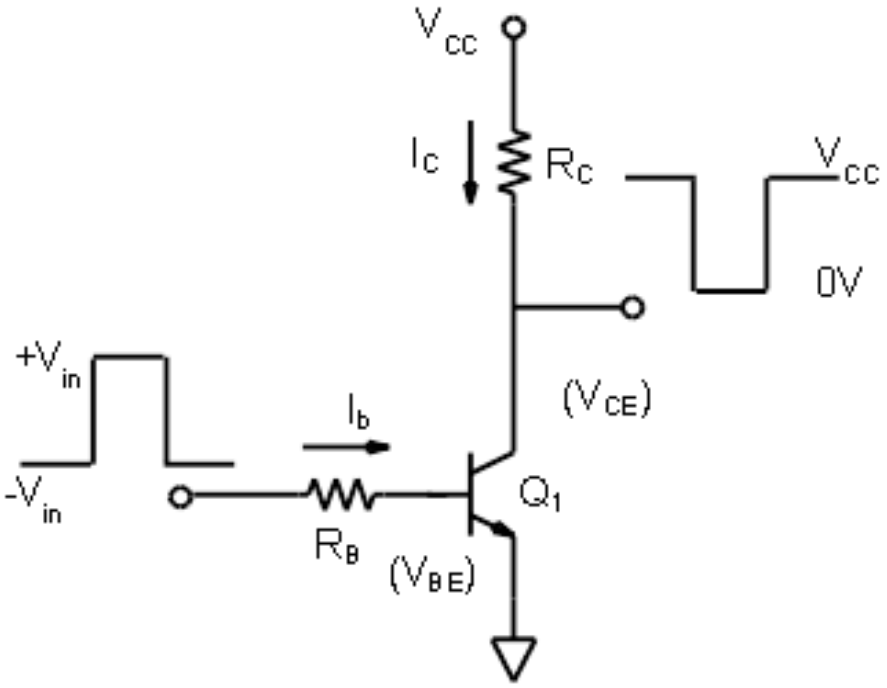


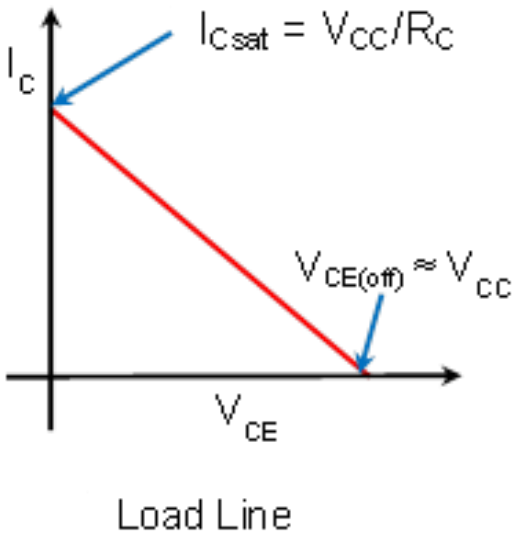
Load Line

- An actual BJT switch differs from the ideal switch in several aspects.
- In practice, even in cut-off there is some leakage current through the transistor.
- Also, in saturation, there is always some voltage dropped across the transistor's internal resistance.

6. Load Line of BJT Switching Circuit (cont.)

- Typically, this will be between 0.2 and 0.4 V in saturation depending on the collector current and size of the device.
- These variations from the ideal are generally minor with a properly sized device, so we can assume near ideal conditions when analysing or designing a BJT switch circuit.





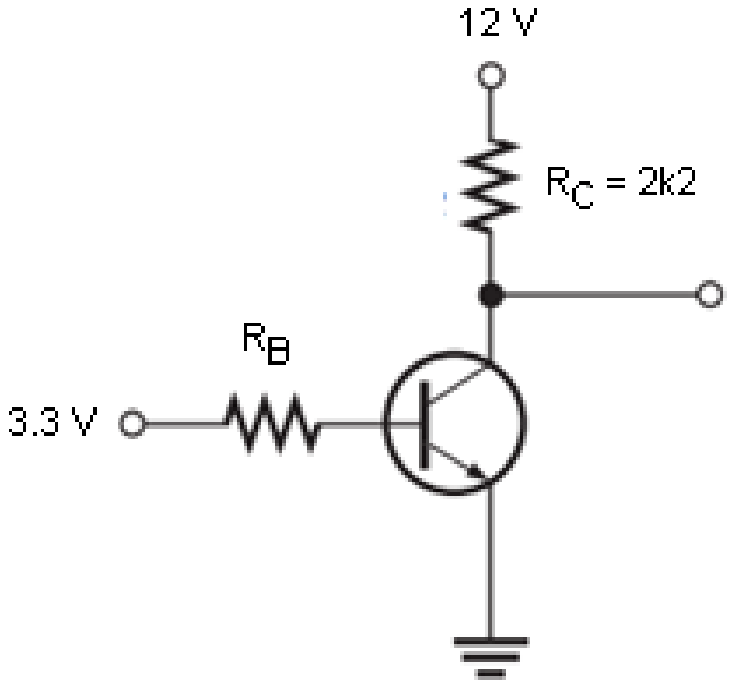
Load Line

Example 1 – BJT Switching Circuit Biasing

For the BJT circuit as shown in the figure given below, design it for switching application.

a. What minimum value of I_B is required to saturate this transistor if β_{DC} is 150? Neglect $V_{CE(\text{sat})}$. [4 marks]

b. Describe briefly the significant of this current. Explain what happens when you further increase this current. [2 marks]



Answer

a. Since $V_{CE(\text{sat})}$ is neglected (assumed to be 0 V), the saturation current at the collector is found from:

$$I_{C(\text{sat})} = \frac{V_{CC}}{R_C} = \frac{12\ \text{V}}{2.2\ \text{k}\Omega} = 5.45\ \text{mA}$$

As a result, the minimum current at the base of transistor is:

$$I_{B(\text{min})} = \frac{I_{C(\text{sat})}}{\beta_{DC}} = \frac{5.45\ \text{mA}}{150} = 36.3\ \mu\text{A}$$

This is the value of I_B necessary to drive the transistor to the point of saturation.

b. Any further increase in I_B will ensure the transistor remains in saturation, but there cannot be any further increase in I_C.

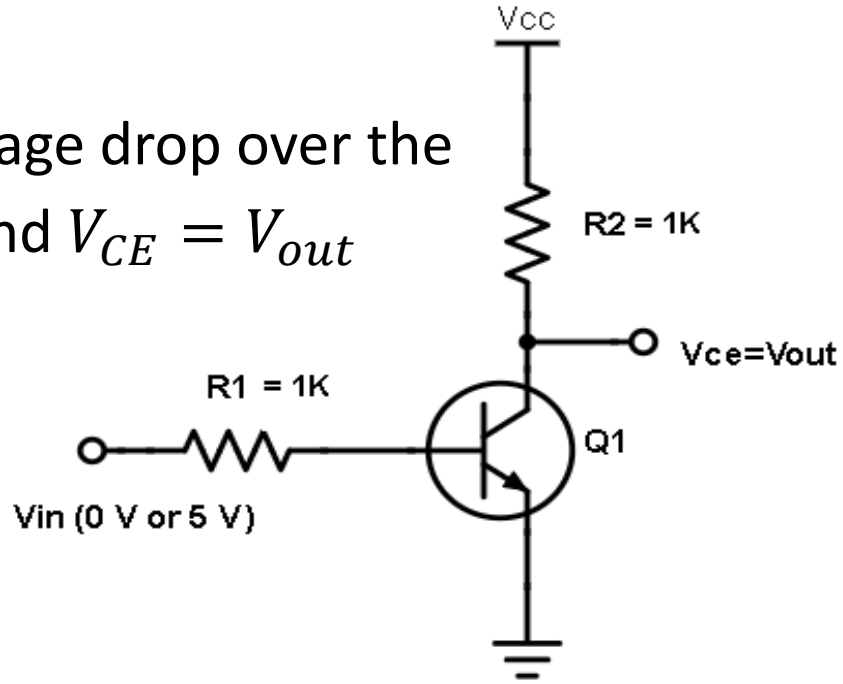
7. Design with Common Emitter Configuration

Consider a common emitter BJT configuration given below.

In the given circuit:

Step 1. Assume initially V_{in} ~ 0 V (OFF)

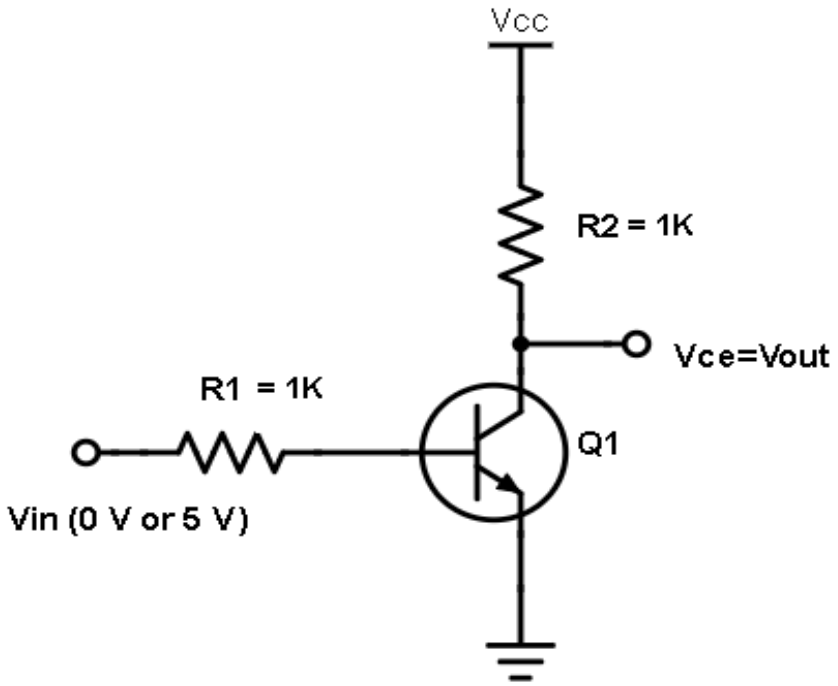
- So, that V_{BE} < 0.7 V, as a result the transistor is OFF with $I_B = I_C = 0$.
- If $I_B = 0$, then there is no voltage drop over the resistor at the collector (R_2) and $V_{CE} = V_{out}$ which is ~ V_{CC}.
- The transistor is an open circuit as it is OFF -> *cut-off*.



7. Design with Common Emitter Configuration (cont.)

Step 2. Now, increase V_{in} to produce V_{BE} ~ 0.7 V.

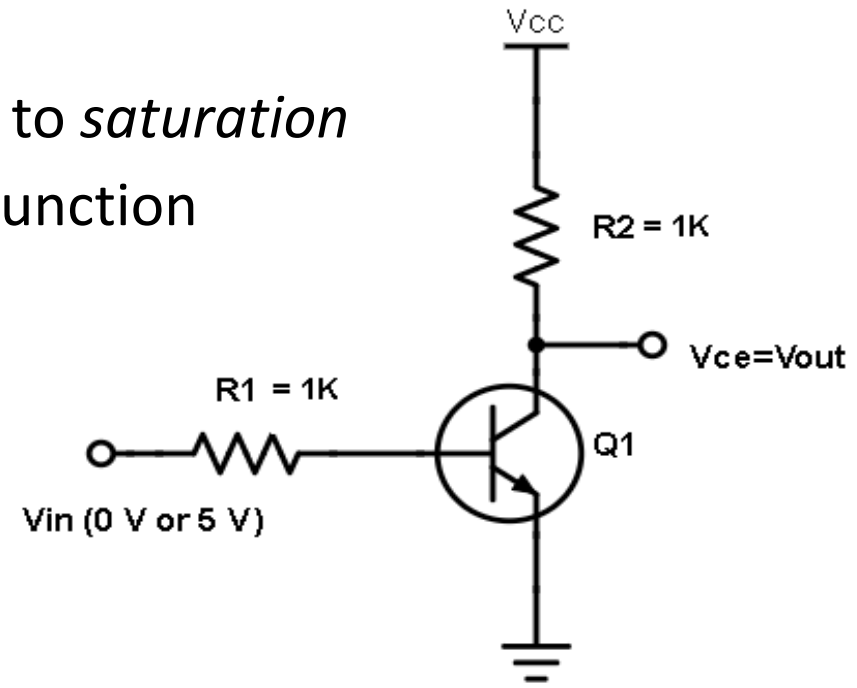
- As I_B increases, I_C will rapidly increase as $I_C = \beta I_B$ in *active region.*
- The current I_C will eventually be limited by the value of collector resistor (R_2).



7. Design with Common Emitter Configuration (cont.)

Step 3. Keep on increasing I_C

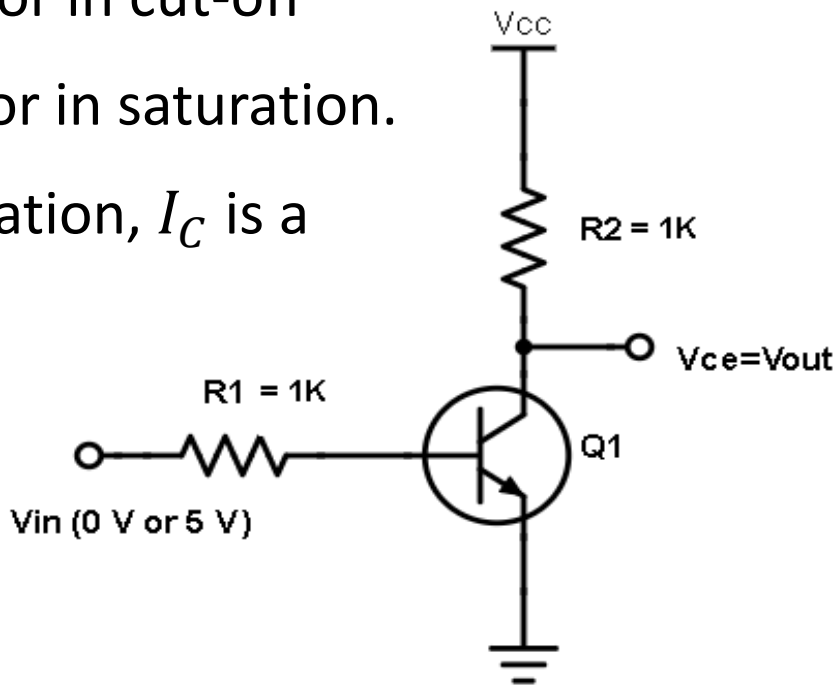
- As I_C increases, the voltage drop over the resistor at the collector (R_2) will increase -> the voltage drop V_{CE} will decrease
- This will eventually decrease to *saturation level* (V_{CE} ~ 0.2 V) as the BC junction becomes forward biased.



7. Design with Common Emitter Configuration (cont.)

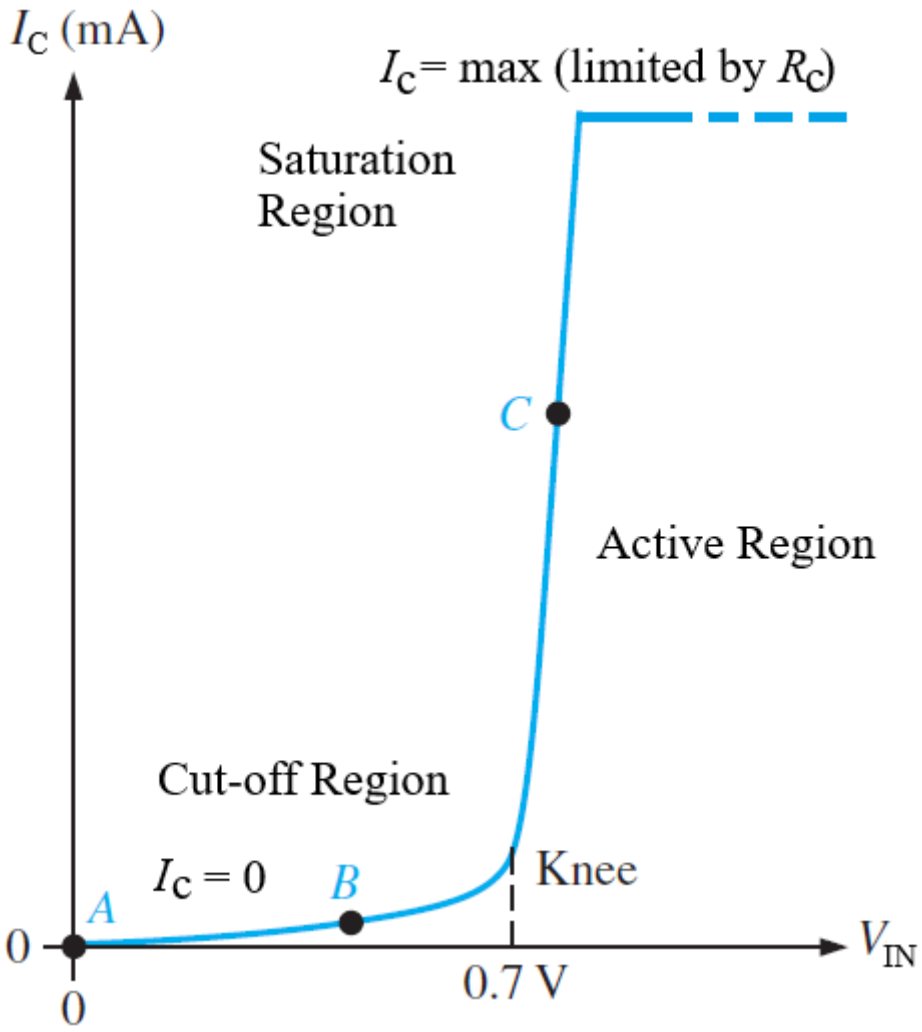
Step 4. For switch operation, we want to use a binary signal level on V_{in}:

- V_{in} = LO must put transistor in cut-off
- V_{in} = HI must put transistor in saturation.
- Since transistor is in saturation, I_C is a maximum.



7. Design with Common Emitter Configuration (cont.)

Step 5. Plot a typical graph of V_{in} vs. I_C



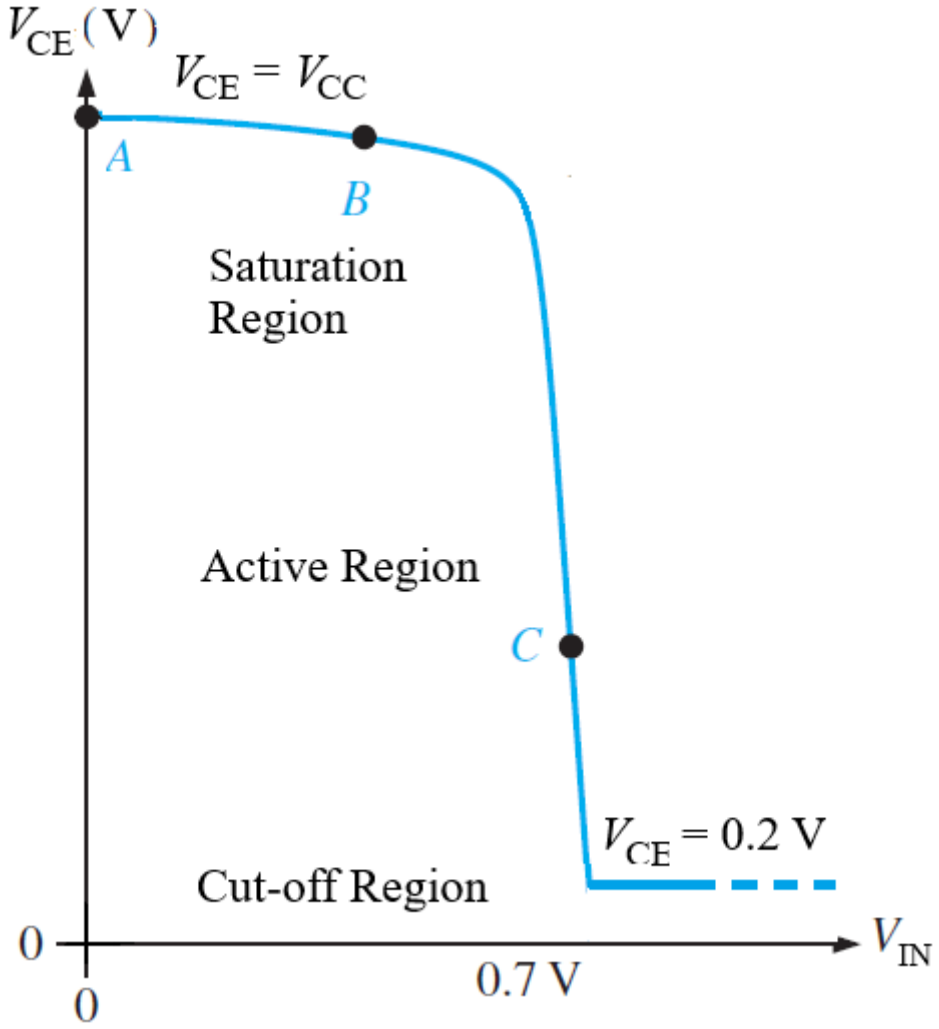
7. Design with Common Emitter Configuration (cont.)

Step 5. Plot a typical graph of V_{in} vs. I_C

- When the transistor is turned on at around 600 mV of the input voltage, the collector current starts to flow.
- There is a limit on the collector current is set by the value of the resistor at the collector (R_2) in the circuit.
- Region between the turn on and the maximum point is called active region.

7. Design with Common Emitter Configuration (cont.)

Step 6. Plot a typical graph of V_{in} vs V_{CE}.



7. Design with Common Emitter Configuration (cont.)

Step 6. Plot a typical graph of V_{in} vs V_{CE} (cont..)

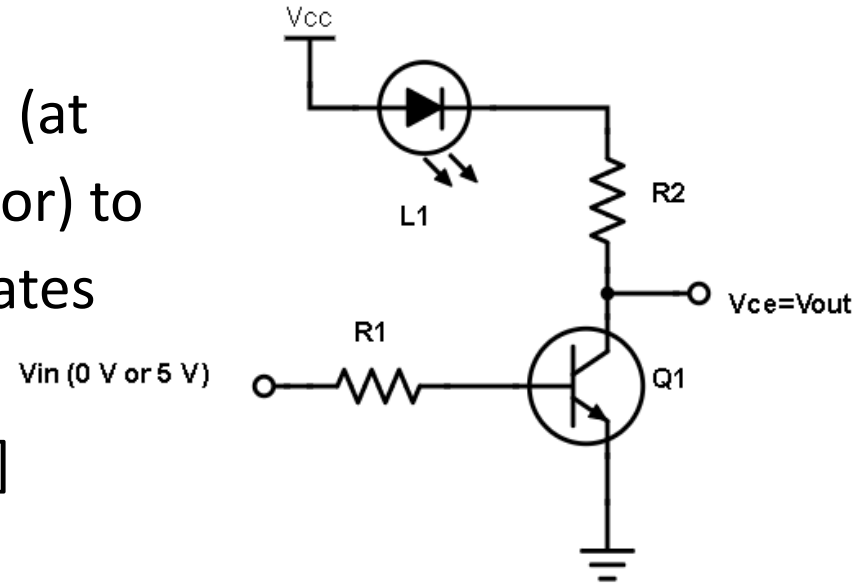
- When the BJT transistor is off, V_{CE} is found to be equal to V_{CC}.
- When the transistor is on, it is held to a value of 0.2 V.
- Notice the **inverter** behaviour of this circuit i.e. the output voltage is the inverse voltage of the input.

Example 2 – BJT Switching Circuit

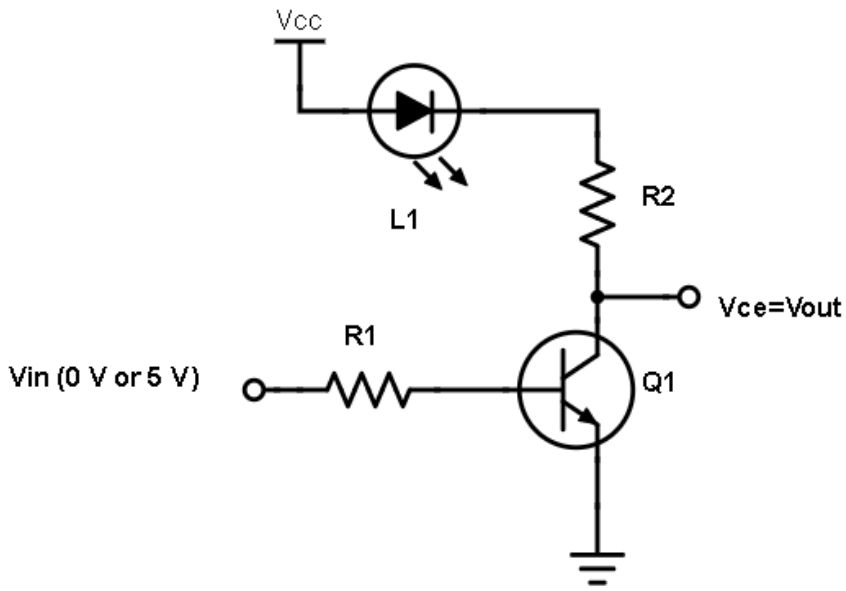
The circuit below must be used to switch on a LED when a 5 V logic signal is used as the input voltage on the base of the transistor.

Calculate sensible values for R_1 (at the base) and R_2 (at the collector) to ensure that the transistor operates effectively as a switch.

[6 marks]



- The circuit is to be supplied with a V_{CC} = 12 V and saturation level voltage across the collector-emitter junction of the BJT transistor Q_1, V_{CE} = 0.2 V.



- The LED needs 20 mA for operation with optimum brightness and has a voltage drop of V_D = 1.8 V over it when forward biased (e.g. a red LED).
- You will be using a microcontroller to provide the V_{in} signal and the output of the microcontroller can provide a maximum current of 8 mA.

Answer

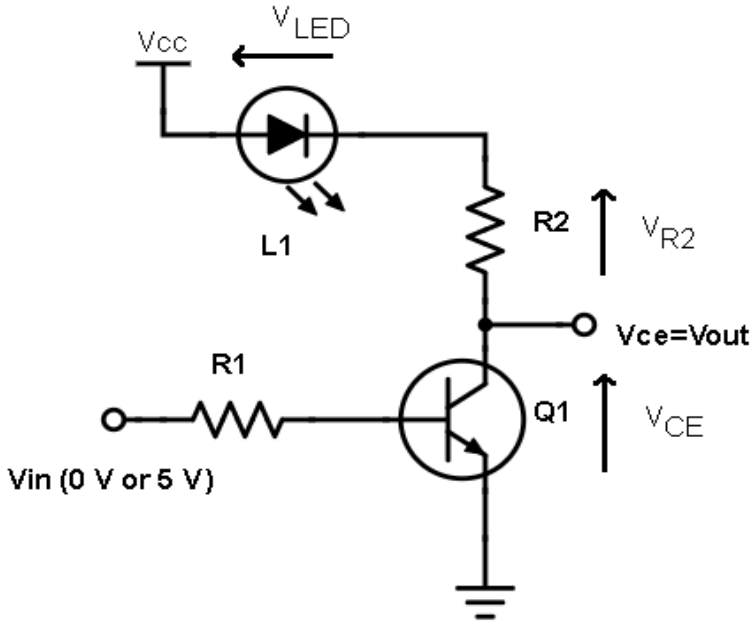
For the CE loop we can write a KVL for the saturation case:

$$V_{CC} - V_D - I_C R_2 - V_{CE} = 0$$

- Entering values into the equation:

$$12\ \text{V} - 1.8\ \text{V} - (20\ \text{mA})(R_2) - 0.2\ \text{V} = 0$$

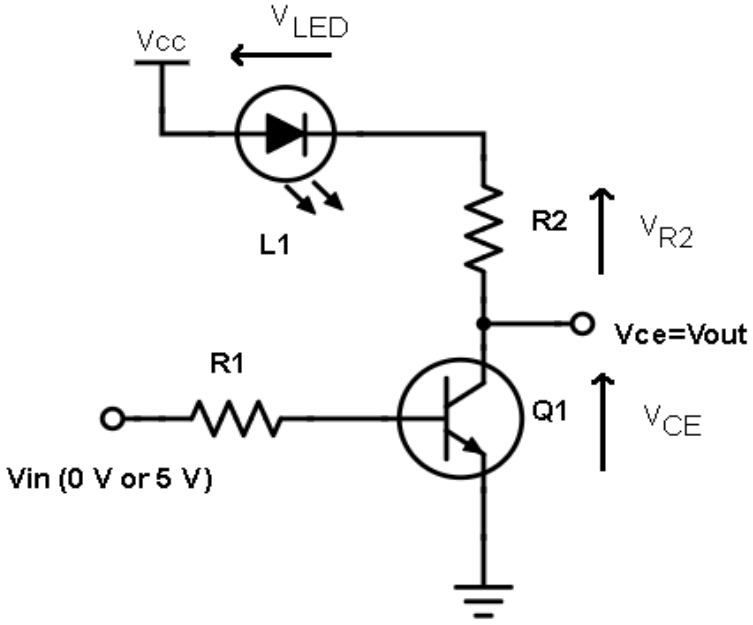
- Solve for the resistor at the collector (R_2) to find R_2 = 500 Ω.
- Do we get a 500 Ω resistor?
  -> choose 470 Ω resistor from the E12 resistor series.



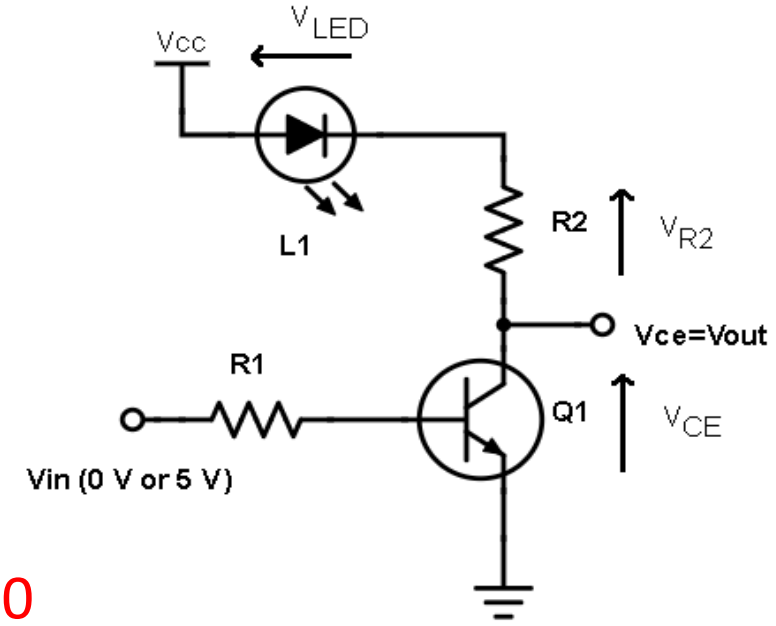
- Now, need to find the base current I_B that will be sufficient to generate this collector current we have: $I_C = \beta I_B$ with β typically 100 to 500 in the active region.

- But we are operating in the saturation region where β is considerably lower – thus take β = 50.
- We would then need a base current of:

$$I_B = \frac{I_C}{\beta} = \frac{20\ \text{mA}}{50} = 0.4\ \text{mA}$$



- The calculated value of I_B = 0.4 mA represents the minimum value of base current that would be able to drive the transistor into saturation.
- However, when we use a transistor in a switch configuration, we would typically overdrive the transistor to ensure that we are in saturation.



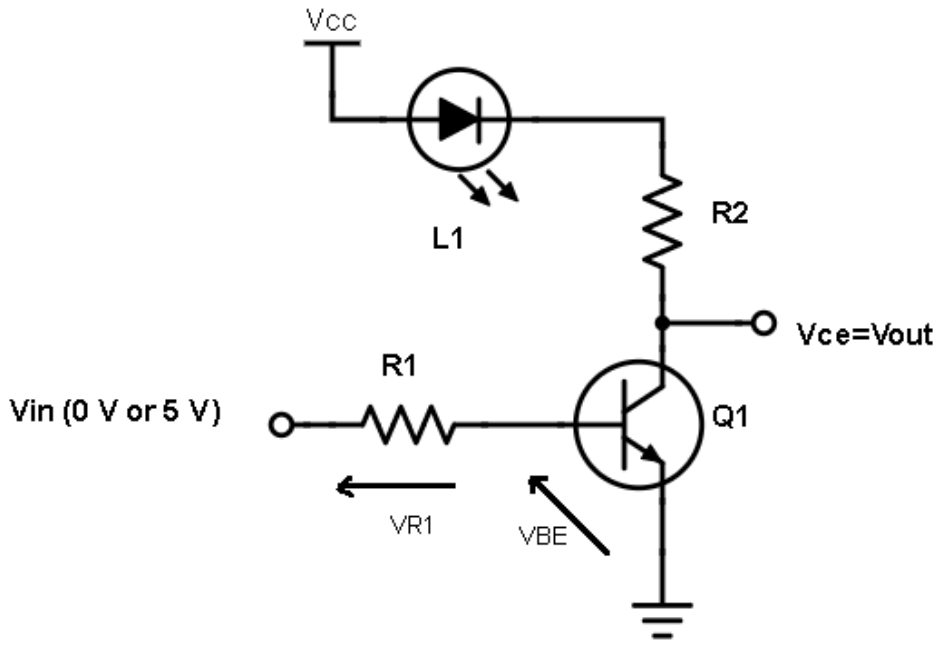
- A typical overdrive factor of 10 x can be used.
- The base current to aim for would thus be I_B = 4 mA.

- Solve for the resistor at the base (R_1) by looking at the BE current loop:

  $V_{in} - I_{R1}R_1 - V_{BE} = 5\ \text{V} - (4\ \text{mA})R_1 - 0.7\ \text{V} = 0$

- Thus $R_1 \approx 1.1\ \text{k}\Omega$

- This will ensure cut-off and saturation behaviour.
- I_B will be within the output capability of the microcontroller.

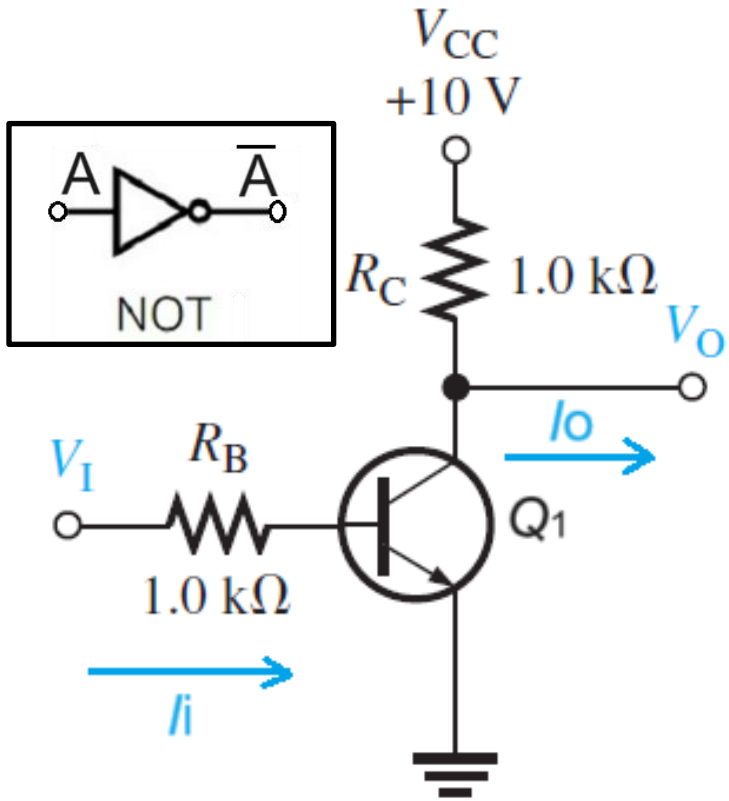


8. BJT Switching Application for Logic Devices

- Use BJT to design and construct logic gates.
- For logic gate design, like BJT switching applications, there are two states of operation:
  - Saturation, or
  - Off.
- The voltages and resistors are picked -> the above conditions hold.
- In short, the transistor now behaves as a switch.

Logic Gates Using BJT

- Consider the following BJT's NOT gate circuit (V_{CC} = 10 V, R_B = 1 kΩ, R_C = 1 kΩ, and V_{BE} = 0.7 V).



- Let.

Voltage (Volt)	Logic Gate
10	1
0	0

- Thus, the conditions and states of the circuit are:

Vi (Volt)	Vi State	Q1 State	Vo (Volt)	Vo State
0	0	OFF	10	1
10	1	SAT	0.2	0

- The circuit performs the NOT function -> NOT logic gate.

Note:

- The current at the input is:

$$I_B = \frac{V_i - V_{BE}}{R_i} = \frac{10\ \text{V} - 0.7\ \text{V}}{1\ \text{k}\Omega} = 9.3\ \text{mA}$$

- If we assume the transistor is :

$$I_C = \beta I_i = (100)(9.3\ \text{mA}) = 930\ \text{mA}$$

- Thus

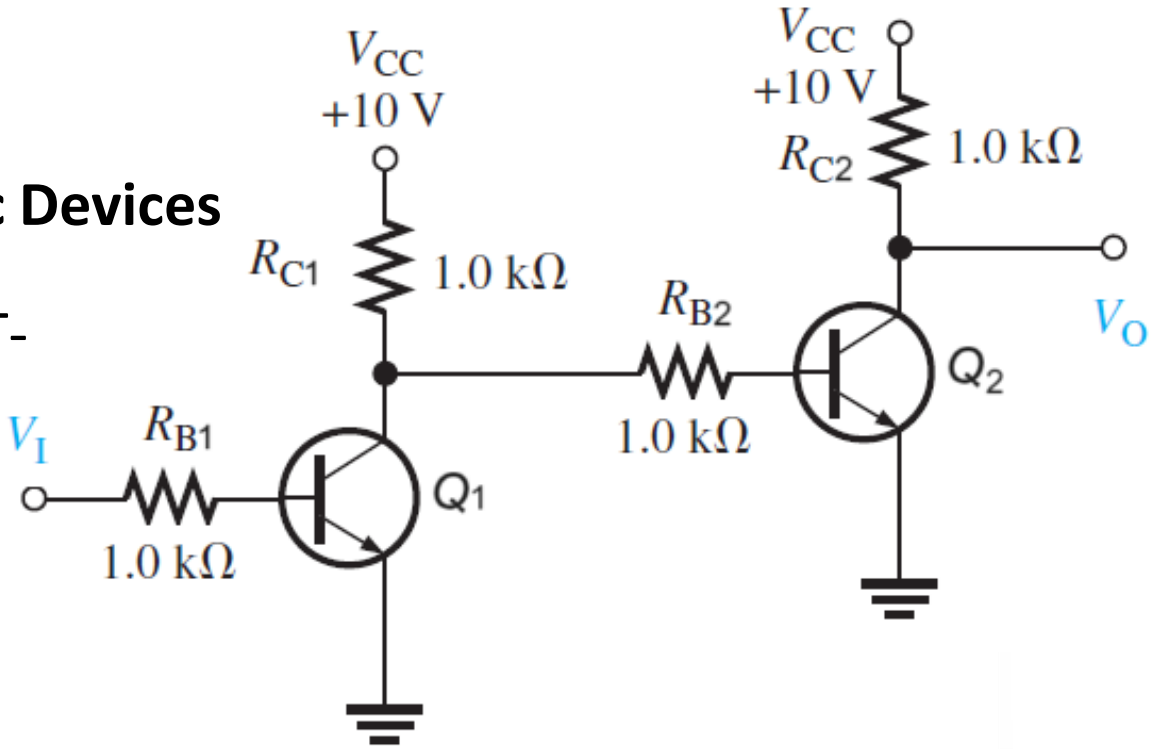
$$V_o = V_{CC} - I_C R_C = 10 - (930\ \text{mA})(1\text{k}\Omega)$$
$$= -920\ \text{V (saturated)}$$

- The current at the output is:

$$I_C = \frac{V_{CC} - V_{CE(\text{sat})}}{R_C} = \frac{10\ \text{V} - 0.2\ \text{V}}{1\ \text{k}\Omega} = 9.8\ \text{mA}$$

Design of BJT as Logic Devices

- Consider BJT's NOT-NOT gate circuit ($V_{BE(\text{on})} = 0.7$ V; $V_{CE(\text{sat})} = 0.2$ V; $\beta = 100$).



- The conditions and states of the circuit are listed below.

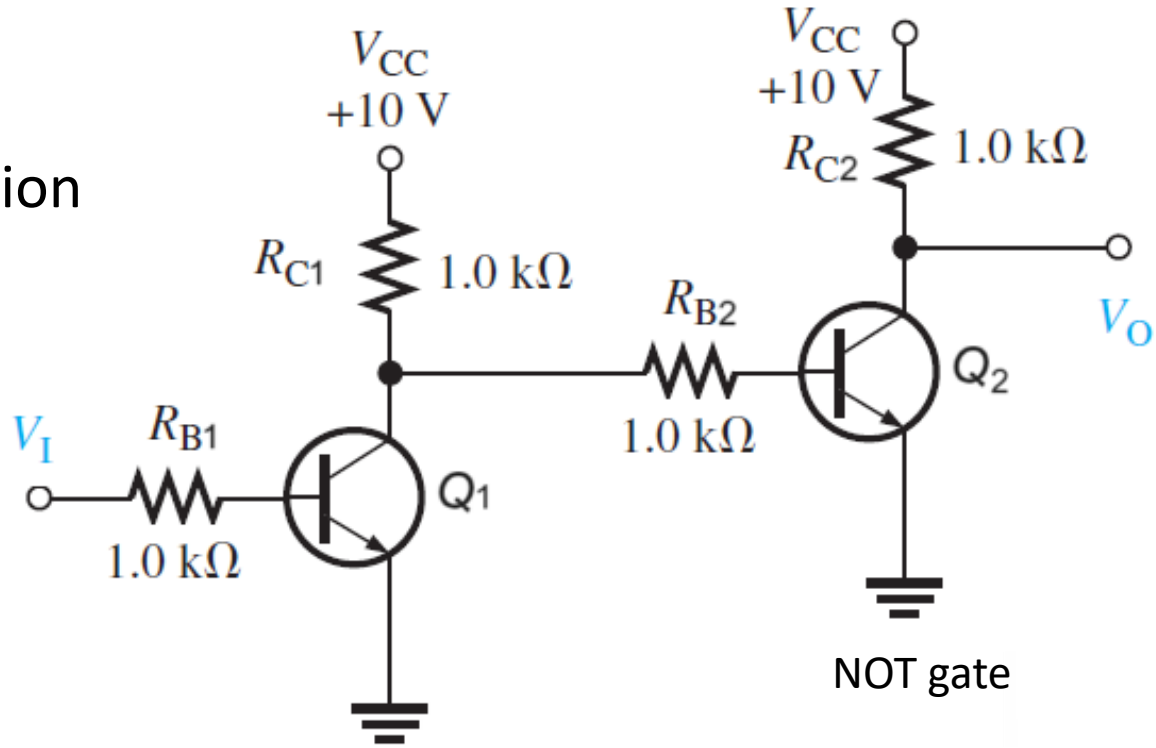
V_i (Volt)	Q_1 State	V_{C1} (Volt)	Q_2 State	$V_{C2} = V_O$ (Volt)
0	OFF	10	SAT	0.2
10	SAT	0.2	OFF	10

- Assuming high: 8 V - 10 V and low: 0 V - 1 V, thus:

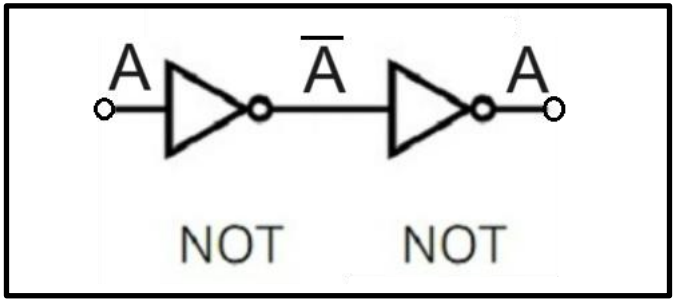
Input	Output
0	0
1	1

Note:

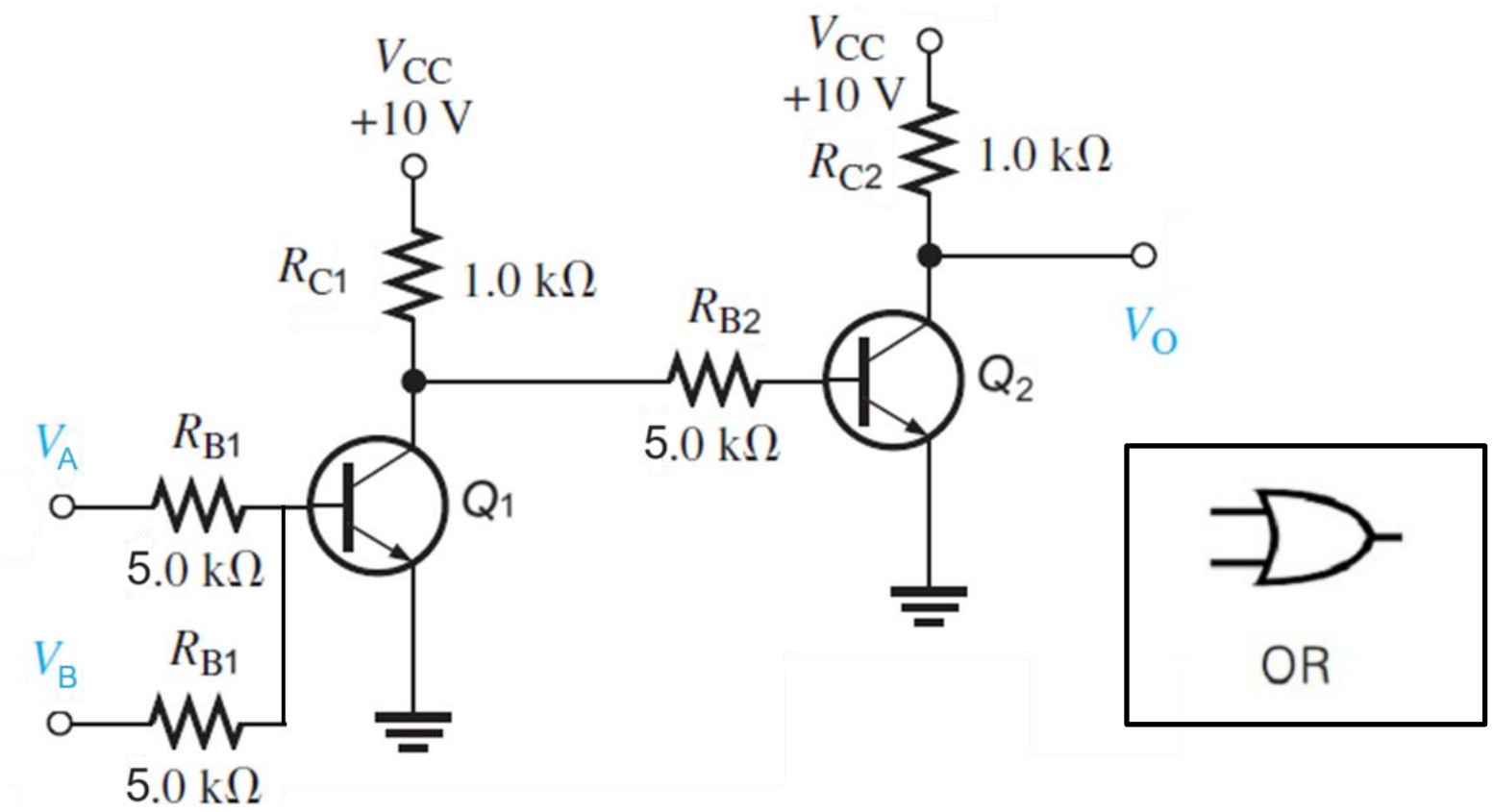
- The overall operation of the circuit is as shown below.



- Thus, the logic gate is realised as outlined below.



- Consider two BJTs in series as OR gate circuit given below ($V_{BE(\text{on})} = 0.7\ V; \beta = 100$).
- Two inputs i.e. V_A and V_B.



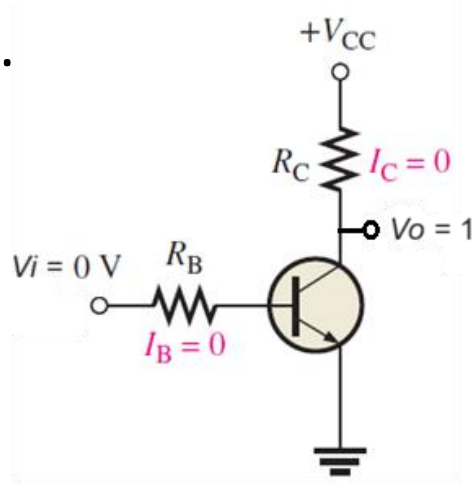
- The conditions and states of the circuit are listed below:

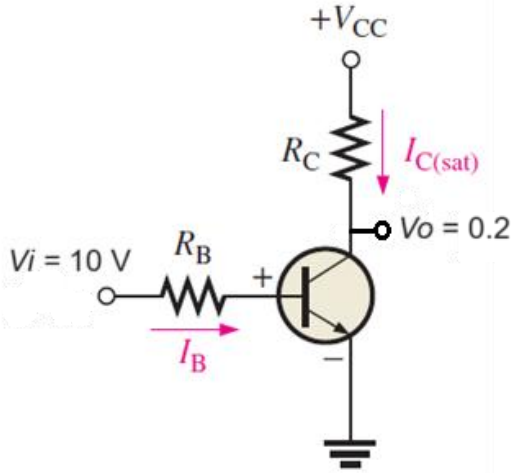
V_A (Volt)	V_B (Volt)	Q_1 State	Q_2 State	V_O (Volt)
0	0	OFF	SAT	0.2
0	10	SAT	OFF	10
10	0	SAT	OFF	10
10	10	SAT	OFF	10

- The logic function is shown below. This is the operation of an OR logic gate.

A	B	Z
0	0	0
0	1	1
1	0	1
1	1	1

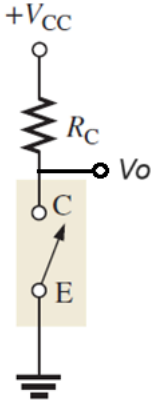
- Transistor as a switch (i.e. knowing V_{CC} = 10 V and $V_{CE(\text{sat})}$ = 0.2 V).

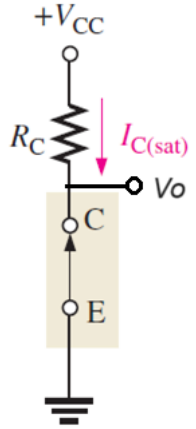




$V_i = 0 \rightarrow Q_1$ (OFF)

$V_i = 10\text{ V} \rightarrow Q_1$ (SAT; ON)



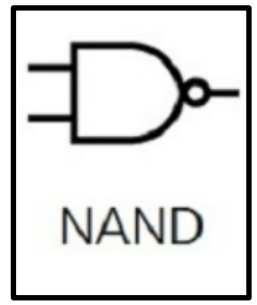


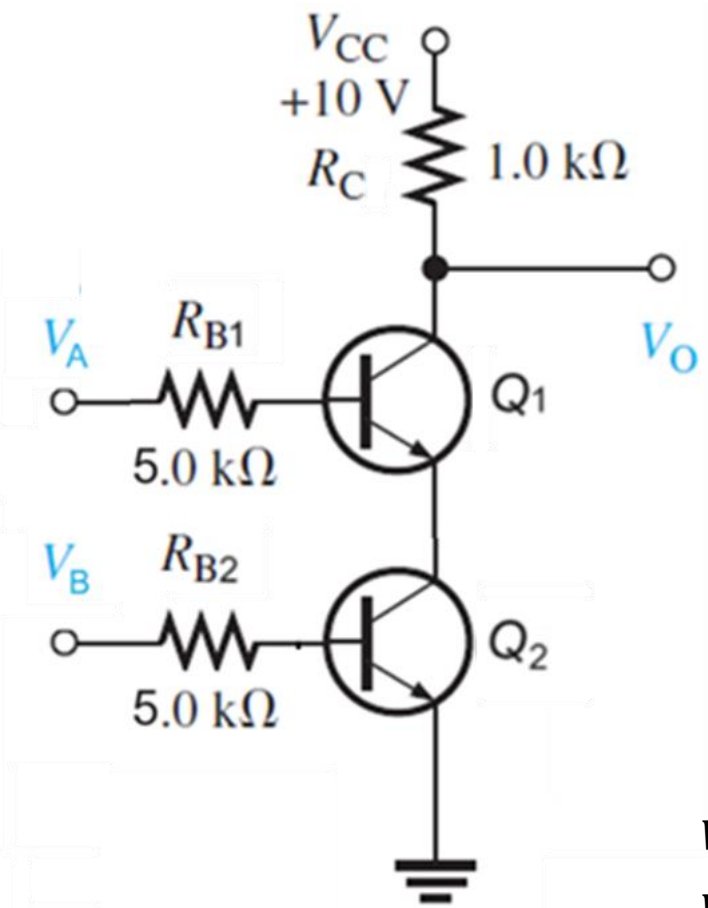
$V_o = V_{CC}$

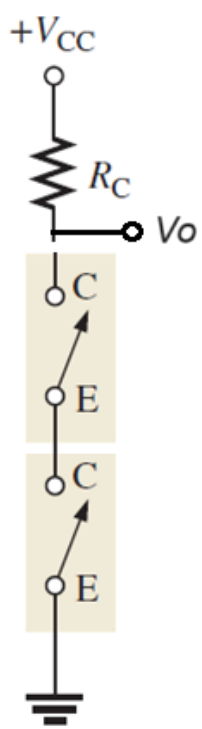
$V_o = 0.2\text{ V} \cong 0\text{ V}$

Consider two BJTs in series as NAND gate circuit:

- Knowing V_{CC} = 10 V and $V_{CE(\text{sat})}$ = 0.2 V.



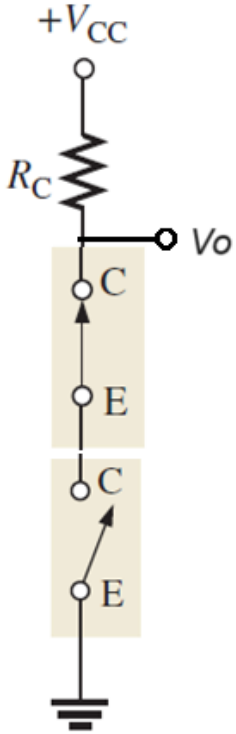




$V_1 = 0$ V

$V_2 = 0$ V

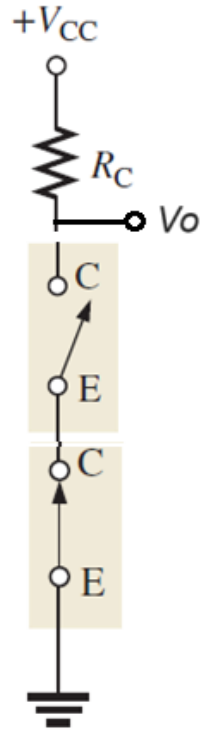
$V_o = 10$ V



$V_1 = 10$ V

$V_2 = 0$ V

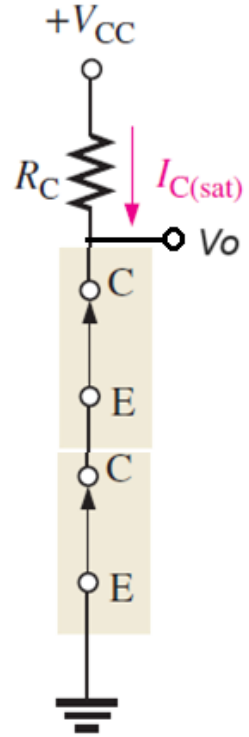
$V_o = 10$ V



$V_1 = 0$ V

$V_2 = 10$ V

$V_o = 10$ V



$V_1 = 10$ V

$V_2 = 10$ V

$V_o = 0$ V

- The conditions and states of the circuit are listed below:

V_A (Volt)	V_B (Volt)	Q_1 State	Q_2 State	V_o (Volt)
0	0	OFF	OFF	10
10	0	SAT	OFF	10
0	10	OFF	SAT	10
10	10	SAT	SAT	0

- The logic function is shown below. This is the operation of a NAND logic gate.

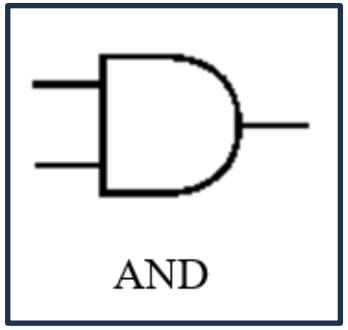
A	B	Z
0	0	1
0	1	1
1	0	1
1	1	0

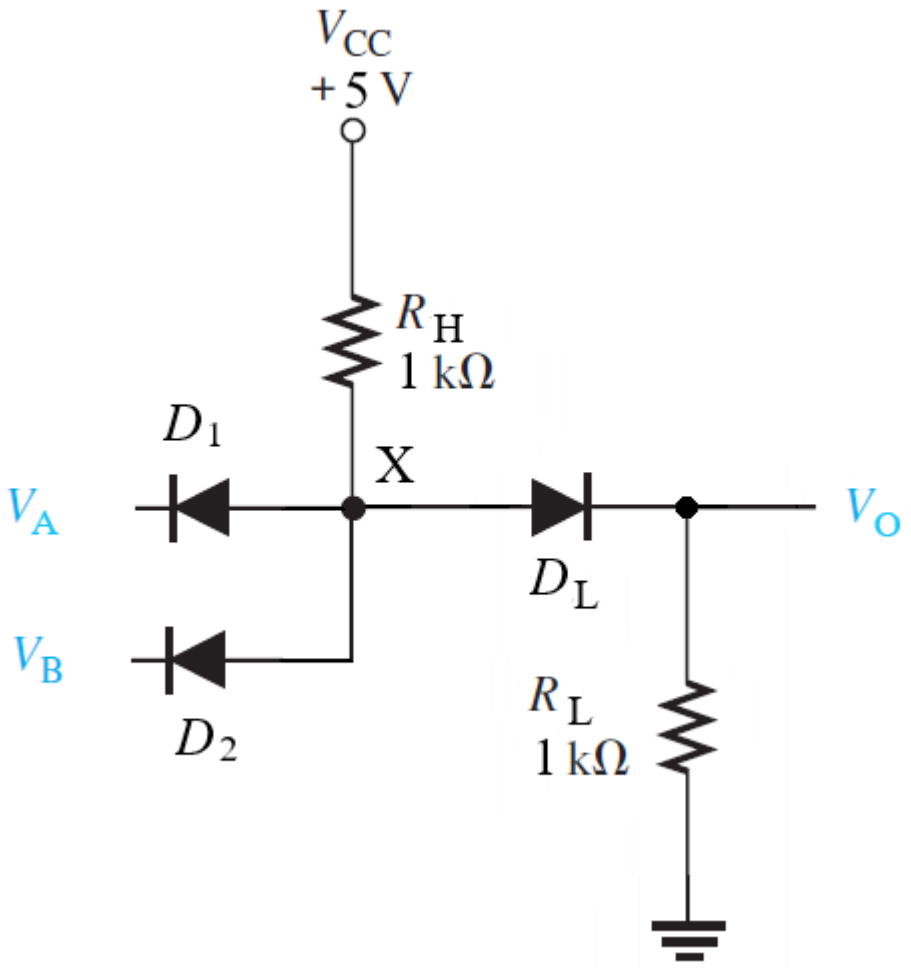
9. Logic Device Families

- Logic devices can be designed and constructed from diodes, transistors, and a few passive components.
- Based on their histories, logic device families are:
  - Diode Logic (DL).
  - Resistor-Transistor Logic (RTL).
  - Diode-Transistor Logic (DTL).
  - Transistor-Transistor Logic (TTL).
  - Emitter-Coupled Logic (ECL).
  - (Complementary) FET:
    - Complementary Metal Oxide Semiconductor (CMOS).
    - BiCMOS.

Diode Logic (DL)

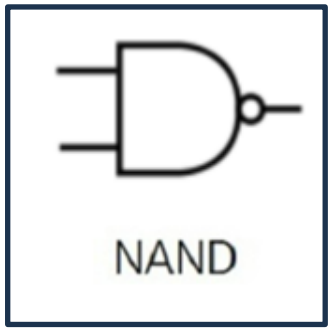
- Simplest form of logic.
- Does not scale.
- NOT logic is not possible (need an active element).
- Example of DL's AND logic circuit.

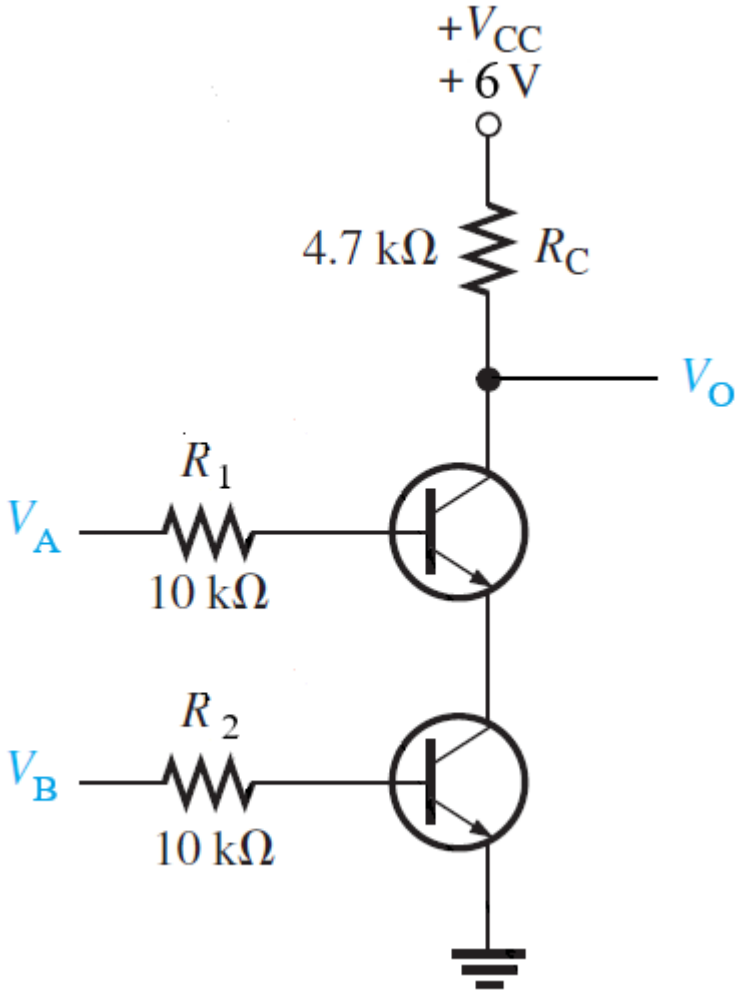




Resistor-Transistor Logic (RTL)

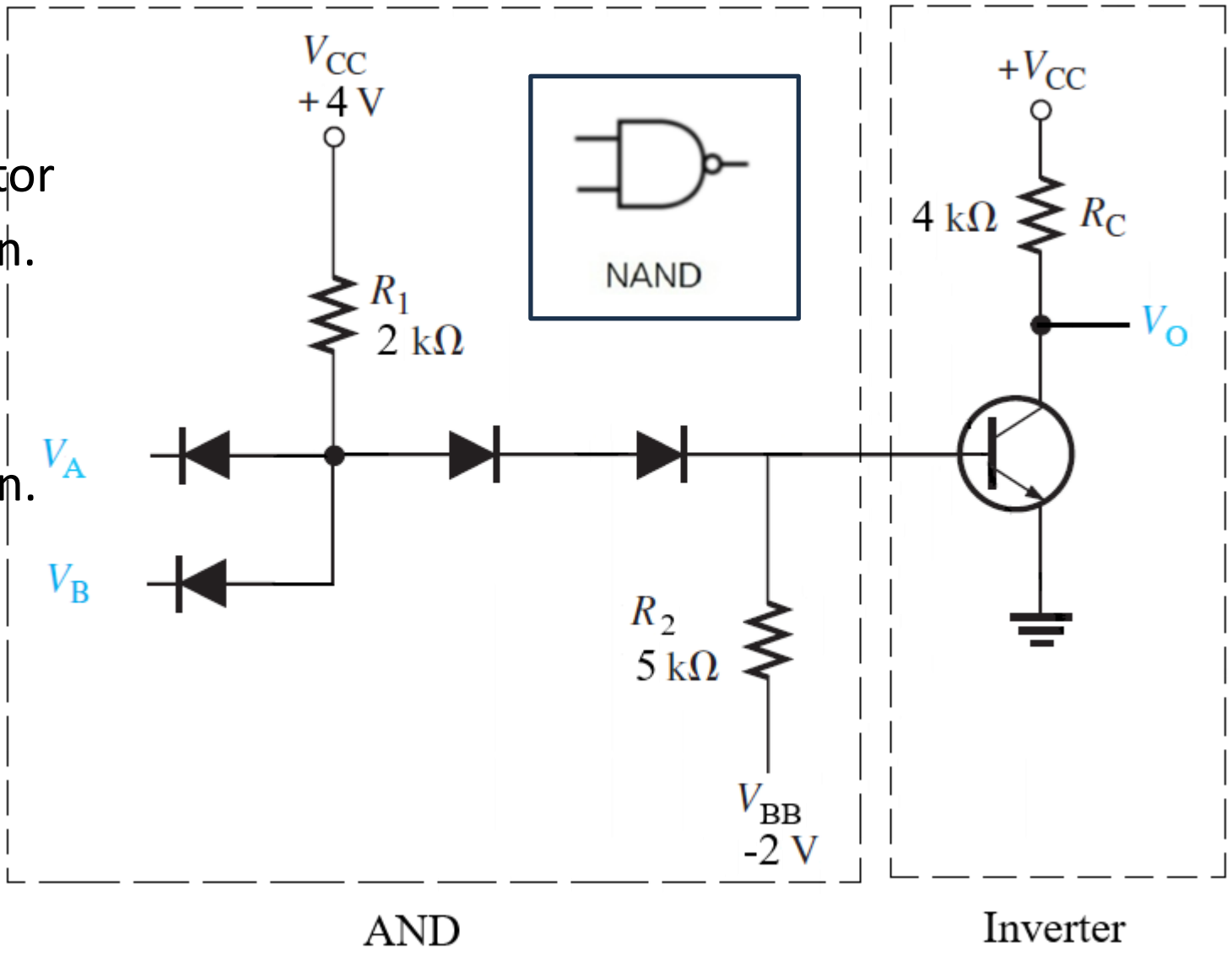
- Replace diode switch with a transistor switch.
- Can be cascaded.
- Large power draw.
- Example of RTL's NAND logic circuit.





Diode-Transistor Logic (DTL)

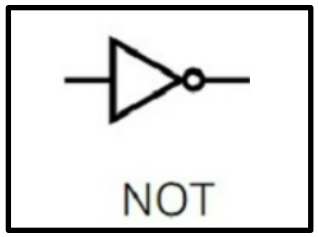
- Essentially diode logic with transistor amplification.
- Reduced power consumption.
- Faster than RTL.
- Example of ECL's NAND logic circuit

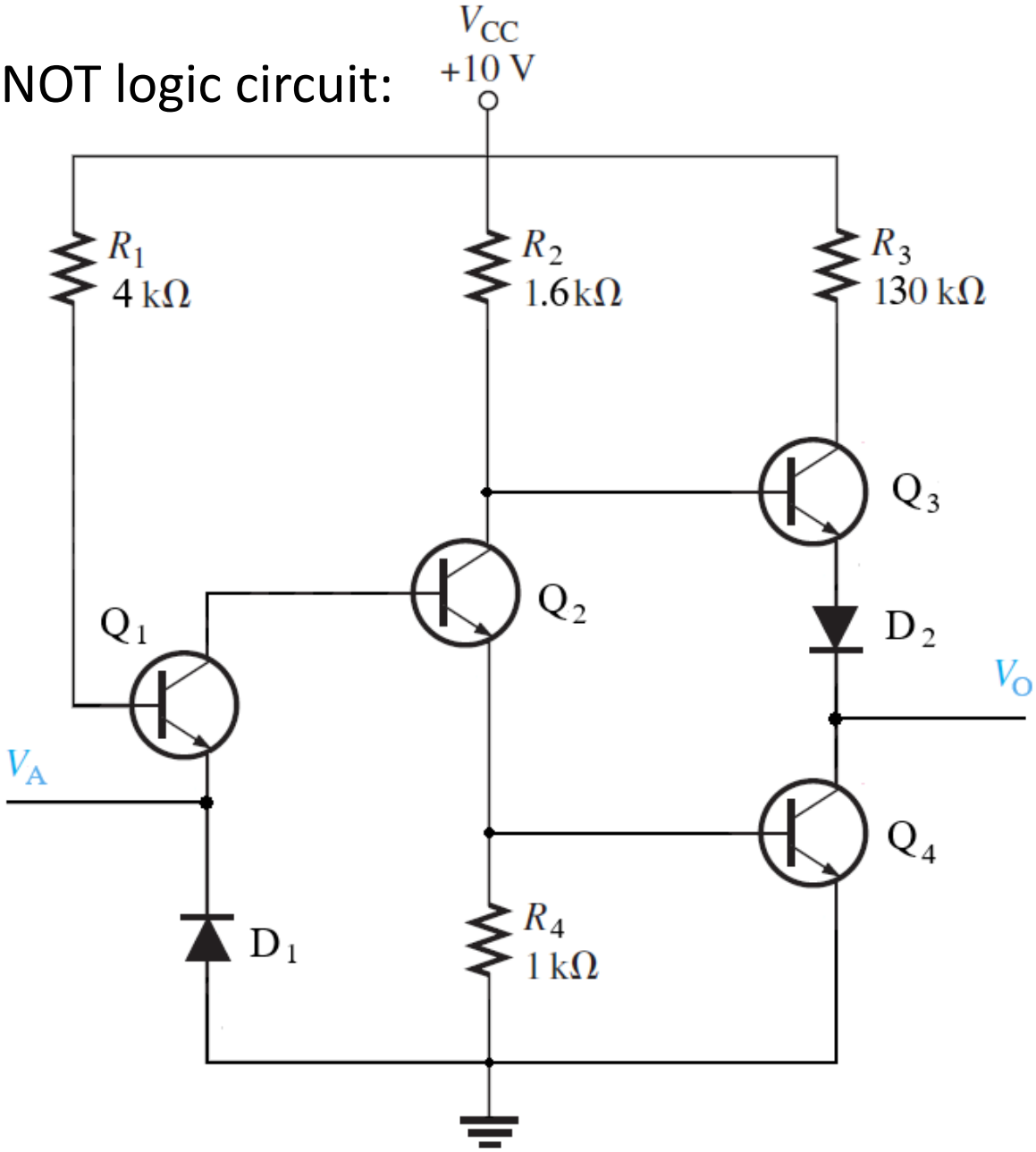


Transistor-Transistor Logic (TTL)

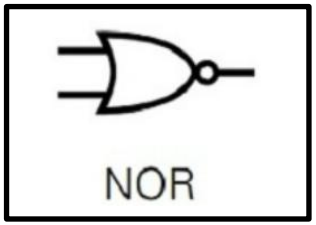
- First introduced by Texas Instruments in 1964.
- TTL has shaped digital technology in many ways.
- Standard TTL family (e.g. 7400) is obsolete.
- Newer TTL families still used (e.g. 74ALS00).
- Distinct features:
  - Multi-emitter transistors.
  - Totem-pole transistor arrangement.

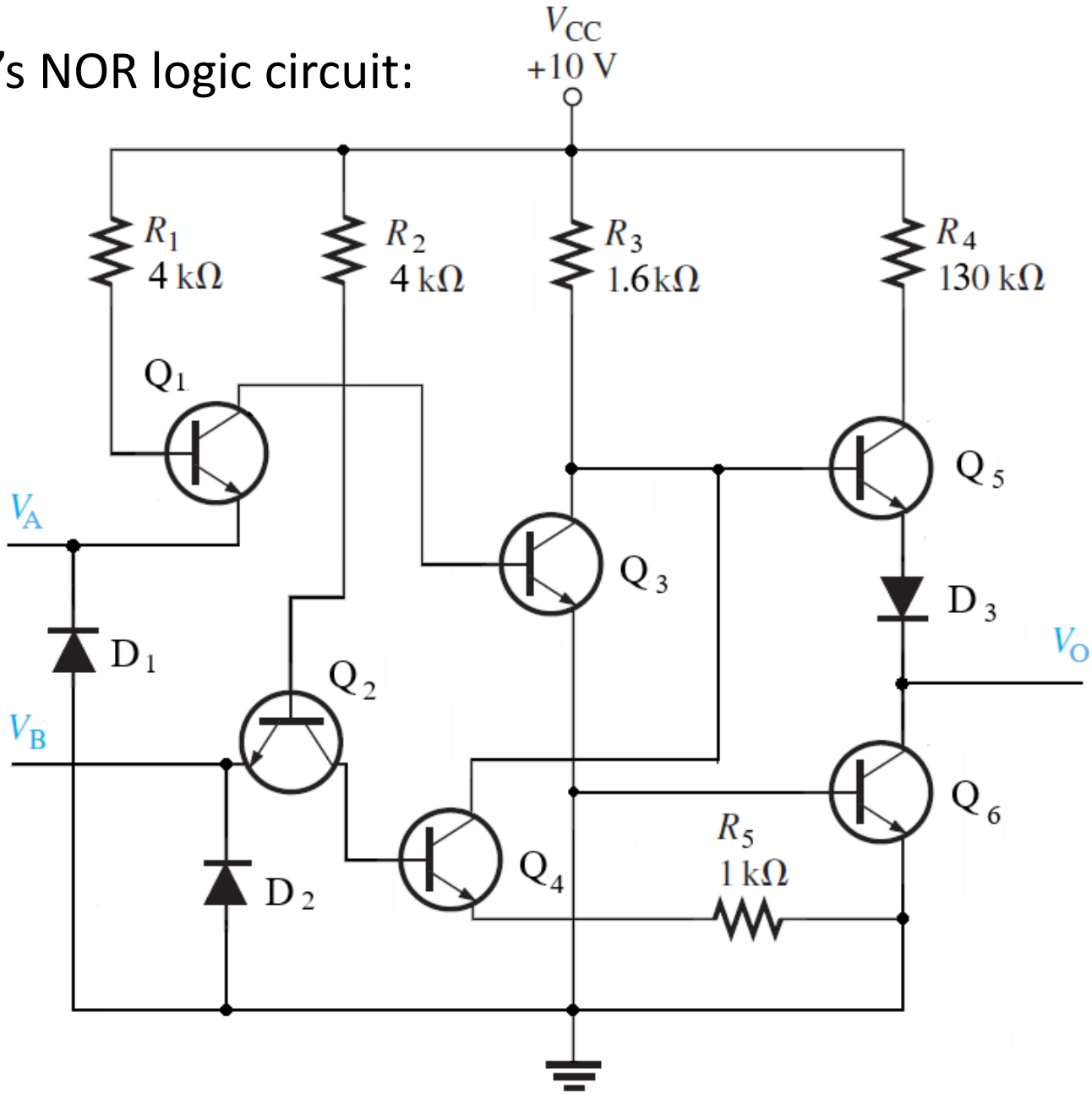
- Examples of TTL's NOT logic circuit:





- Example of TTL's NOR logic circuit:





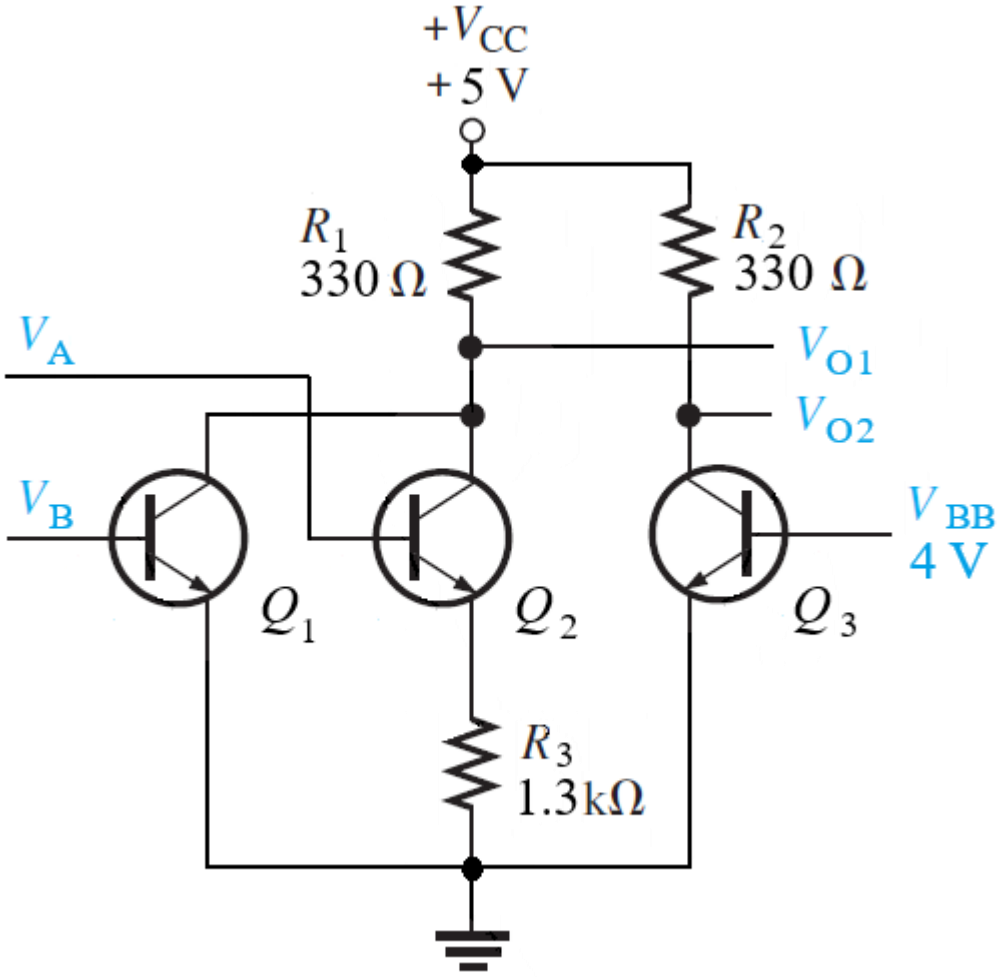
Emitter-Coupled Logic (ECL)

- Fastest logic family available (~ 1 ns) (pros).
- Low noise margin and high-power dissipation (cons).
- Operated in emitter coupled geometry (i.e. emitter-follower), transistors are biased and operate near their Q-point (i.e. never near saturation).
- Logic levels. “0”: –1.7 V. “1”: –0.8 V.
- Such uncommon logic levels require extra effort when interfacing to TTL/CMOS logic families.

- Example of ECL's NOR logic circuit.

NOR

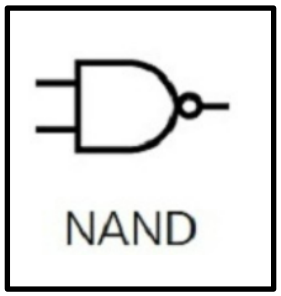
X	Y	Out1	Out2
0	0	1	0
0	1	0	1
1	0	0	1
1	1	0	1

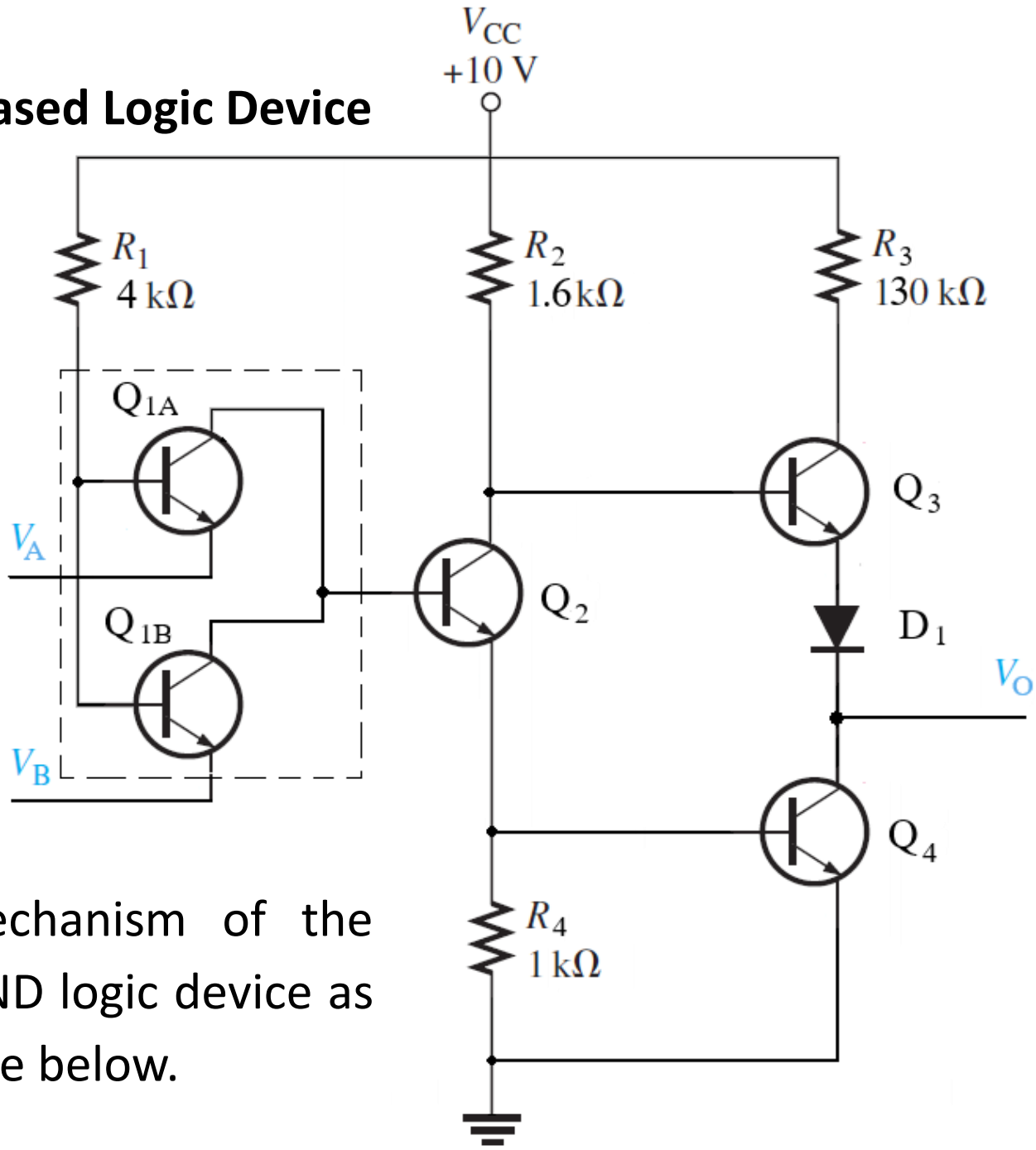


- Comparison of families of the logic gate circuits:

SPECIFICATION	TTL	ECL	CMOS
Components	Transistors & passive elements	Transistors & passive elements	MOSFETs
Basic Gate	NAND	OR/NOR	NAND/NOR
Noise Immunity	Strong	Good	Very strong
Fan-out	10	25	More than 50
tPD in ns	1.5-30	1-4	1-210
Noise margin	Moderate	Low	High
Power/gate in mWatt	10	40-55	0.0025
Clock rate in MHz	35	>60	10
Figure of Merit	100	40-100	0.7

Example 3 – TTL Based Logic Device

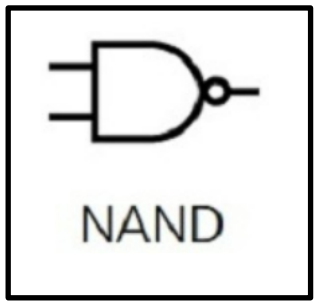




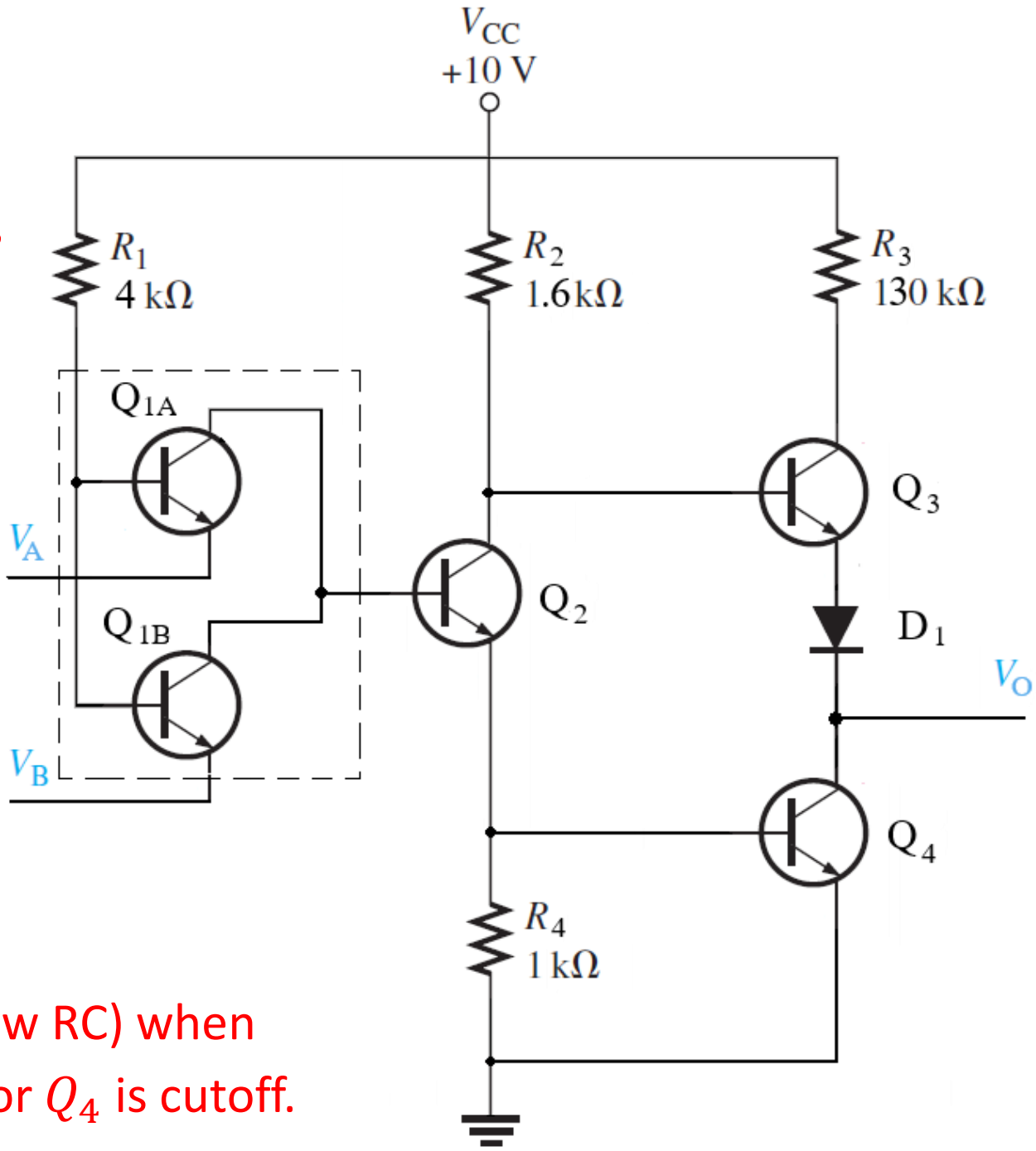
Describe the mechanism of the following TTL NAND logic device as shown in the figure below.

Answer

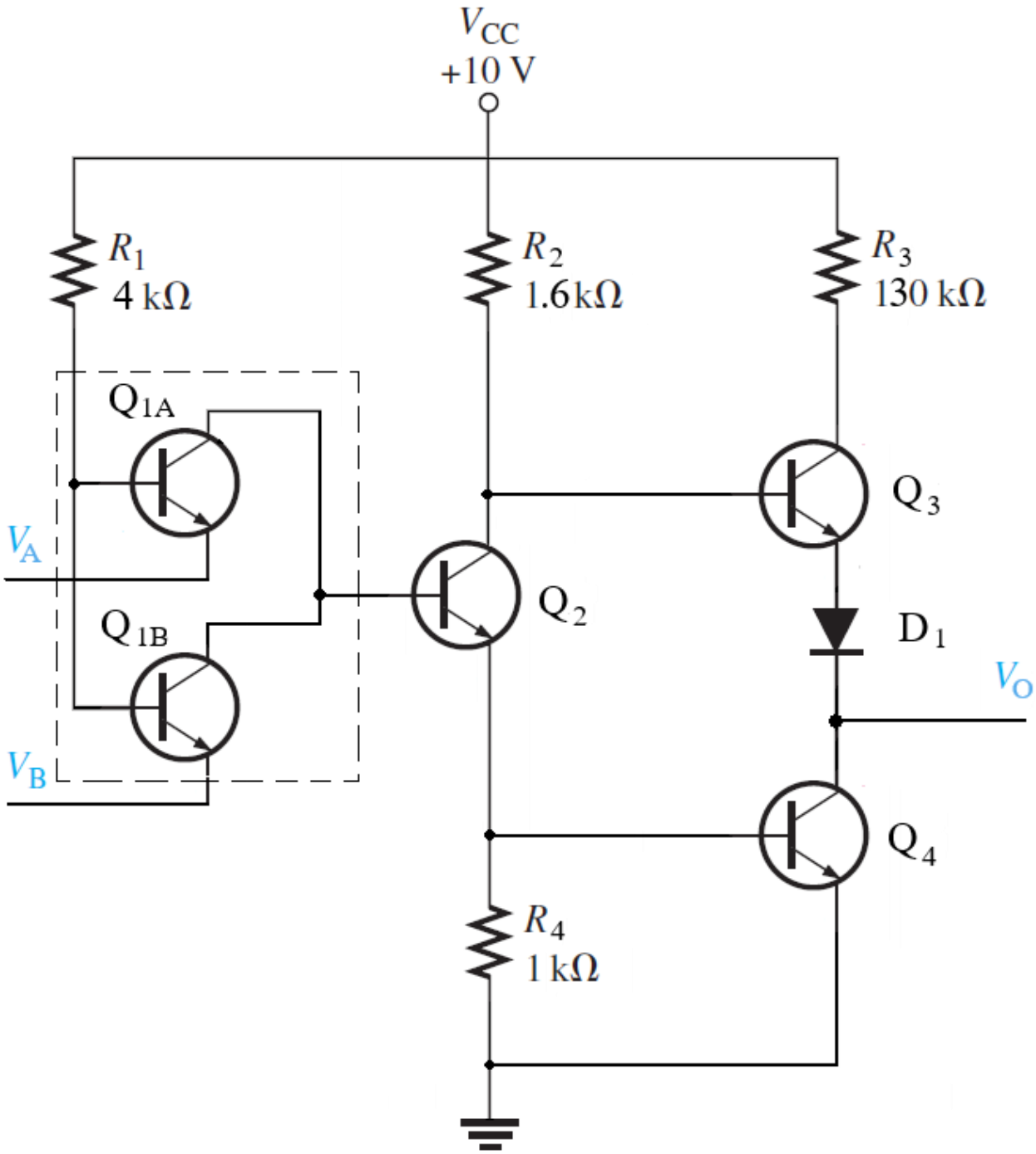
- Transistor Q_3 is cutoff (i.e. act like a high RC) when output transistor Q_4 is saturated, and Q_3 is saturated

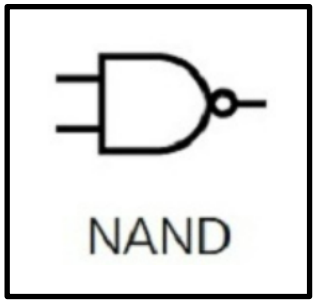


(i.e. act like a low RC) when output transistor Q_4 is cutoff.

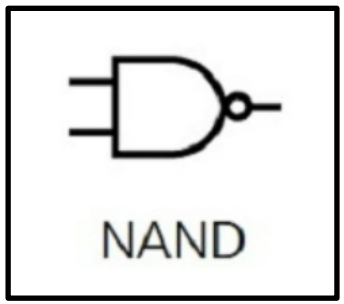


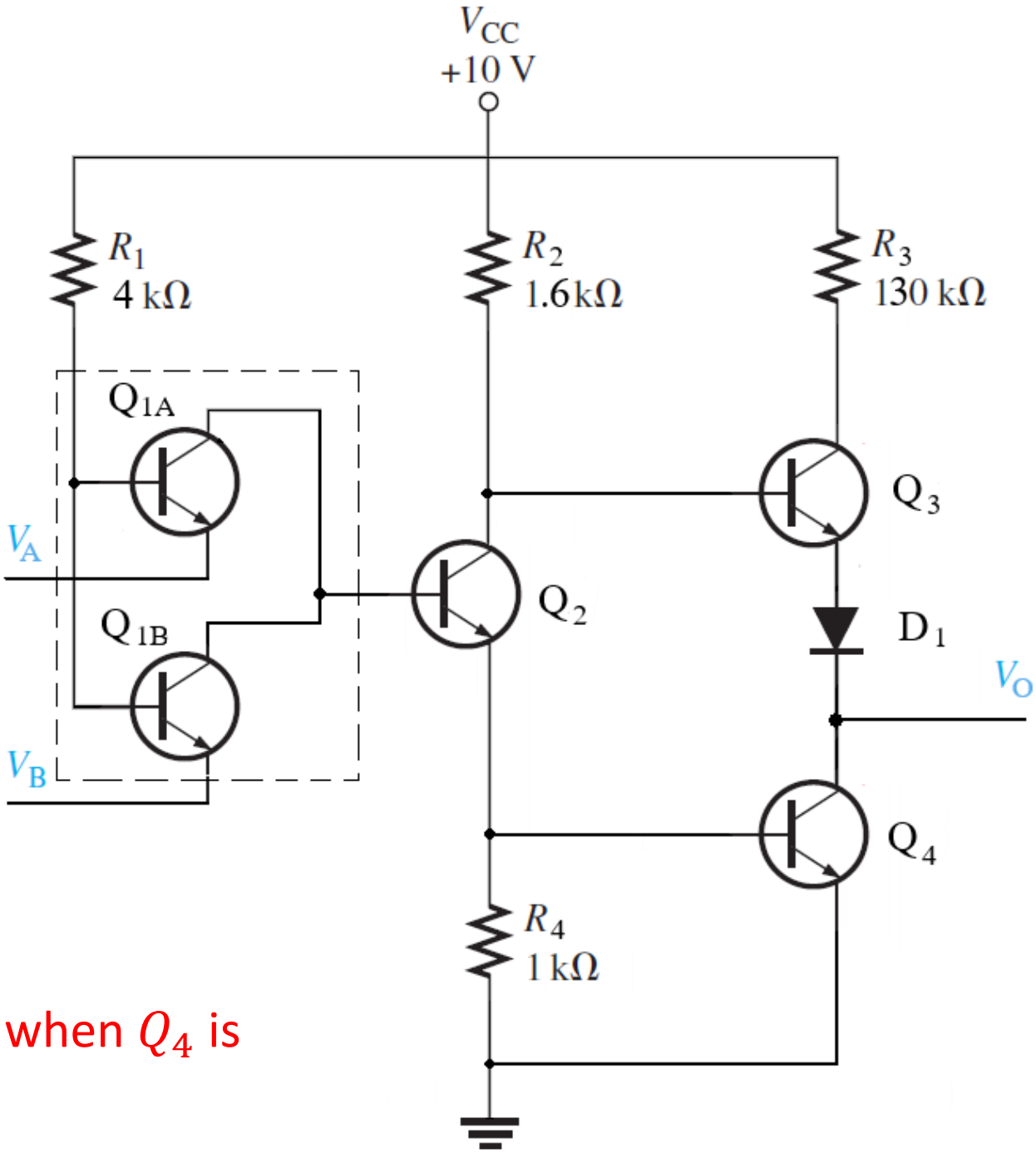
- Thus, one transistor is ON at one time.
- The combination of Q_3 and Q_4 is called TOTEM POLE arrangement.



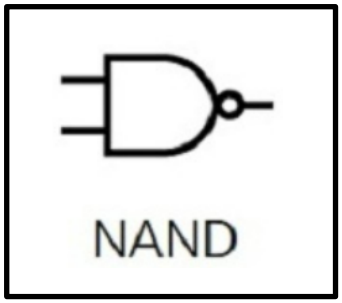


- Transistor Q_1 is called input transistor, which is multi emitter transistor, that drive transistor Q_2 which is used to control Q_3 and Q_4.

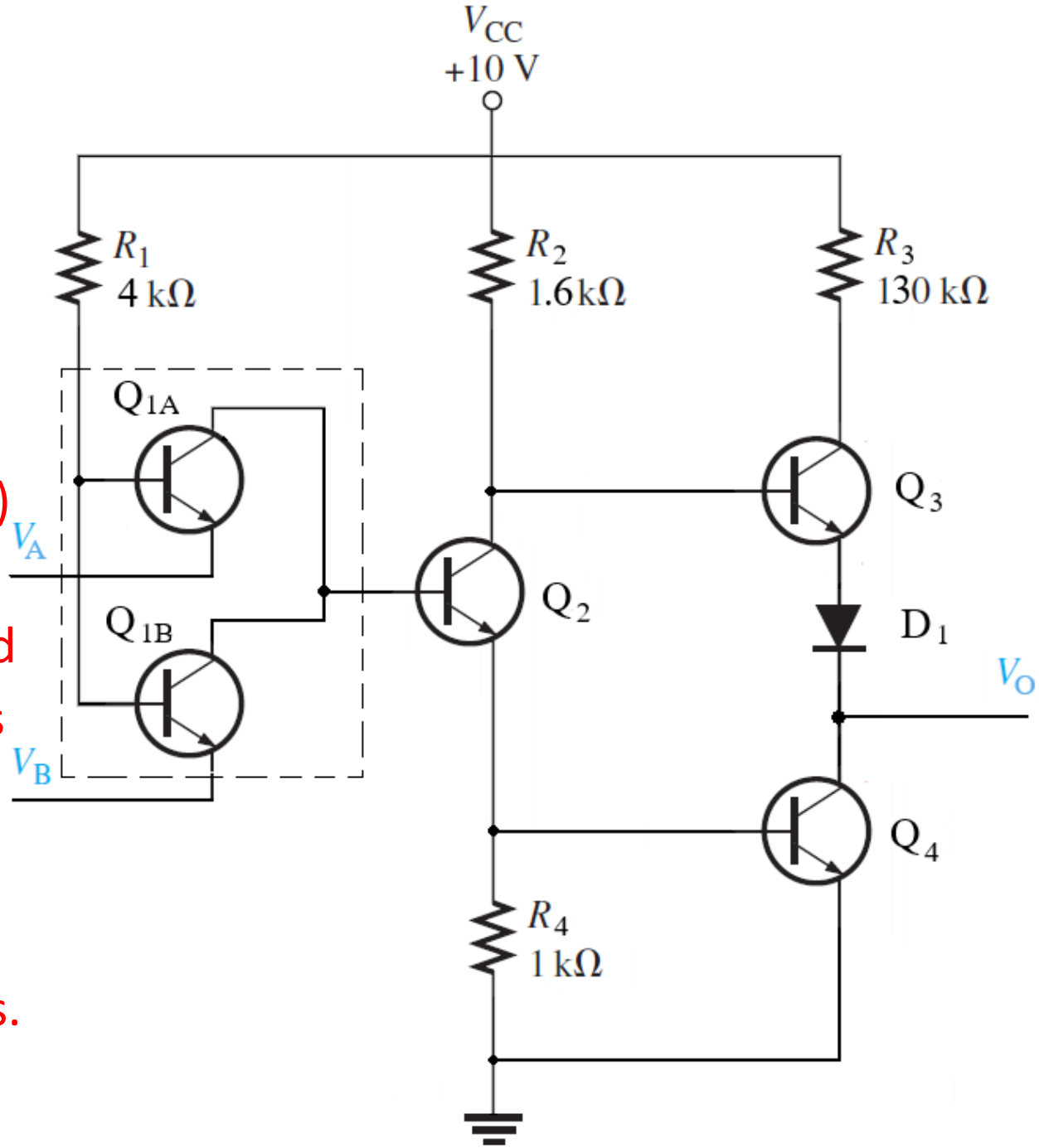




- Diode D_1 ensures when Q_4 is ON and Q_3 is OFF.



- (In some designs) two additional diodes connected to V_A and V_B pins are used to protect Q_1 from unwanted negative voltages.



- The conditions and states of the circuit are listed below:

V_A (Volt)	V_B (Volt)	Q_{1A} State	Q_{1B} State	Q_2 State	Q_3 State	Q_4 State	V_O (Volt)
0	0	OFF	OFF	SAT	SAT	SAT	10
10	0	SAT	OFF	SAT	SAT	SAT	10
0	10	OFF	SAT	SAT	SAT	SAT	10
10	10	SAT	SAT	OFF	SAT	OFF	0

- The logic function is shown below. This is the operation of a NAND logic gate.

A	B	Z
0	0	1
0	1	1
1	0	1
1	1	0