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XMUT204 Electronic Design

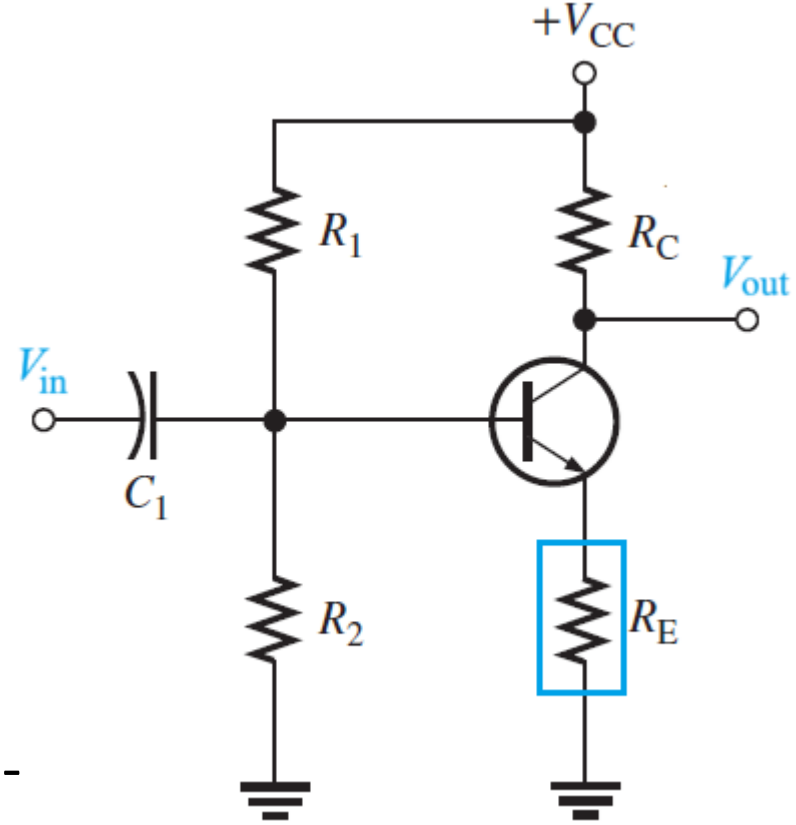
Lecture 3f – BJT Frequency Response Analysis

Overview

1. Small-Signal (AC) Analysis of CE Feedback Amplifier Circuit.
2. A Comment on the Voltage Gain.
3. Use of an Emitter Bypass Capacitor.
4. Swamped Resistor.
5. Frequency Response of BJT Amplifier.
6. Design Procedures.
7. BJT Amplifier Design Example.

1. Small-Signal (AC) Analysis of CE Feedback-Amplifier Circuit

- We will start the design with the common-emitter amplifier circuit as shown in the figure given below.



Assumptions:

- Small-signal gain β_{ac} is large so the small-signal base current i_b may be neglected.
- The DC value of V_{BE} remains constant ~ 0.7 V so that small-signal v_{be} is very small.

1. Small-Signal (AC) Analysis of CE Feedback-Amplifier Circuit (cont.)

- As v_{be} is very small, we will have:

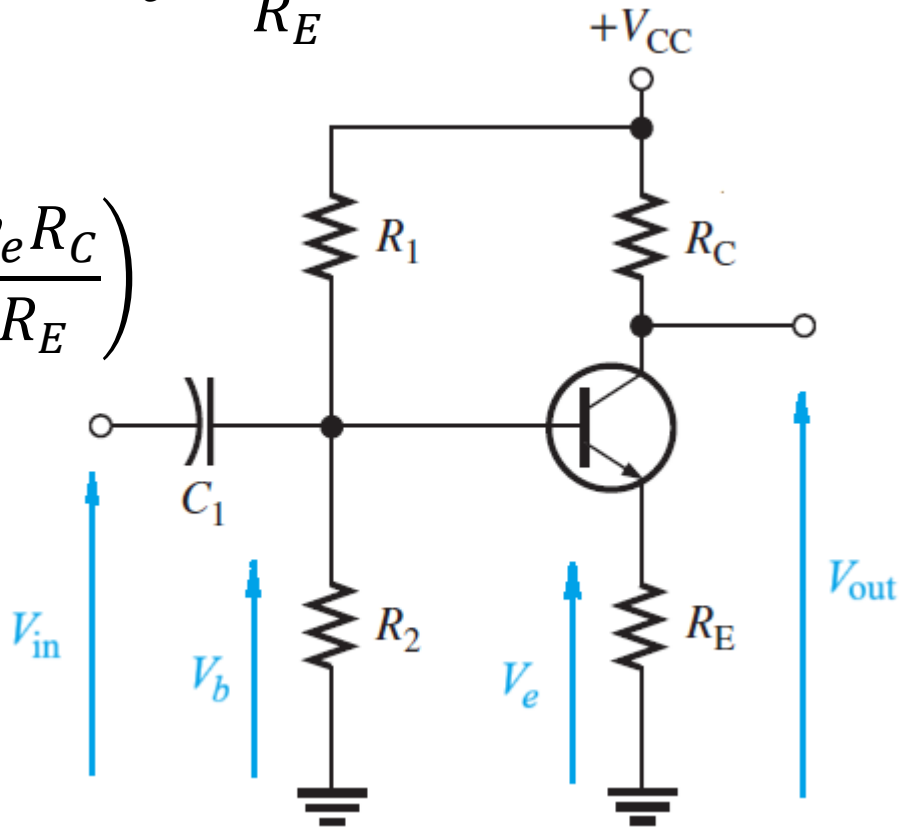
$$v_e = v_b = v_i \quad \text{so} \quad i_e = \frac{v_e}{R_E}$$

- As $i_c \approx i_e$, we will have:

$$v_o = -i_c R_c \approx -i_e R_C = -\left(\frac{v_e R_C}{R_E}\right)$$

- As $v_e \approx v_i$, we will have:

$$v_o \approx -\left(\frac{v_i R_C}{R_E}\right)$$

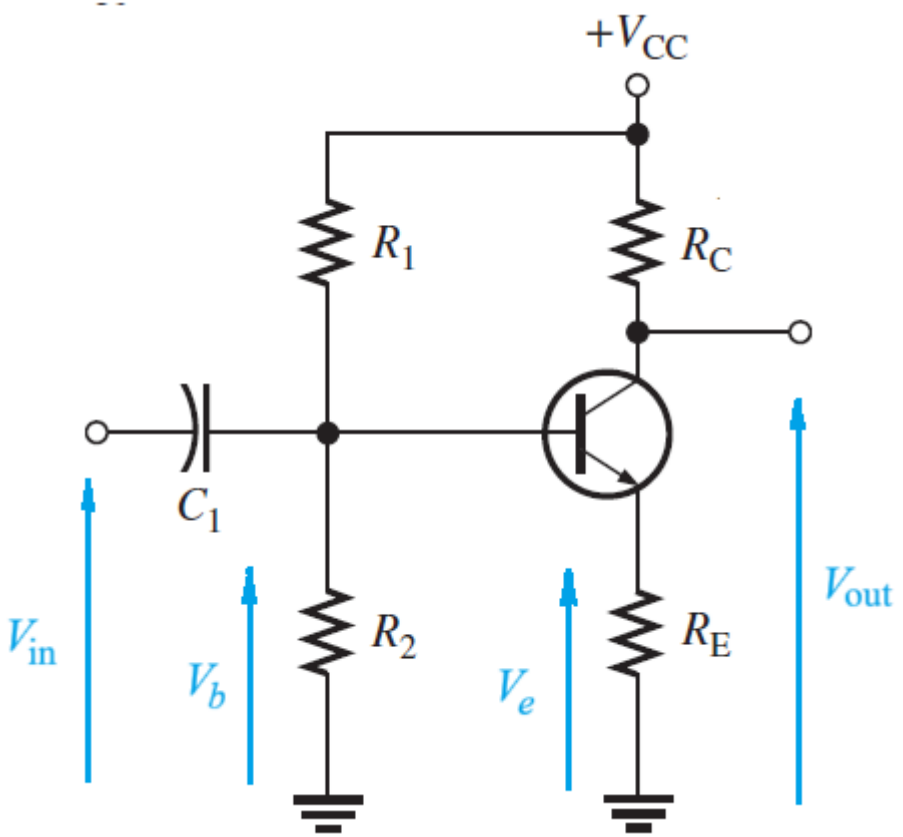


1. Small-Signal (AC) Analysis of CE Feedback-Amplifier Circuit (cont.)

- And the voltage gain will be given by:

$$\frac{v_o}{v_i} \approx -\left(\frac{R_C}{R_E}\right)$$

- Gain now only controlled by the value of passive components and is independent of β!



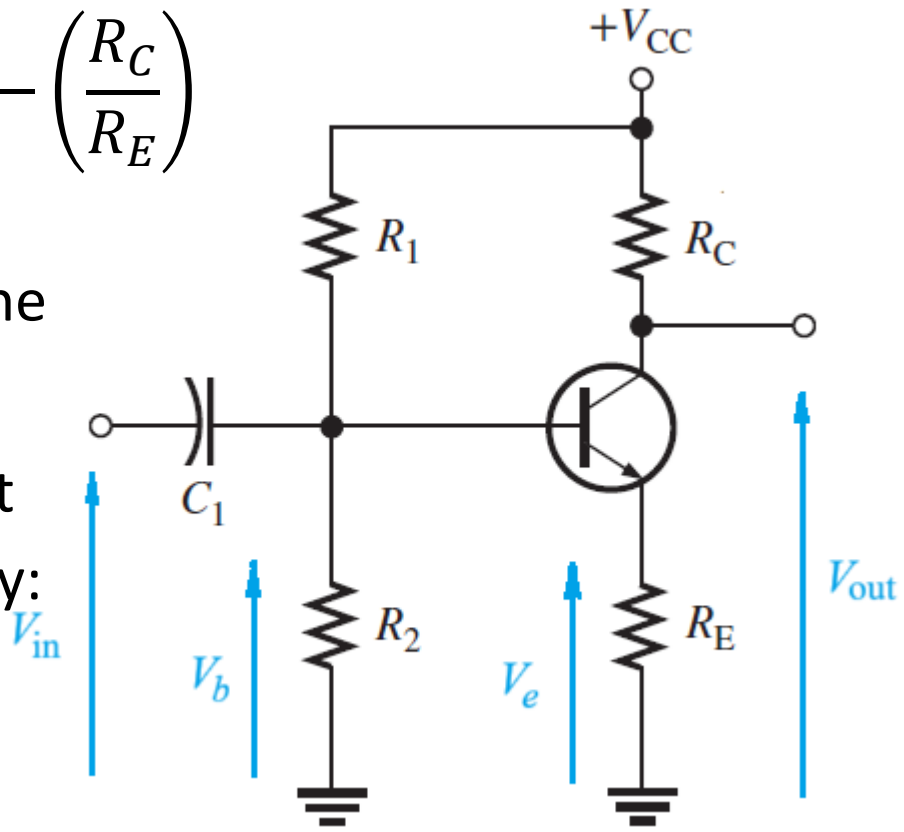
2. Voltage Gain of BJT Amplifier

- We have an expression for the voltage gain given by:

$$v_o/v_i \approx -\left(\frac{R_C}{R_E}\right)$$

- This considerably smaller than the gain without feedback in the CE configuration.
- In the CE configuration without feedback, the gain was given by:

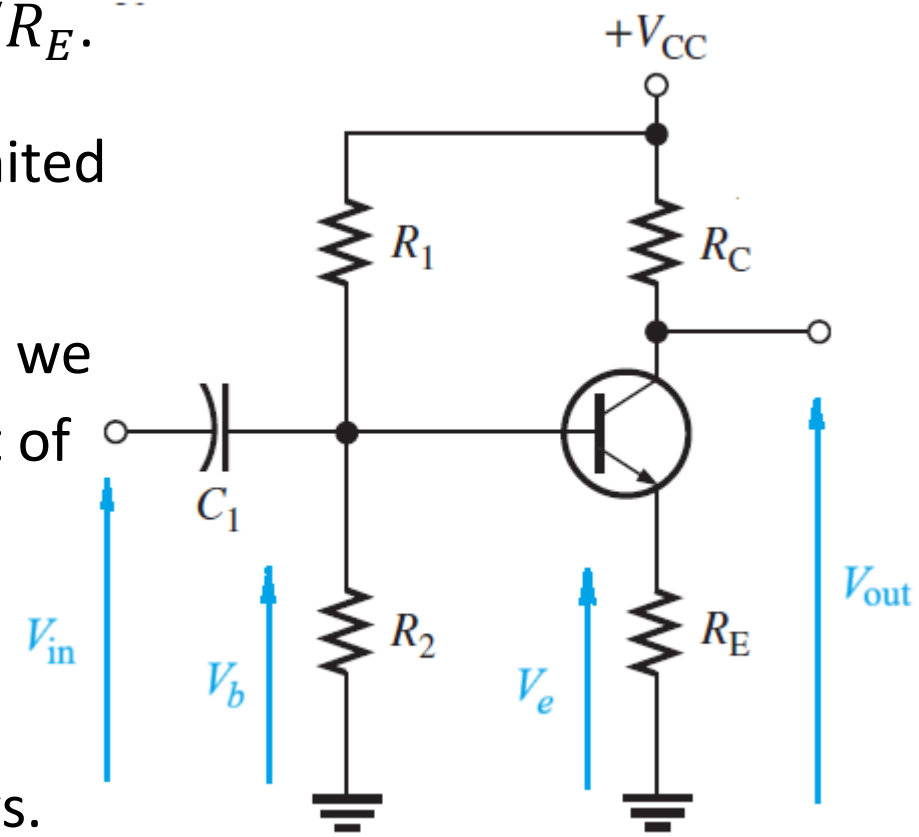
$$A_v = -\left(\frac{R_E}{r_e}\right)$$



Where: $r_e = 1/g_m$ with g_m is the transconductance (ratio of I_c/V_{BE}).

2. Voltage Gain of BJT Amplifier (cont.)

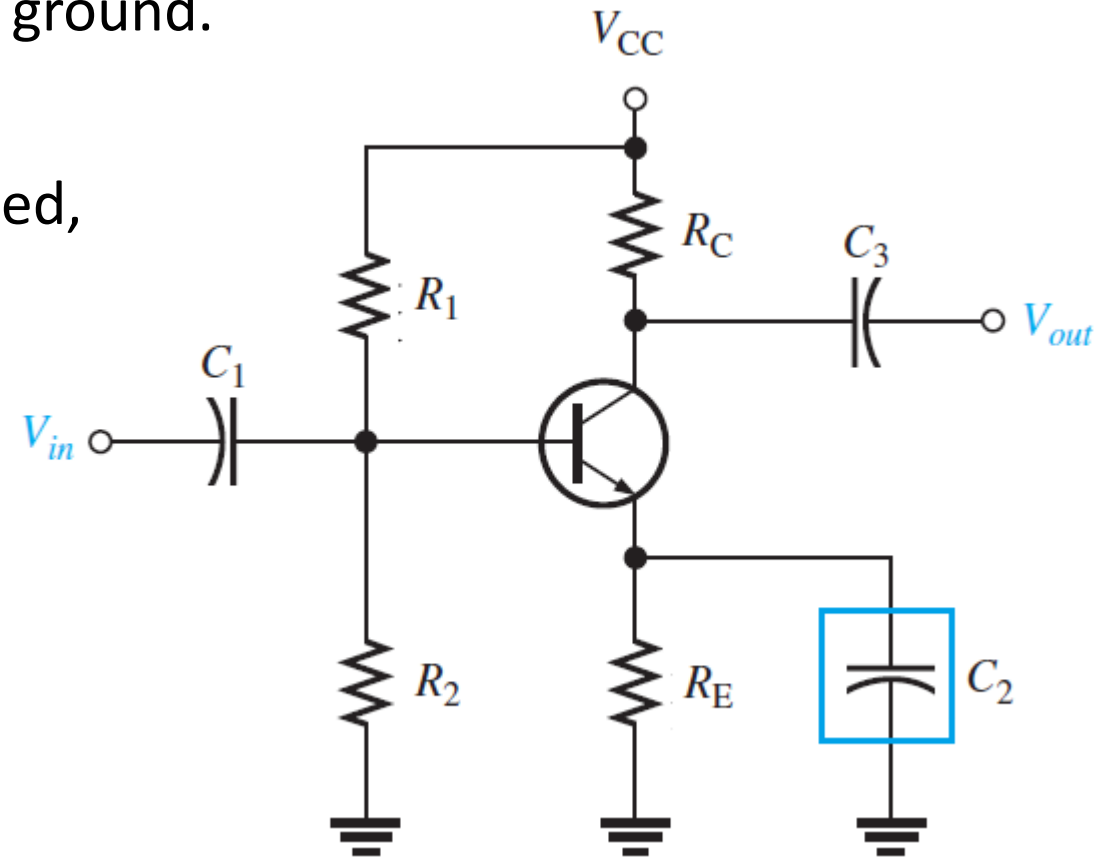
- Thus, it would appear that we can increase the gain simply by increasing this ratio of R_C/R_E.
- This can only be done to a limited extent in practice:
  - R_E cannot be too small as we need a significant amount of feedback to make circuit work.
  - R_C cannot be too large to limit the current that flows.



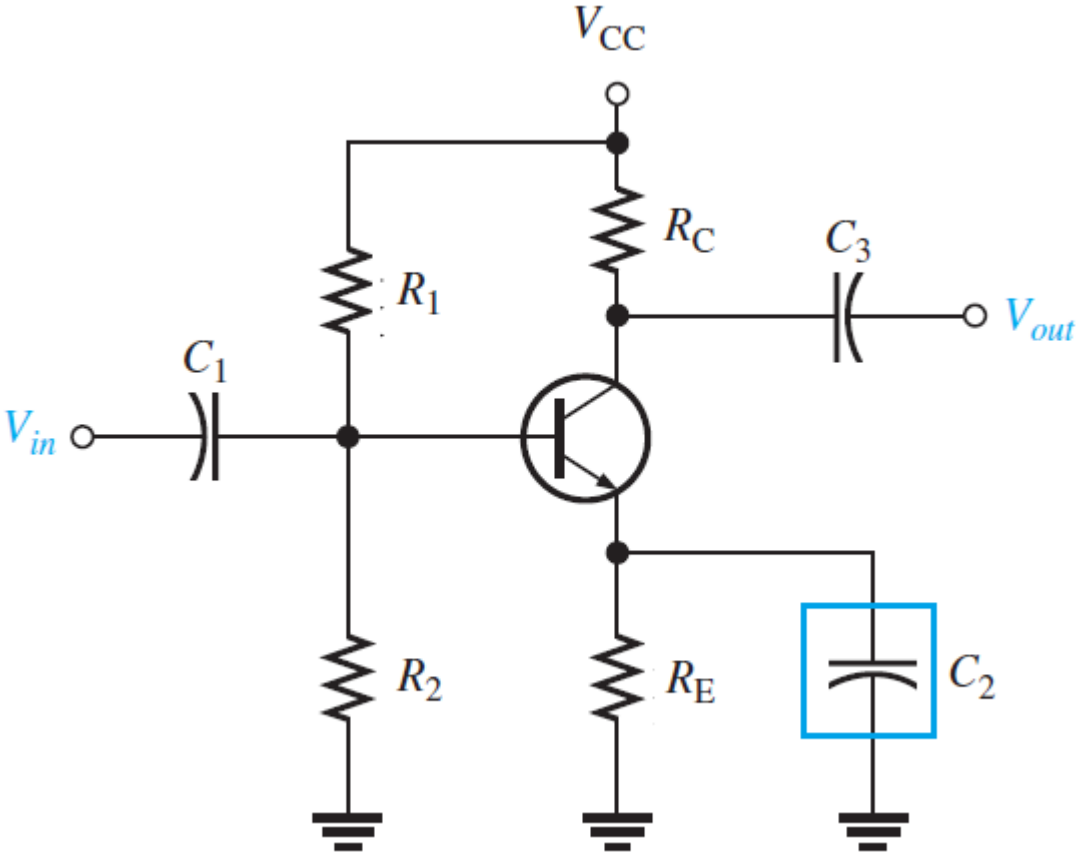
- We have thus traded off increased stability for a loss of high gain.

3. Use of an Emitter-Bypass Capacitor

- Previously stated that the use of an emitter-bypass capacitor leads to increased gain as the small signal passes through this capacitor and to ground.
- In this way, the DC feedback is maintained, but AC feedback is removed.
- At low frequencies, the effect of the bypass capacitor will fall, and small-signal gain will fall.



- This point is determined by the frequency at which the impedance of the bypass capacitor becomes appreciable compared to the parallel combination of R_E and r_e, where r_e is the resistance looking into the emitter.

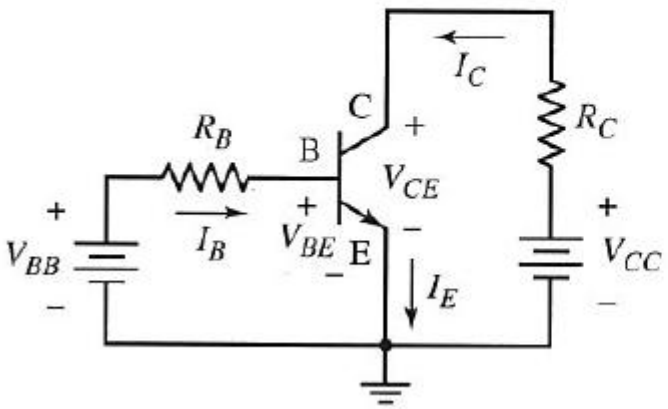


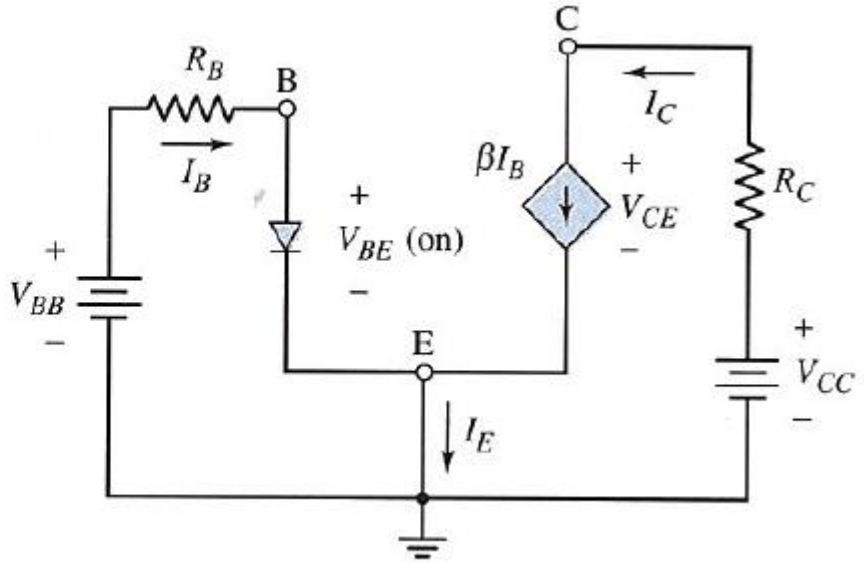
- We have: $r_e = 1/g_m$ and it can be shown that:

$$r_e \approx \frac{1}{40 I_E} = \frac{25\ \text{mV}}{I_E}$$

Where: the transconductance of the amplifier, $g_m = I_c/V_{BE}$ and $I_e \approx I_c$.

- The value of r_e is then typically only a few Ω and a lot smaller than R_E.



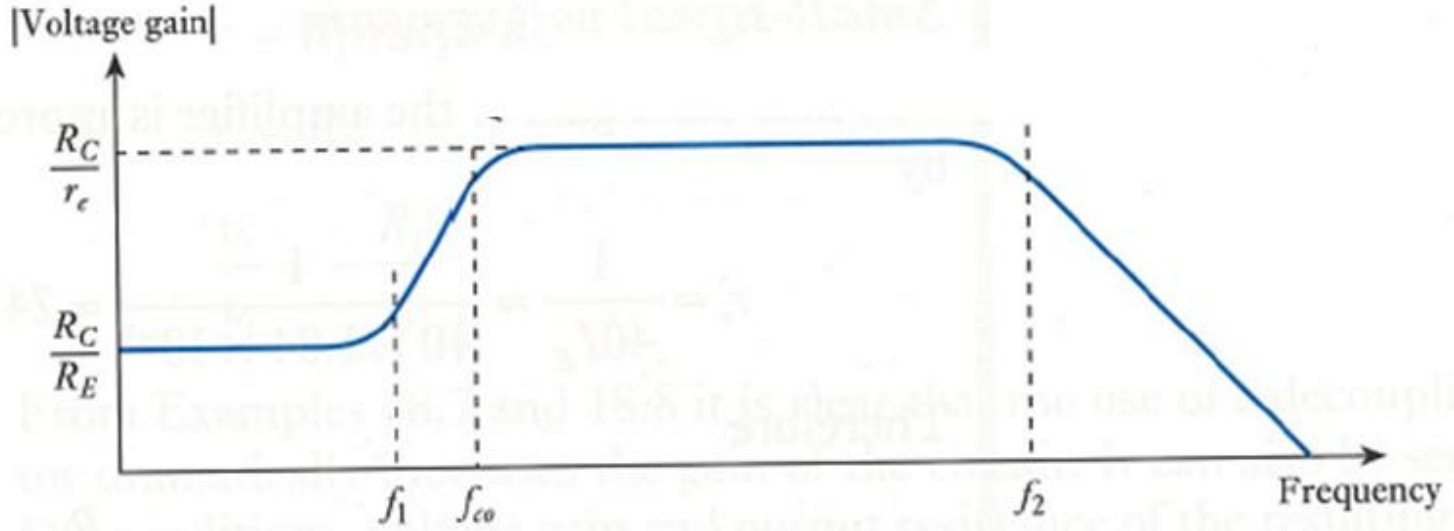


Cut-off Frequency of Bypass Capacitor

- The equation for the cut-off frequency due the bypass capacitor is then:

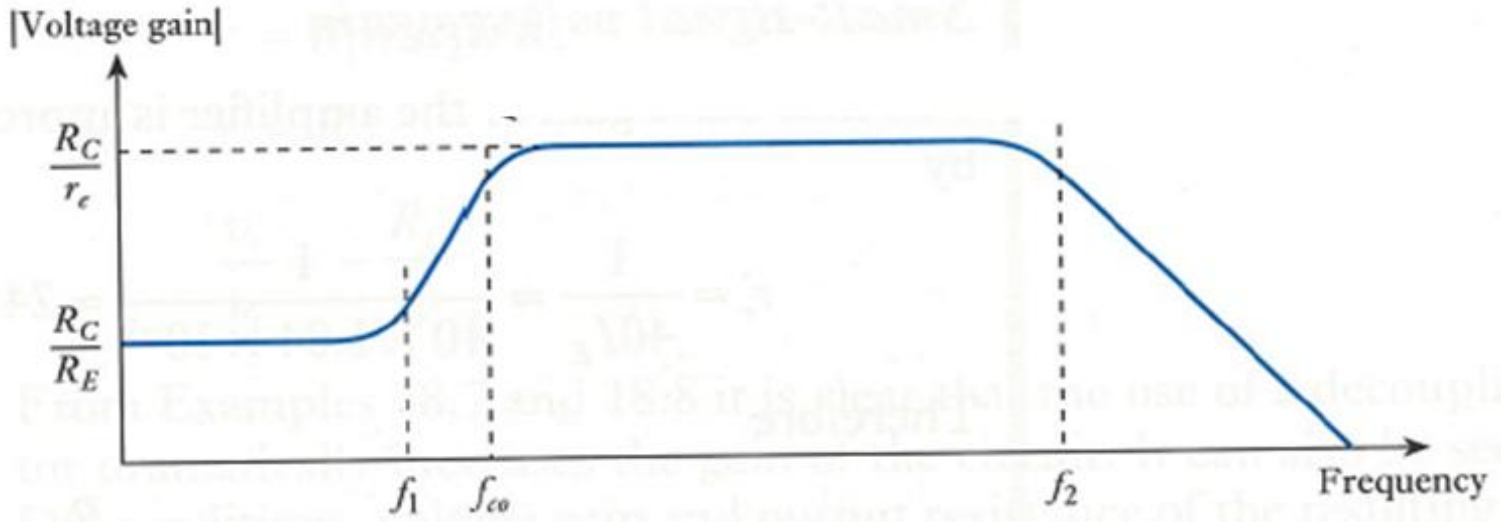
$$f_c = \frac{1}{2\pi C_E r_e}$$

- We can use the above expression to calculate the size of the bypass capacitor that will be required to provide a sufficient low cut-off for the desired application.



- Below the cut-off frequency, the gain will drop by -6 dB per octave until the impedance of C_E becomes comparable to R_E.
- Further below this frequency, the gain will level out as R_E now dominates the response.
- The frequency at which this occurs is given by:

$$f_c = \frac{1}{2\pi C_E R_E}$$



Bandwidth Graph

- The frequency response of the given BJT amplifier depends bandwidth of the amplifier i.e. on the values of lower cut-off frequency (f_1), upper cut-off frequency (f_2) and frequency due to addition of the bypass capacitor (f_{co}).
- The frequency response below is for common-emitter amplifier with emitter resistor and decoupling capacitors.

- With the bypass capacitor in place, the small-signal gain is then given by:

$$A_v = -\frac{R_C}{r_e}$$

- And in our case, we have (with I_E = 1 mA):

$$r_e \approx \frac{1}{40 I_E} = \frac{1}{40(1\ x\ 10^3)} = 24\ \Omega$$

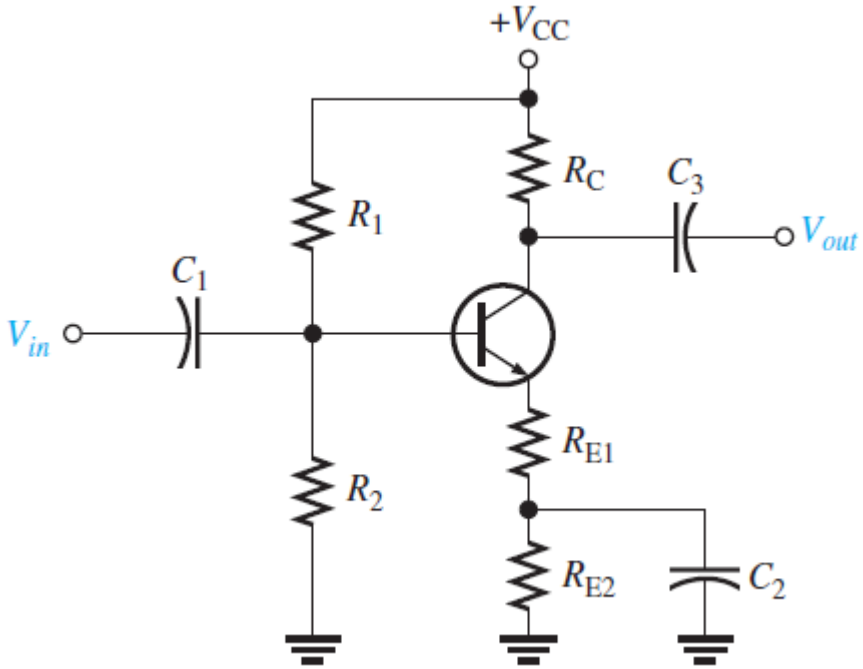
- Thus, small-signal gain of the amplifier:

$$A_v = -\frac{5.6\ \text{k}\Omega}{24\ \Omega} = -233$$

- Which is considerably larger than R_E/R_C.

4. Swamped Resistor

- A swamped amplifier uses a partially bypassed emitter resistance to minimise the effect of r_e' on the gain to achieve gain stability.
- The total external emitter resistance, R_E, is formed with two separate emitter resistors, R_{E1} and R_{E2}.



- Both R_{E1} and R_{E2} affect the DC bias while only R_{E1} affects the AC voltage gain:

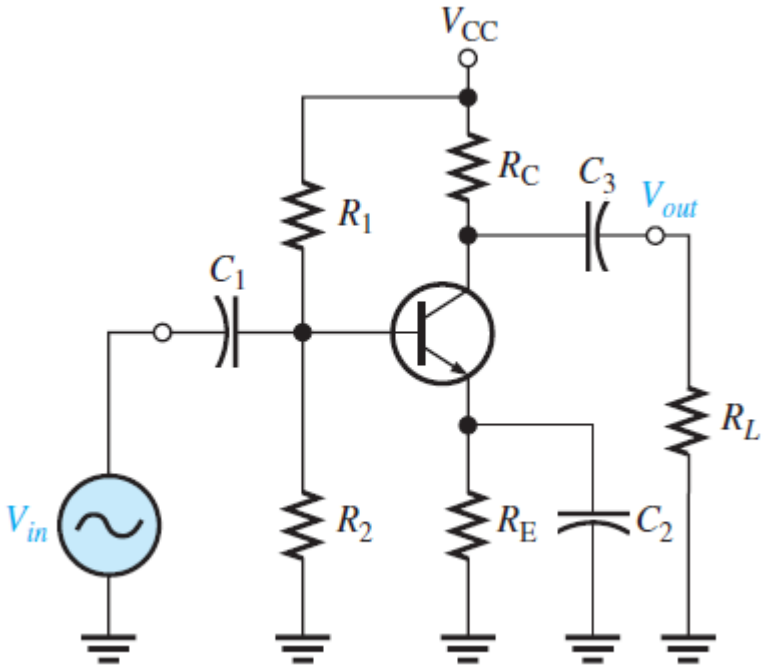
$$A_v = \frac{R_C}{r_e' + R_{E1}}$$

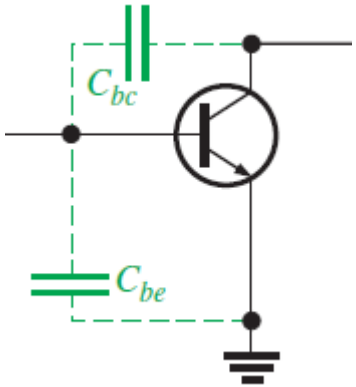
- If R_{E1} is at least ten times larger than r_e', then the effect of r_e' is minimised.
- The approximate voltage gain for the amplifier with the swamped resistor is:

$$A_v \cong \frac{R_C}{R_{E1}}$$

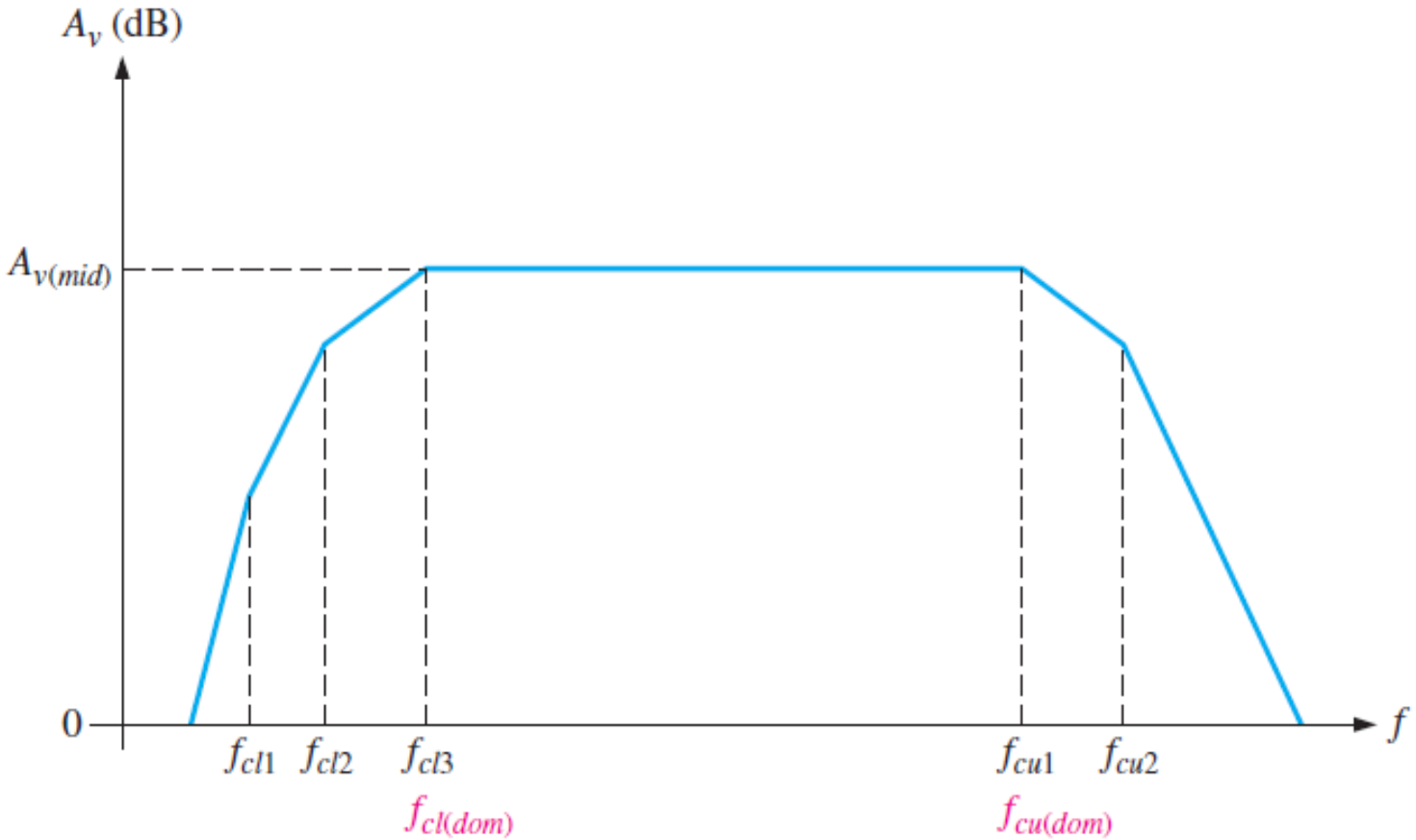
5. Frequency Response of CE BJT Amplifier

- Lower critical frequencies (f_{cl1}, f_{cl2}, and f_{cl3}) are three low-frequency RC circuits of the coupling and bypass capacitors.
- Upper critical frequencies, f_{cu1} and f_{cu2} are two high-frequency RC circuits of the transistor's internal capacitances.





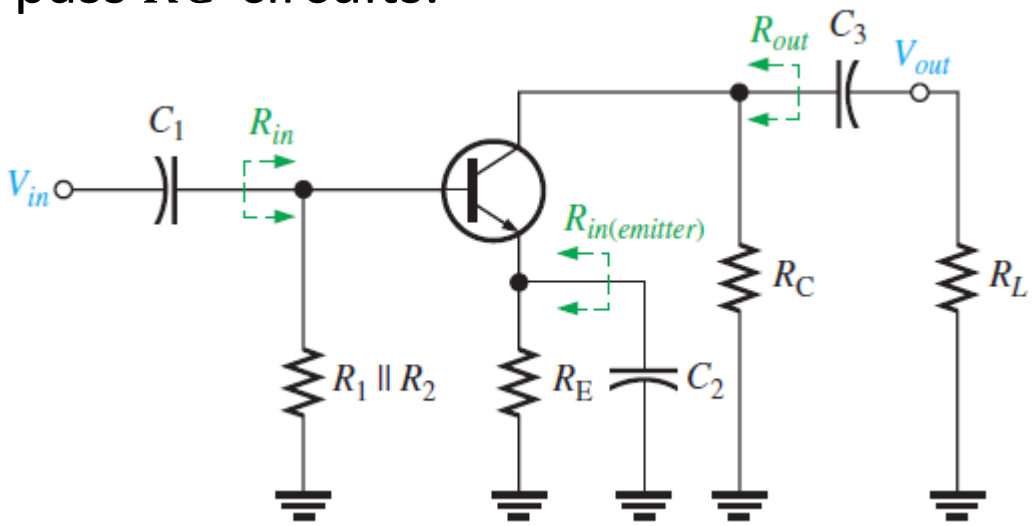
- The cut-off frequencies in the lower frequency region e.g. f_{cl1}, f_{cl2}, and f_{cl3} of the capacitors C_1, C_2, and C_3 respectively.
- The cut-off frequencies at higher frequency region e.g. f_{cu1} and f_{cu2} due to parasitic capacitances in internal BJT.



Determine the Lower Cut-Off Frequency

The low-frequency AC equivalent circuit of the CE BJT amplifier consists of three high-pass RC circuits.

- Input coupling capacitor C_1 and the resistance looking in at the base of the amplifier (R_{in}).



- Output coupling capacitor C_3, the resistance looking in at the collector of the amplifier (R_{out}) and the load resistance (R_L).
- Emitter-bypass capacitor C_1 and the resistance looking in at the emitter of the amplifier ($R_{in(emitter)}$).

- The lower cut-off frequency of the RC circuit at the input of the amplifier is determined from:

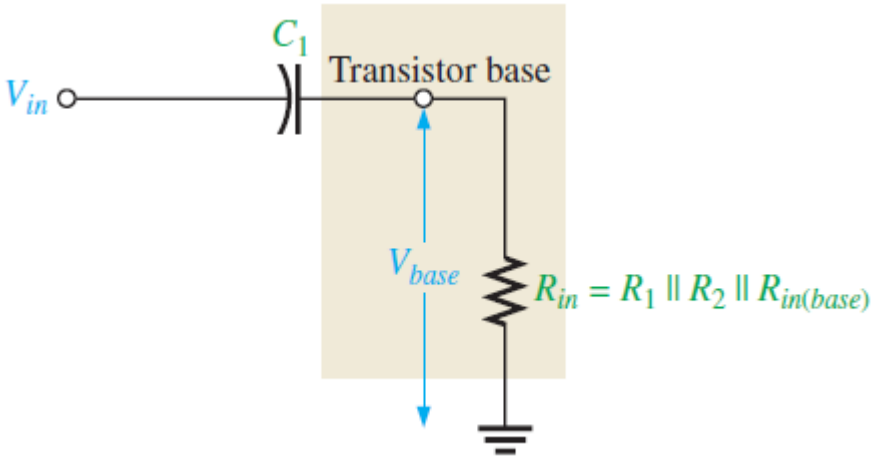
$$X_{C(input)} = \frac{1}{2\pi f_{cl(input)} C_1}$$

- The equivalent resistance at the input of the amplifier is:

$$R_{in} = R_1 \parallel R_2 \parallel R_{in(base)}$$

Where:

$$R_{in(base)} = \beta_{ac} r_e'$$



- Neglecting the reactance at the input of the amplifier, the impedance at the input of the amplifier is:

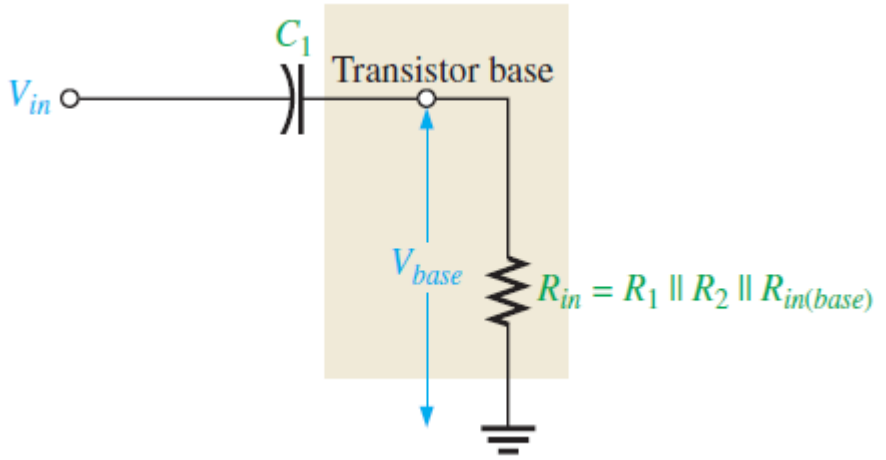
$$X_{C(input)} = R_{in}$$

- So, since, the lower cut-off frequency due to capacitance at the input of the amplifier is:

$$f_{cl(input)} = \frac{1}{2\pi R_{in} C_1}$$

- If the resistance of the input source is considered, the lower cut-off frequency at input is:

$$f_{cl(input)} = \frac{1}{2\pi (R_s + R_{in}) C_1}$$

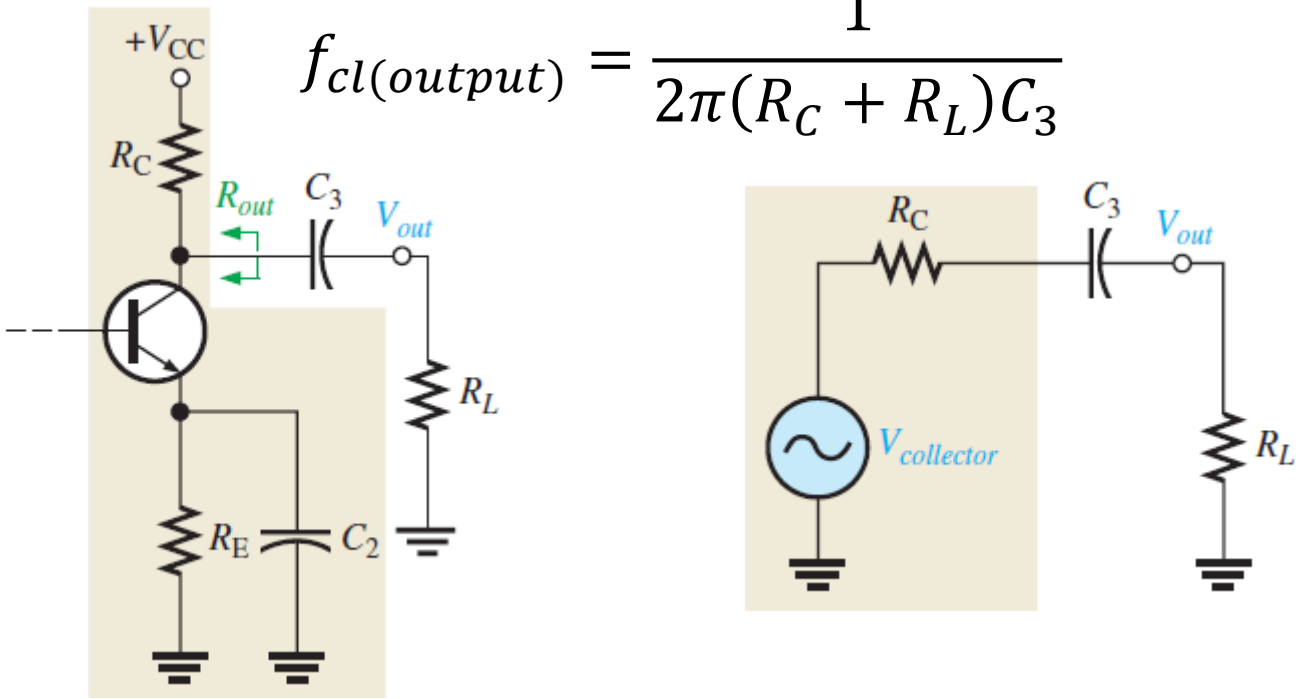


- The collector and load resistors make up impedance at the output of amplifier.

$$X_{C(out)} = R_C + R_L$$

- Lower cut-off frequency of the RC circuit at the output of the amplifier is:

$$f_{cl(output)} = \frac{1}{2\pi(R_C + R_L)C_3}$$



- Equivalent input resistance at the emitter.

$$R_{in} = r_e' + \frac{V_e}{I_e}$$

- Since $V_e = V_b$, $I_e \cong I_c$ and $I_c = \beta_{ac} I_b$, then:

$$R_{in} \cong r_e' + \frac{V_b}{\beta_{ac} I_b}$$

- Knowing $V_b = I_b R_{Th}$, the above equation becomes:

$$R_{in} = r_e' + \frac{I_b R_{Th}}{\beta_{ac} I_b}$$

- Rearranging the above equation, the equivalent input resistance at the emitter is:

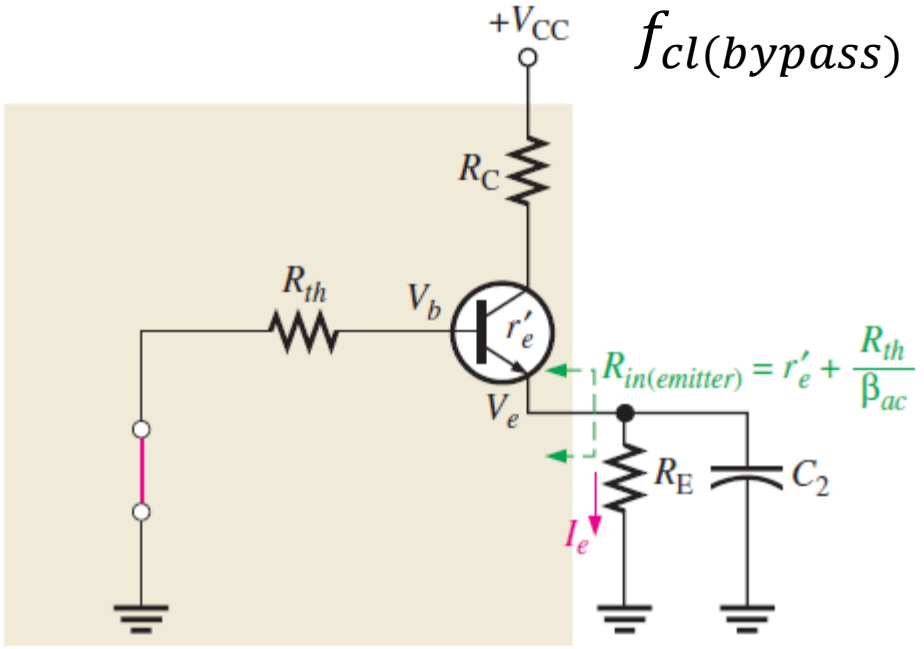
$$R_{in} = r_e' + \frac{R_{th}}{\beta_{ac}}$$

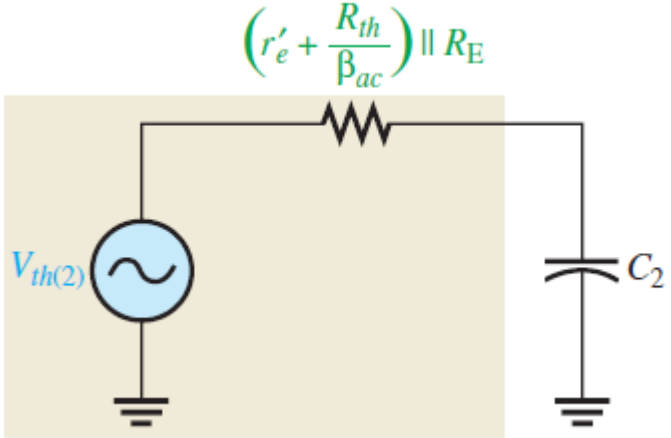
- The total impedance at the emitter is a parallel combination of this equivalent input resistance at the emitter (R_{in}) and emitter resistor (R_E):

$$X_{C(bypass)} = R_{in} \parallel R_E$$

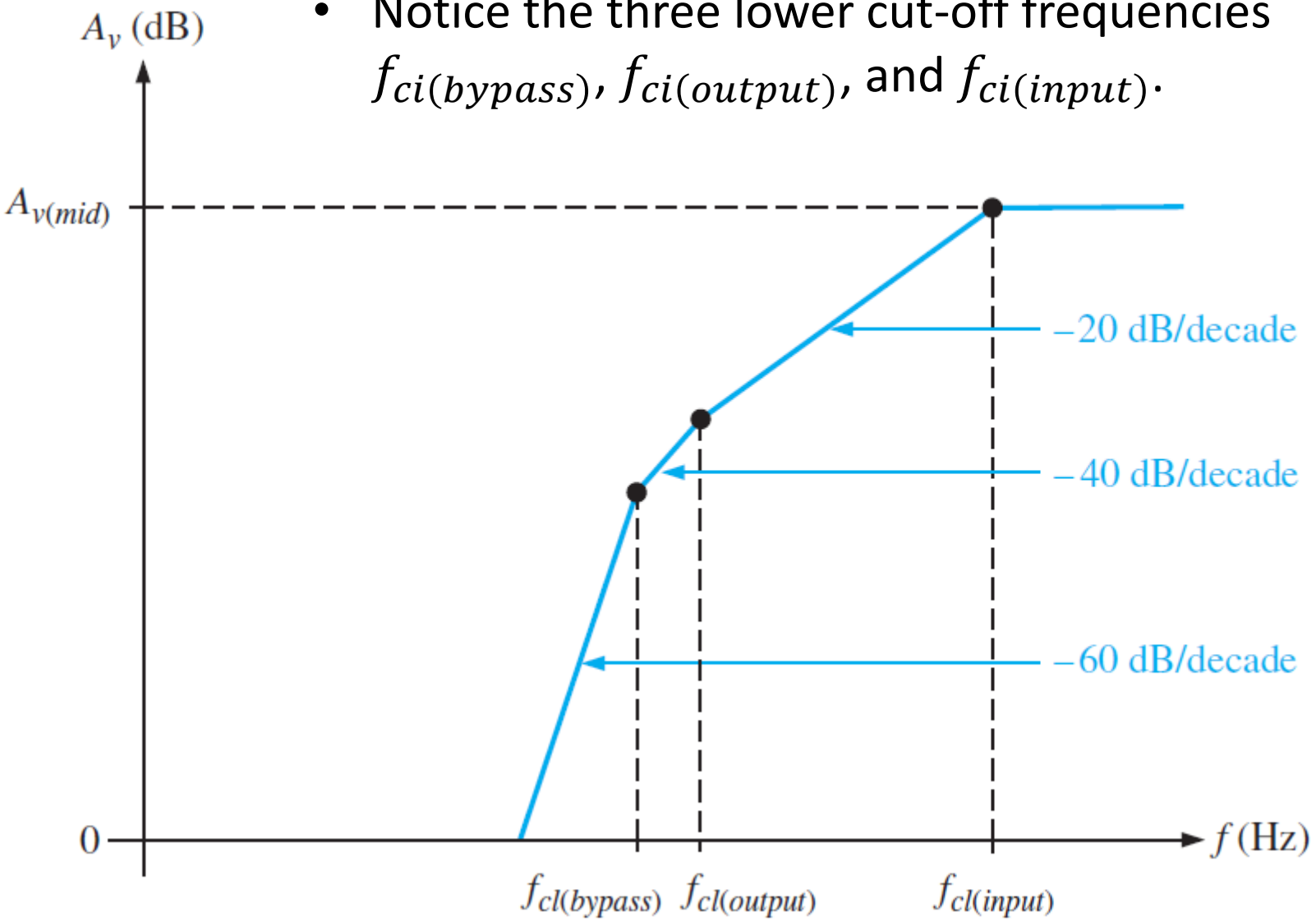
- So, the lower cut-off frequency of the RC circuit at the (bypass) emitter of the amplifier is:

$$f_{cl(bypass)} = \frac{1}{2\pi\left[\left(r'_e + \frac{R_{Th}}{\beta_{ac}}\right) \parallel R_E\right] C_2}$$



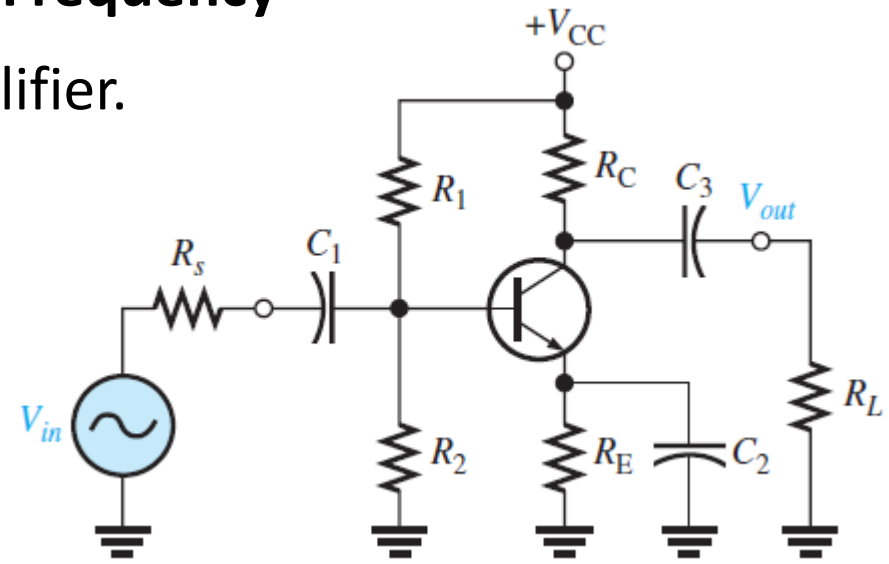


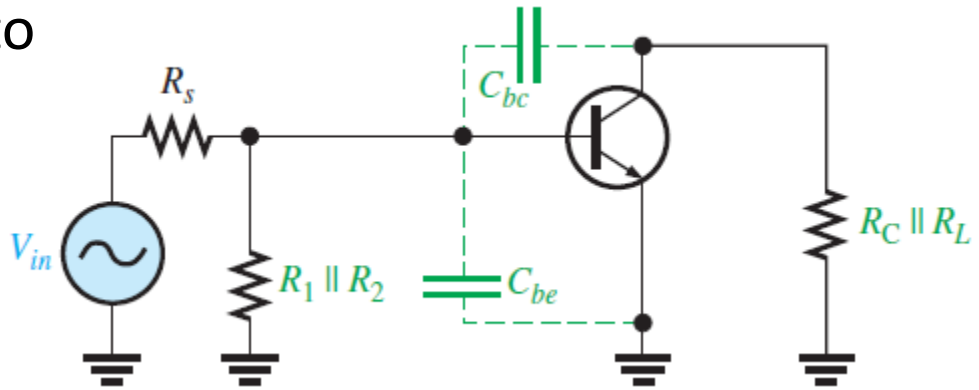
- The frequency response of the BJT amplifier with lower cut-off frequencies.
- Notice the three lower cut-off frequencies $f_{ci(bypass)}$, $f_{ci(output)}$, and $f_{ci(input)}$.



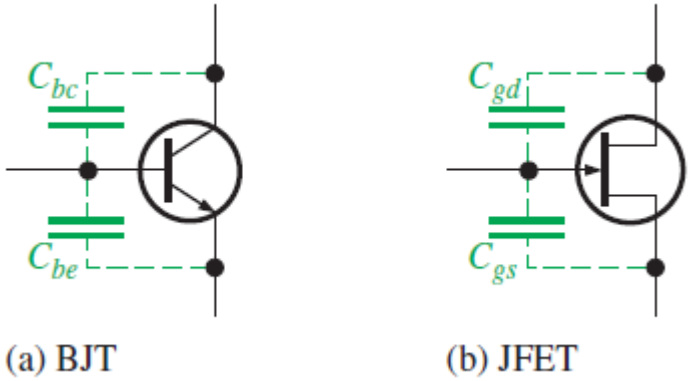
Determining the Upper Cut-Off Frequency

- Capacitively coupled BJT amplifier.
- Internal capacitances, C_{be} and C_{bc} which are significant only at high frequencies.
- High-frequency parasitic capacitances in the BJT:
  - C_{bc} appears as the input capacitance from base to ground.
  - C_{be} simply appears as a capacitance to ac ground.



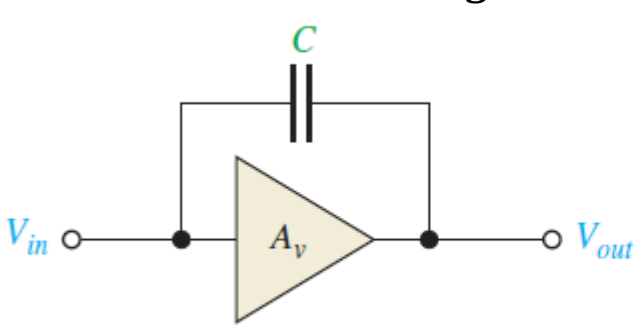


- According to John M. Miller, these parasitic capacitances decrease the gain of a common-emitter amplifier at higher frequencies.
- The amount of negative gain-reducing feedback is related to both current gain and amount of collector-base capacitance.

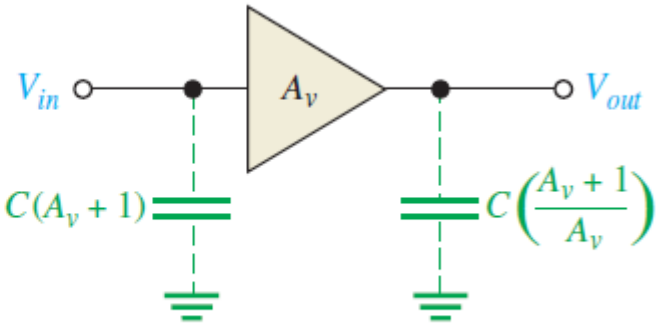


(a) BJT (b) JFET

- General case of Miller input and output capacitances. C represents C_{bc} or C_{gd}.



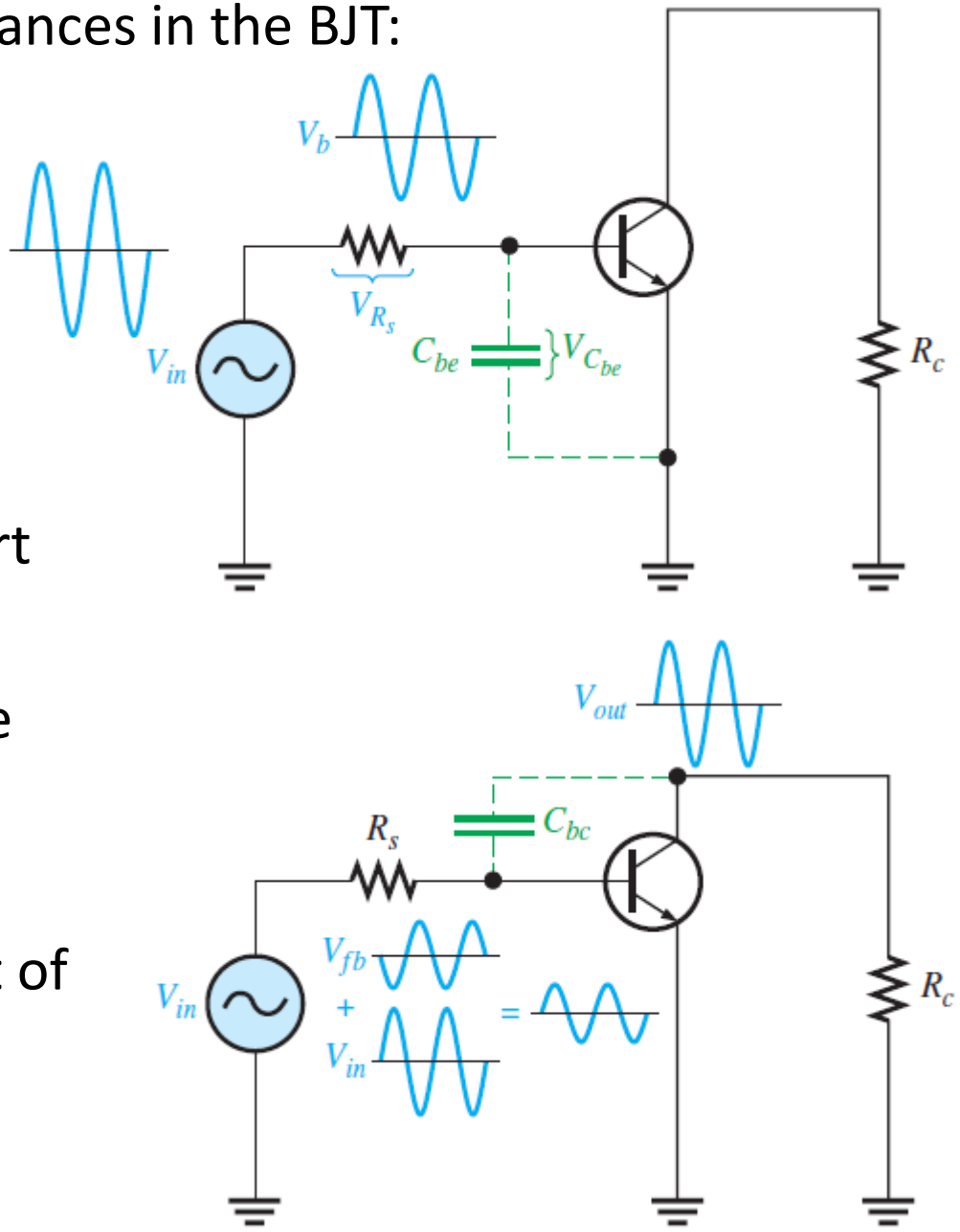
(a)



(b)

Effects of parasitic capacitances in the BJT:

- Effect of C_{be}, where V_b is reduced by the voltage-divider action of R_s and X_{cbe}
- Effect of C_{bc}, where part of V_{out} (V_{fb}) goes back through C_{bc} to the base and reduces the input signal because it is approximately 180° out of phase with V_{in}.



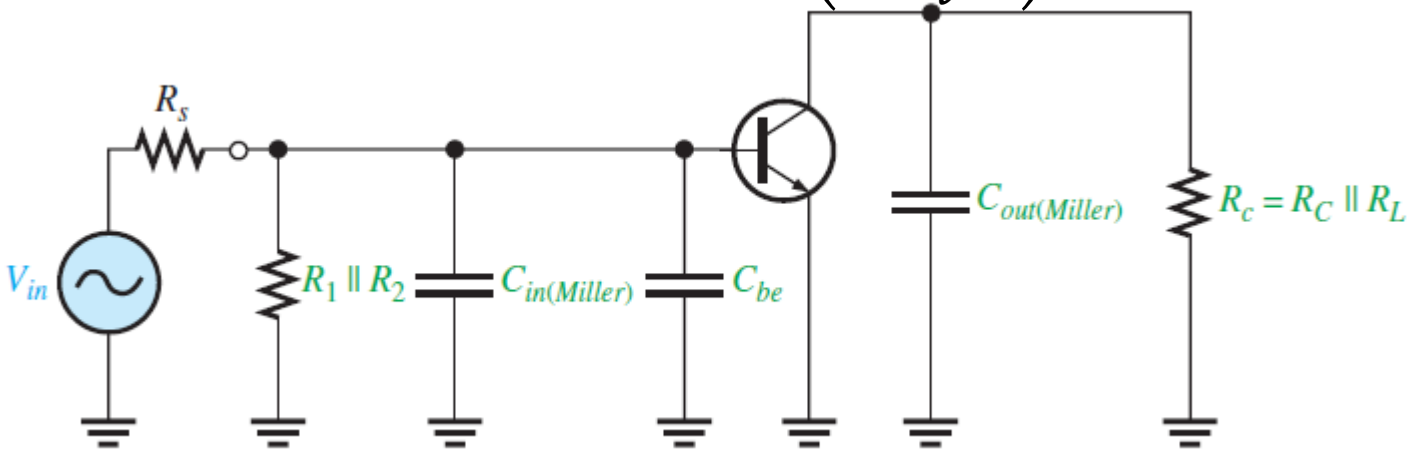
Following Miller's theorem, these parasitic capacitances are:

- C_{be} simply appears as a capacitance to AC ground in parallel with Miller input capacitance.
- C_{bc} appears in the Miller input capacitance from base to ground:

$$C_{in(\text{Miller})} = C_{bc}(A_v + 1)$$

- C_{bc} also appears in the Miller output capacitance (that is also in series with collector resistor):

$$C_{out(\text{Miller})} = C_{bc}\left(\frac{A_v + 1}{A_v}\right)$$



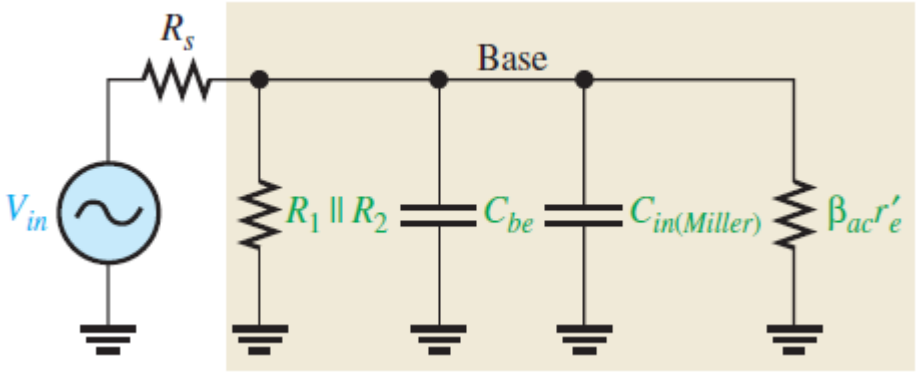
- High-frequency input RC circuit is parallel of Miller input capacitance with base-emitter capacitance and the total impedance at the base:

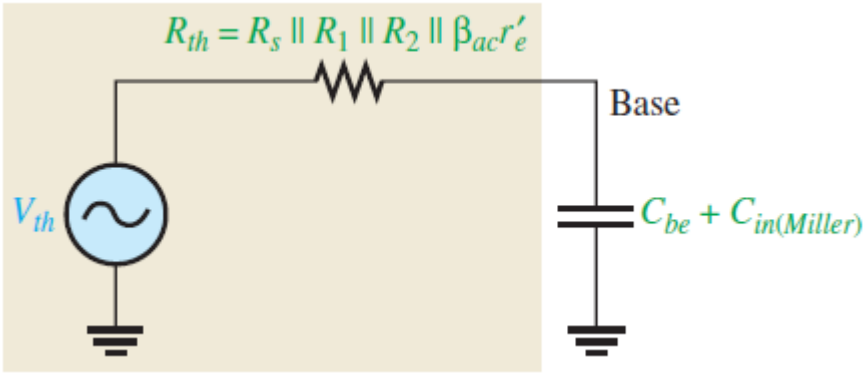
$$X_{C(\text{tot})} = R_s \parallel R_1 \parallel R_2 \parallel \beta_{ac} r_e'$$

- Therefore, the upper cut-off frequency due to parasitic capacitor at the input is:

$$f_{cu(\text{input})} = \frac{1}{2\pi(R_s \parallel R_1 \parallel R_2 \parallel \beta_{ac} r_e')C_{tot}}$$

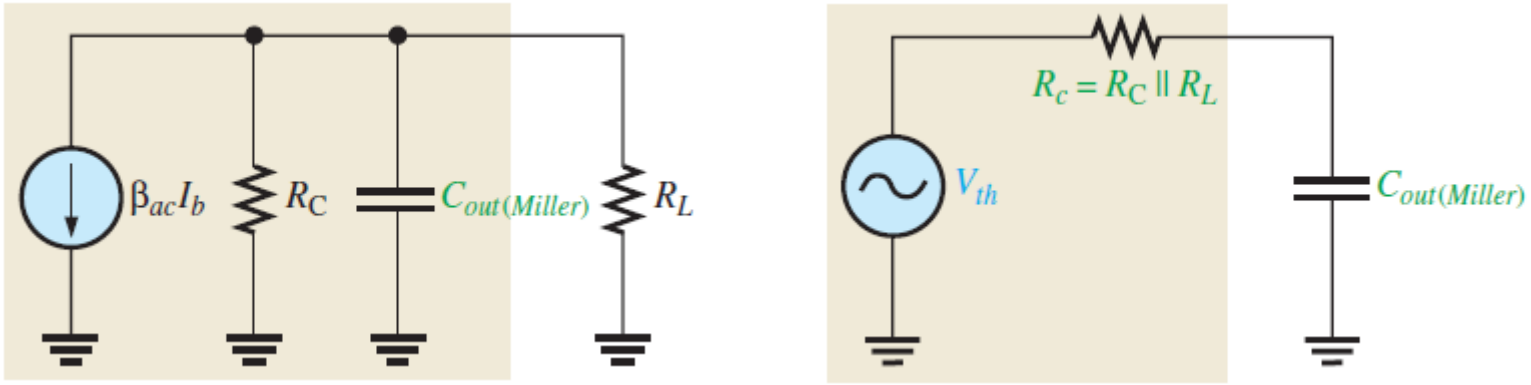
Where: $C_{tot} = C_{be} + C_{in(\text{Miller})}$



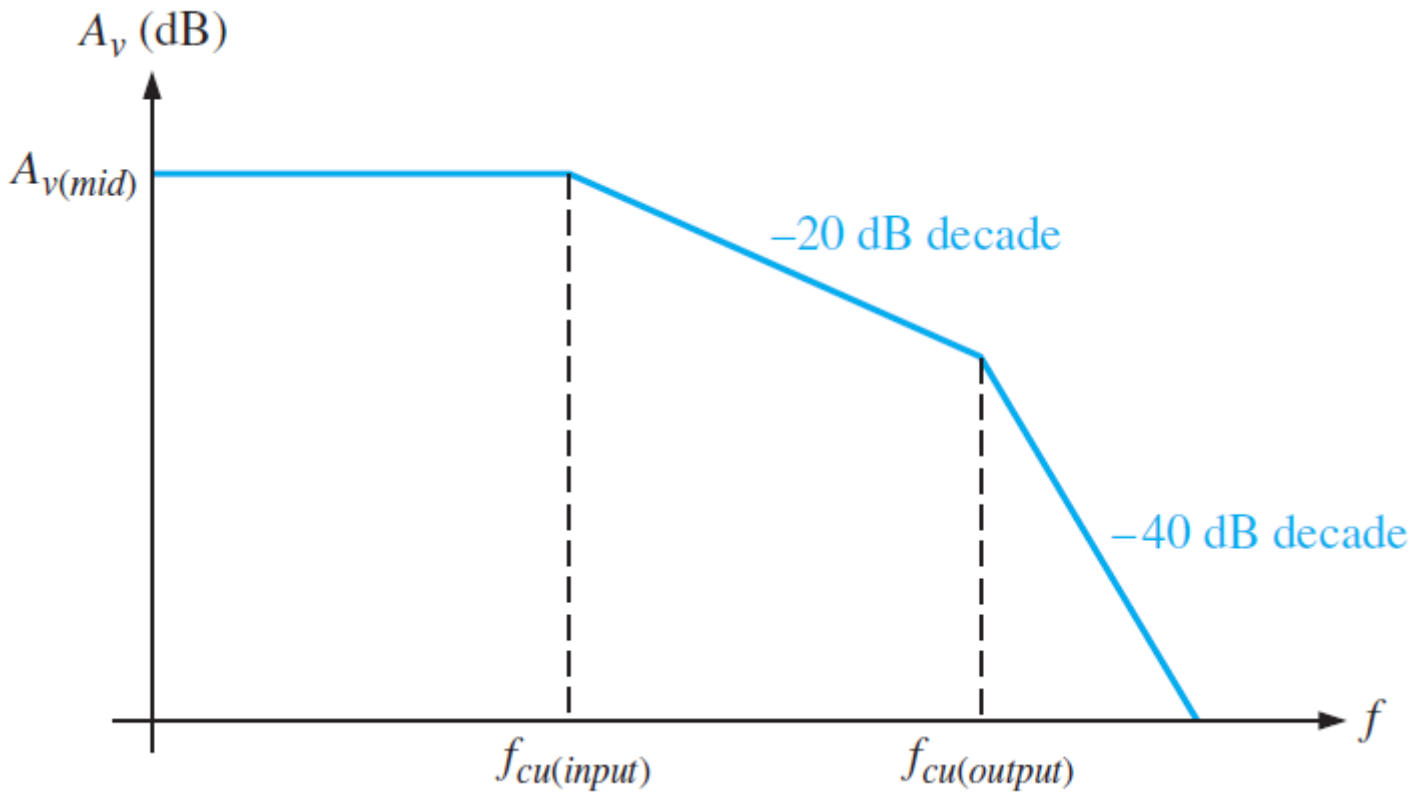


- High-frequency output RC circuit is formed by the Miller output capacitance and the resistance looking in at the collector.
- The impedance at the collector is a parallel combination of collector resistor and load resistor e.g. $R_C \parallel R_L$.
- The upper cut-off frequency due to parasitic capacitor at the output is:

$$f_{cu(\text{output})} = \frac{1}{2\pi(R_C \parallel R_L)C_{out(\text{Miller})}}$$



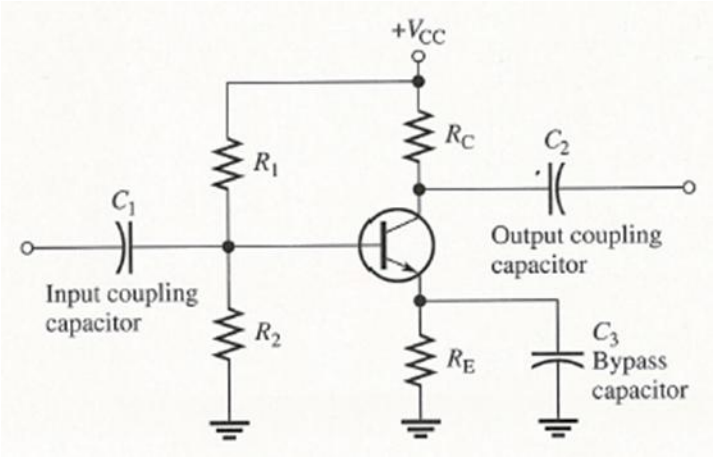
- The frequency response of the BJT amplifier with upper cut-off frequencies.
- Notice the two upper cut-off frequencies $f_{cu(input)}$ and $f_{cu(output)}$.



6. Design Procedures

- Given the following BJT amplifier circuit. Need to select components for the following functions:

1. C_1 is to capacitive couple the I/P signal to the base. Blocks DC component of this signal to the base.



2. C_2 is to block any DC component of the O/P signal. Only amplified AC component will then appear at V_{out}.

3. R_1 and R_2 provide a voltage dividing network on the input to ensure that BE junction is forward biased at a stable voltage.

4. R_C and R_E provide a voltage dividing network on the output side to ensure the transistor is operating in the active region with the correct Q point. R_E acts as a negative feedback to stabilise the gain to variations in β and R.

5. C_E is a bypass capacitor to short the AC signal around the emitter resistor and increase voltage gain.

Design Overview

- Design example of a basic transistor-based amplifier and use of an emitter bypass capacitor.
- Heuristic BJT amplifier design processes are:
  1. Overall design – gain, maximum output voltage swing.
  2. Q-point determination – collector current and collector-emitter voltage.
  3. Biasing circuit design – input and output resistors.
  4. Values of capacitors – coupling capacitors and bypass capacitor.

Example 1 – Basic BJT Amplifier Design with Input Coupling Capacitor

- Design a single stage amplifier using a NPN transistor to give a small signal voltage gain of -4 and a maximum peak-to-peak voltage swing of 10 V when used with a high impedance load. The amplifier is expected to have a rating output current of 1 mA.
- It should operate from a 15 V supply and be AC coupled with a gain of the amplifier that is approximately constant down to 100 Hz.
- Do your design without the use of an emitter bypass capacitor. Then, add an emitter bypass capacitor of 22 µF and calculate how this will influence your gain.

a. What the basic amplifier circuit look like? [4 marks]

b. Sketch the load line and determine the Q-point for DC bias. [12.5 marks]

c. Calculate values of collector resistor (R_C), actual voltage gain (A_v), and emitter resistor (R_E). [7.5 marks]

d. Calculate values of base bias resistors (R_1 and R_2). [12.5 marks]

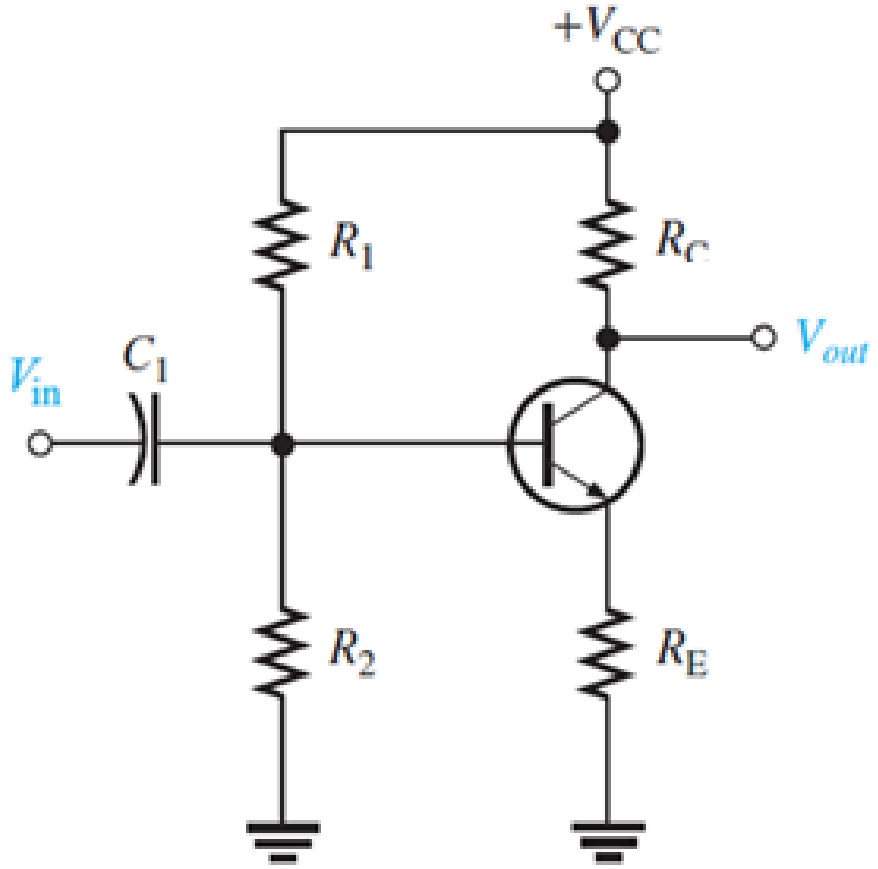
e. Considering the effect of input resistance, determine the input coupling capacitor. [7.5 marks]

f. Add an emitter bypass capacitor of 22 µF and calculate how this will influence your gain. [6 marks]

a. What should the basic circuit look like ?

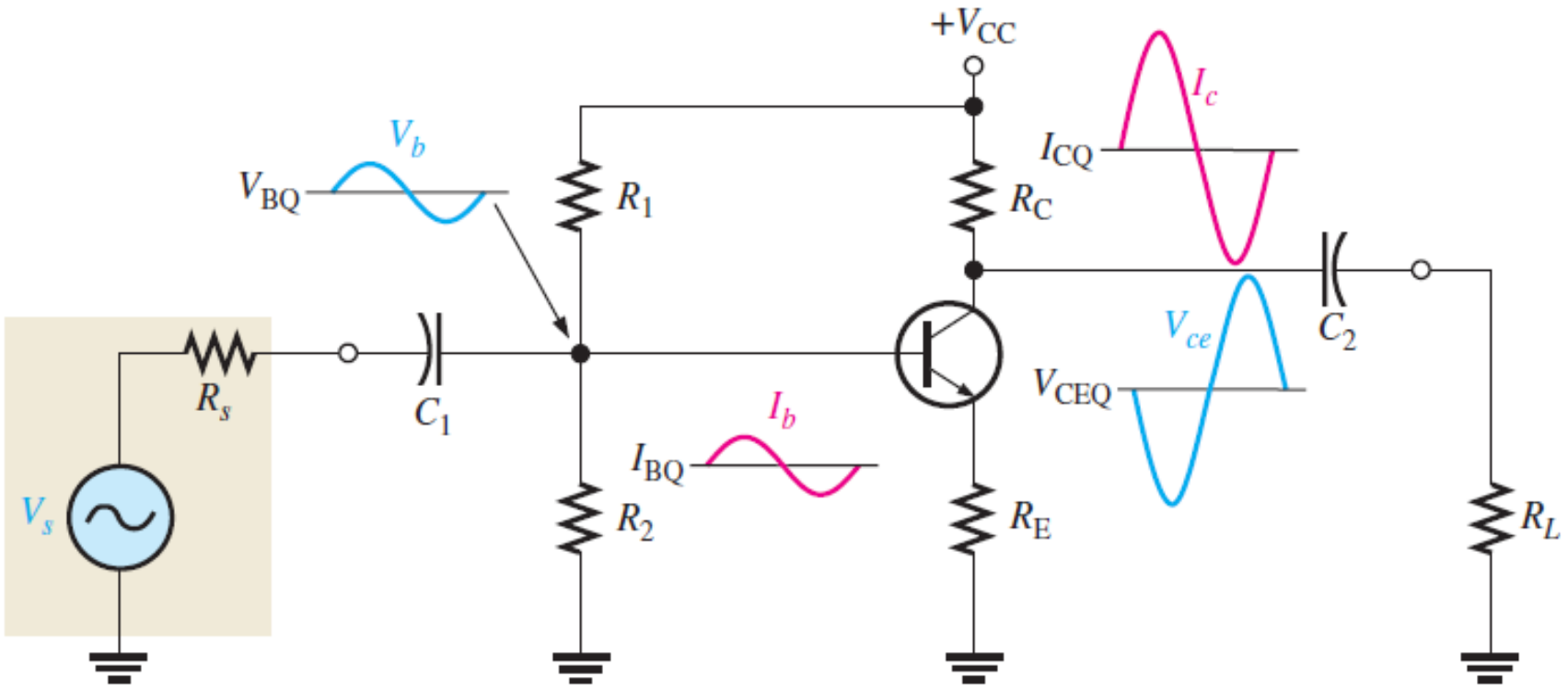
- We will design a common emitter configuration with a feedback resistor as discussed before.

- Important to realise that there will not be any single correct answer i.e. your circuit will depend on the assumptions, design choices and trade-offs you make along the way.



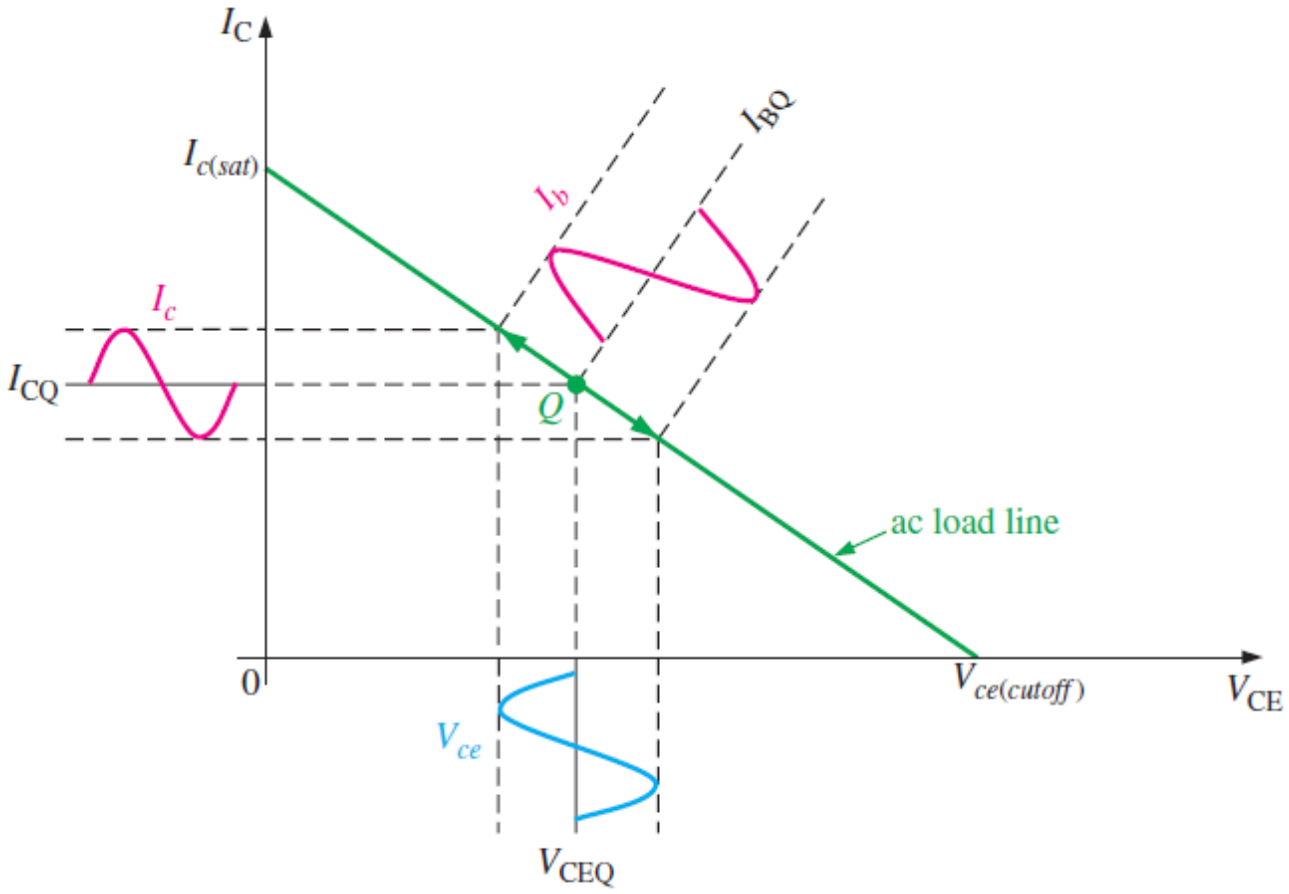
b. Decide on a Q point of operation for DC bias.

- We need to accommodate a large voltage swing of 10 V peak-to-peak.
- So, the operating point needs to be at least 5 V above ground and at least 5 V below the positive voltage supply.



Decide on a Q point of operation for DC bias.

- Choose V_{CQ} to be ≈ 9.5 V, i.e. 5.5 V below V_{CC} = 15 V,



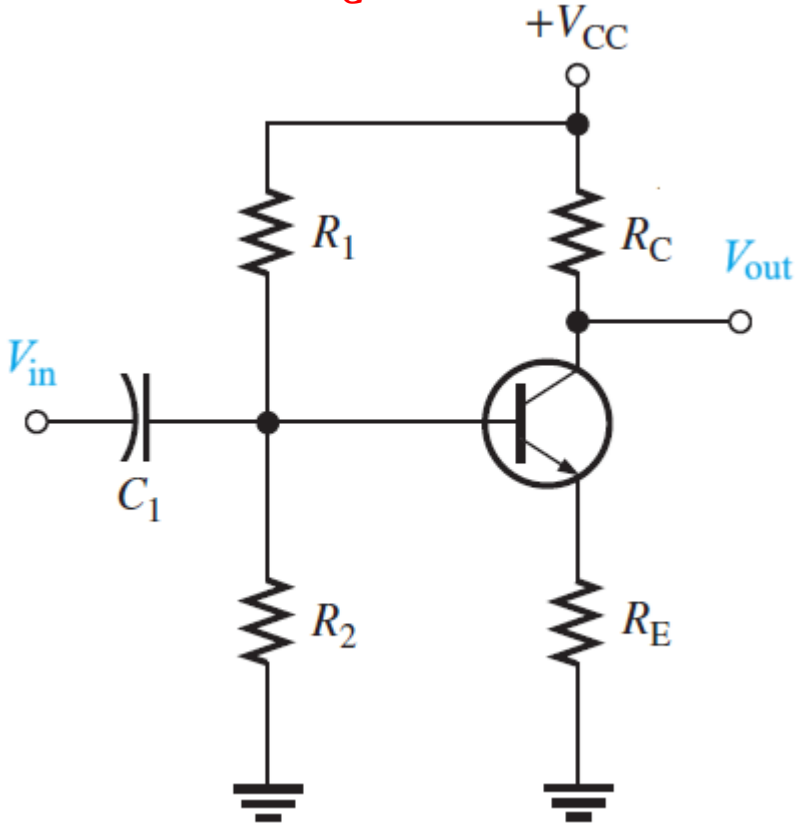
c. Decide on output resistors for the Q point of operation for DC bias.

- Must now decide on a suitable collector current = rating output current of the amplifier.
- As the load impedance is high – decide on $I_C \approx 1$ mA.
- Calculate a value for R_C:

$$R_C = \frac{V_{CC} - V_{CQ}}{I_C}$$

$$= \frac{15\text{ V} - 9.5\text{ V}}{1\text{mA}} = 5.5\text{ k}\Omega$$

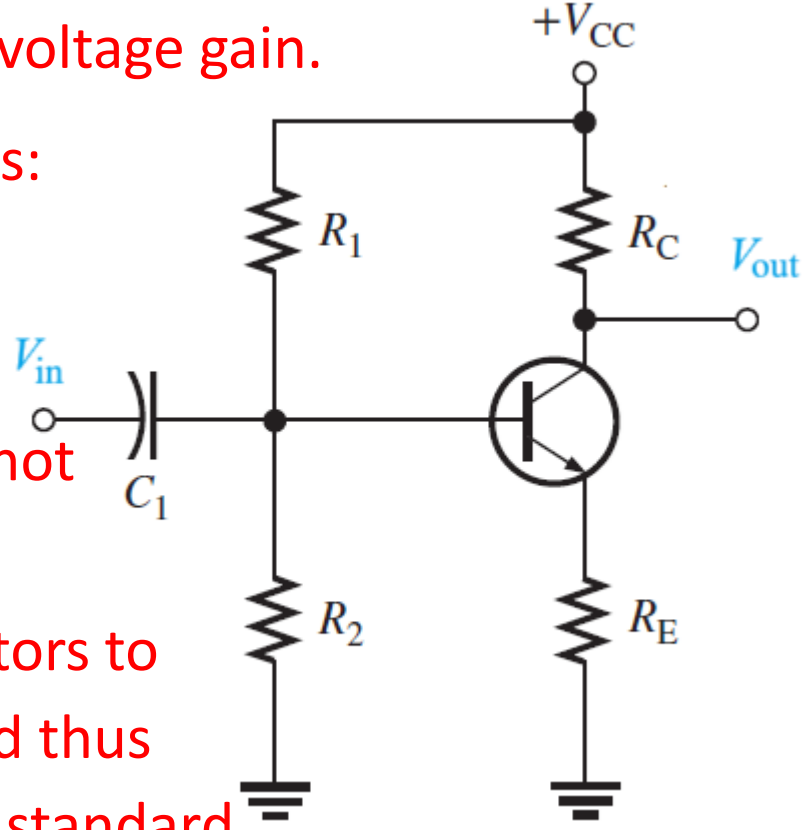
- As 5.5 kΩ is not a standard resistor value, choose the closest E12 value, i.e. 5.6 kΩ.



Choose R_E to meet the small-signal voltage gain.

- The voltage gain of the amplifier is:

$$A_v = -4 = -\frac{R_C}{R_E} = \frac{5.6\ \text{k}\Omega}{R_E}$$



- So that R_E = 1.4 kΩ which is also not a standard transistor value.
- We can use combinations of resistors to obtain the desired value of R_E and thus A_v, or we can choose the nearest standard resistor value and accept that the gain will be slightly off.
- Choose R_E = 1.3 kΩ, so that the voltage gain should be:

$$A_V = -\frac{R_C}{R_E} = \frac{-5.5\ \text{k}\Omega}{1.3\ \text{k}\Omega} = -4.2$$

d. Calculation of base bias resistors:

- The Q point voltage at the emitter can now be calculated by assuming $I_E \approx I_C \approx 1$ mA. Thus:

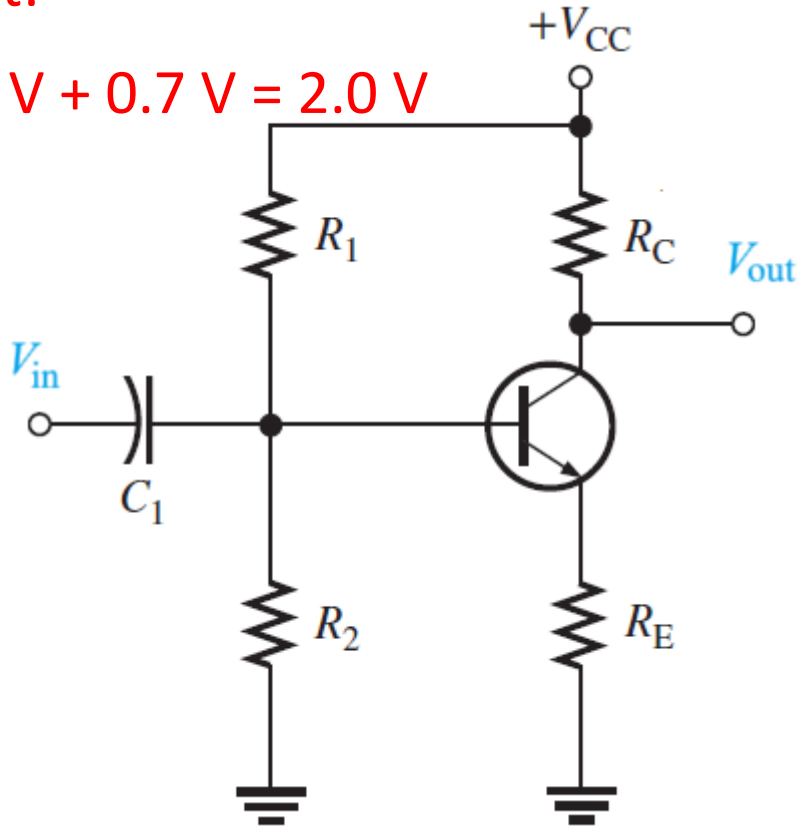
$$V_{EQ} = I_{EQ} R_E = (1\text{ mA})\,(1.3\text{ k}\Omega) = 1.3\text{ V}$$

- The base voltage must then be at:

$$V_B = V_{EQ} + V_{BE} = 1.3\text{ V} + 0.7\text{ V} = 2.0\text{ V}$$

- To achieve this voltage at the base, we can calculate the voltage divider as:

$$V_B = \left(\frac{R_2}{R_1 + R_2}\right) V_{CC} = 2\text{ V}$$

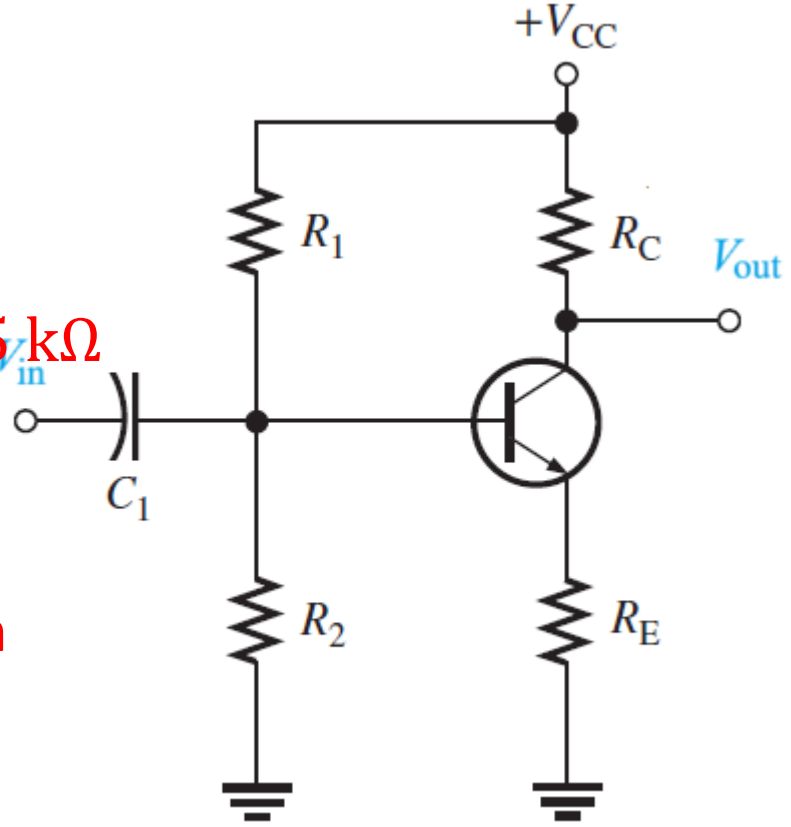


- The choice of values for R_1 and R_2 is a trade-off between high input resistance and a too high current through the base (a basic assumption).
- A good rule of thumb is to make R_2 approximately 10 times R_E. Thus R_2 = (10)(1.3 kΩ) = 13 kΩ and we can calculate R_1 as:

$$R_1 = R_2\left(\frac{V_{CC} - V_B}{V_B}\right)$$

$$= 13\ \text{k}\Omega\left(\frac{15\ \text{V} - 2\ \text{V}}{2\ \text{V}}\right) = 84.5\ \text{k}\Omega$$

- Choose R_1 = 82 kΩ as real resistor value => Make small differences in values of V_B, V_{CQ} and I_E.



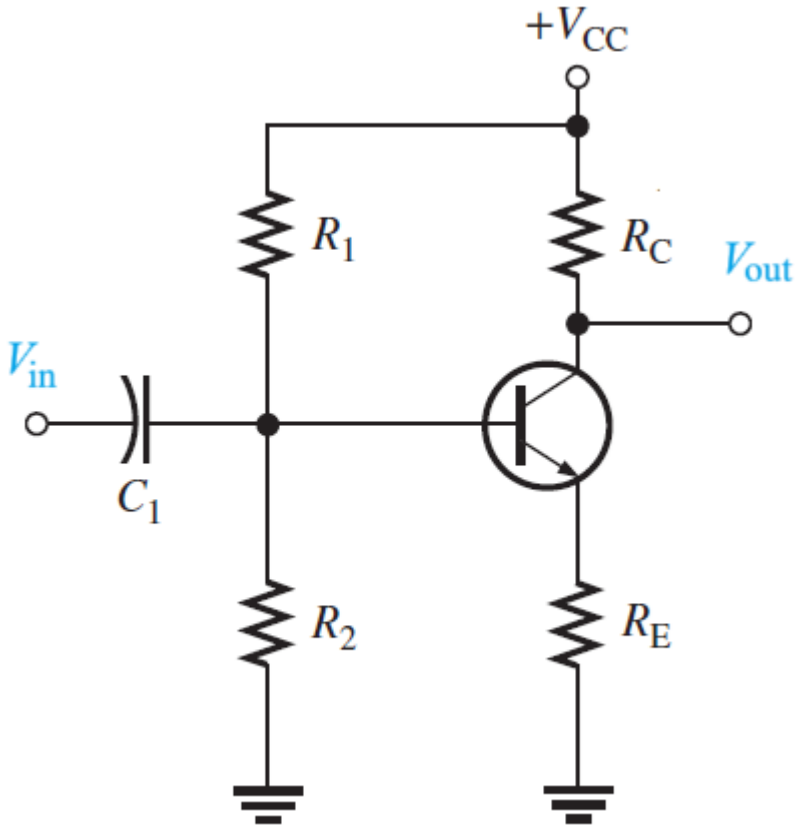
e. Consider the effect of input and output resistances and the choice of coupling capacitors.

- The input resistance into the amplifier is given approximately be the parallel combination of R_1 and R_2 (neglecting any loading from the transistor) so that:

$$R_{in} \approx R_1 \parallel R_2$$

$$= \frac{(13\ \text{k}\Omega)(82\ \text{k}\Omega)}{13\ \text{k}\Omega + 82\ \text{k}\Omega}$$

$$= 11.2\ \text{k}\Omega$$



Because of input resistance, the choice of coupling capacitor is determined as follow.

- The presence of the coupling capacitor will then produce a low frequency cut-off of the signal given by:

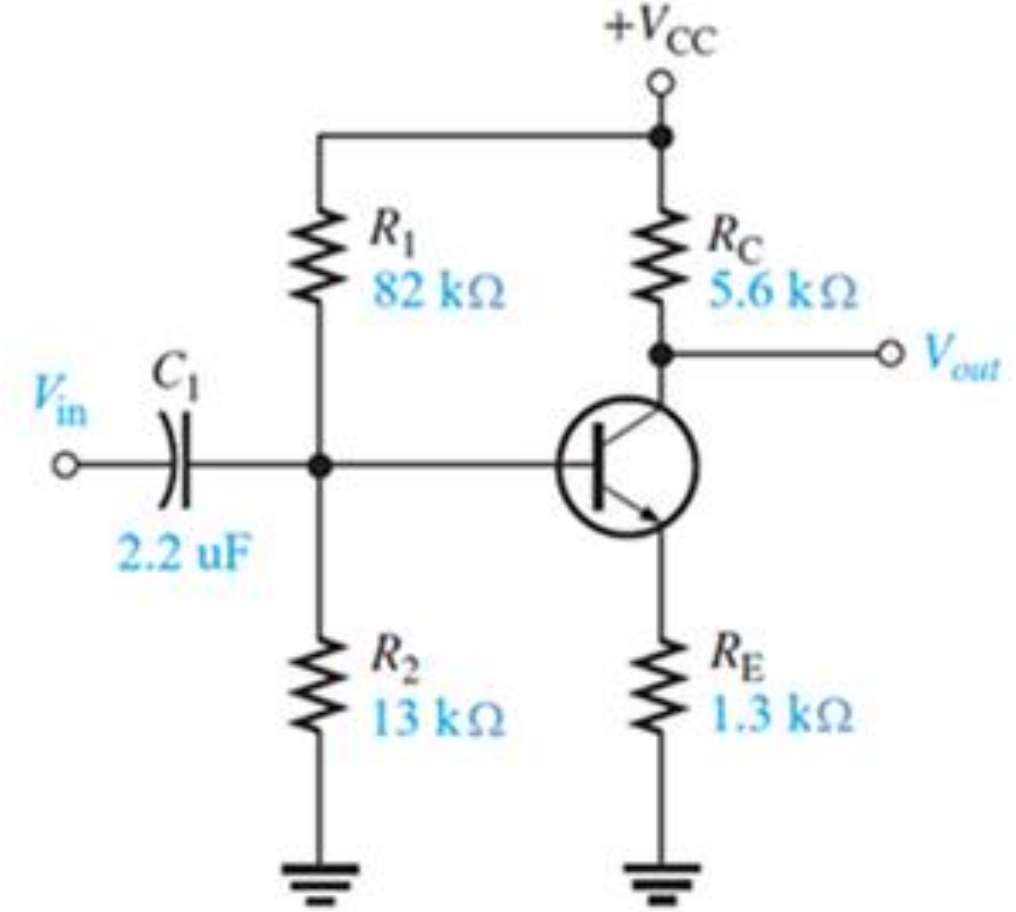
$$f_{C1} = \frac{1}{2\pi C_1 R_{in}}$$

- Design requirements needed to gain to be approximately constant down to 100 Hz i.e. choose the low frequency cut-off ~ 10 times lower than that i.e. 10 Hz:

$$C_1 = \frac{1}{2\pi f_C R_{in}} = \frac{1}{2\pi(10)(11.2 \times 10^3)} = 1.4\ \mu\text{F}$$

- Use a non-polarised capacitor of value > 1.4 µF – e.g. 2.2 µF.

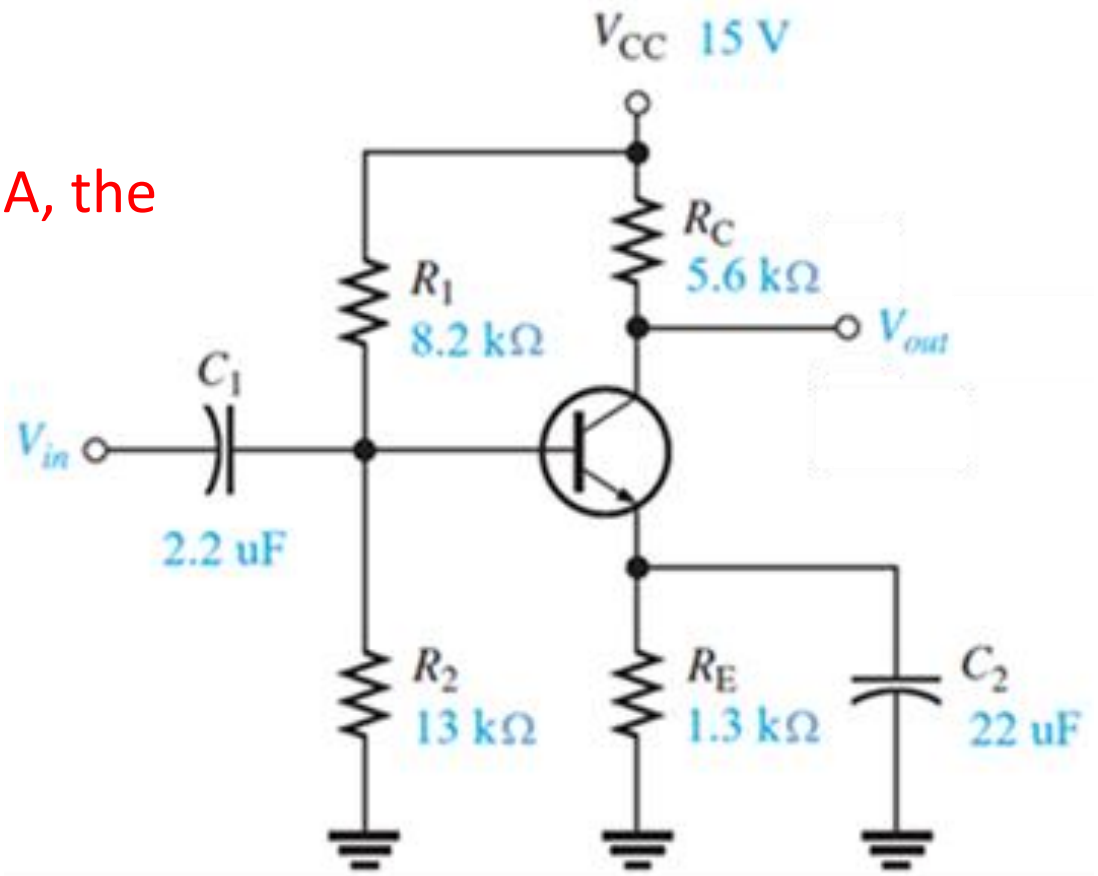
- The final circuit design of the common-emitter BJT amplifier with the calculated values of the components:
  - $R_1 = 82\ \text{k}\Omega$
  - $R_2 = 13\ \text{k}\Omega$
  - $R_C = 5.6\ \text{k}\Omega$
  - $R_E = 1.3\ \text{k}\Omega$
  - $C_1 = 2.2\ \mu\text{F}$



f. Knowing that I_E = 1 mA, the value of AC emitter resistance is:

$$r_e' = \frac{25\ \text{mV}}{I_E}$$

$$= \frac{25\ \text{mV}}{1\ \text{mA}} = 25\ \Omega$$



- With the emitter bypass capacitor in place, the voltage gain of the amplifier is:

$$A_v = -\frac{R_C}{r_e'} = -\frac{5.6\ \text{k}\Omega}{25\ \Omega} = 224$$

Further BJT Amplifier Design

There are two exercises that you could attempt by yourself to extend your BJT amplifier design skills and knowledge.

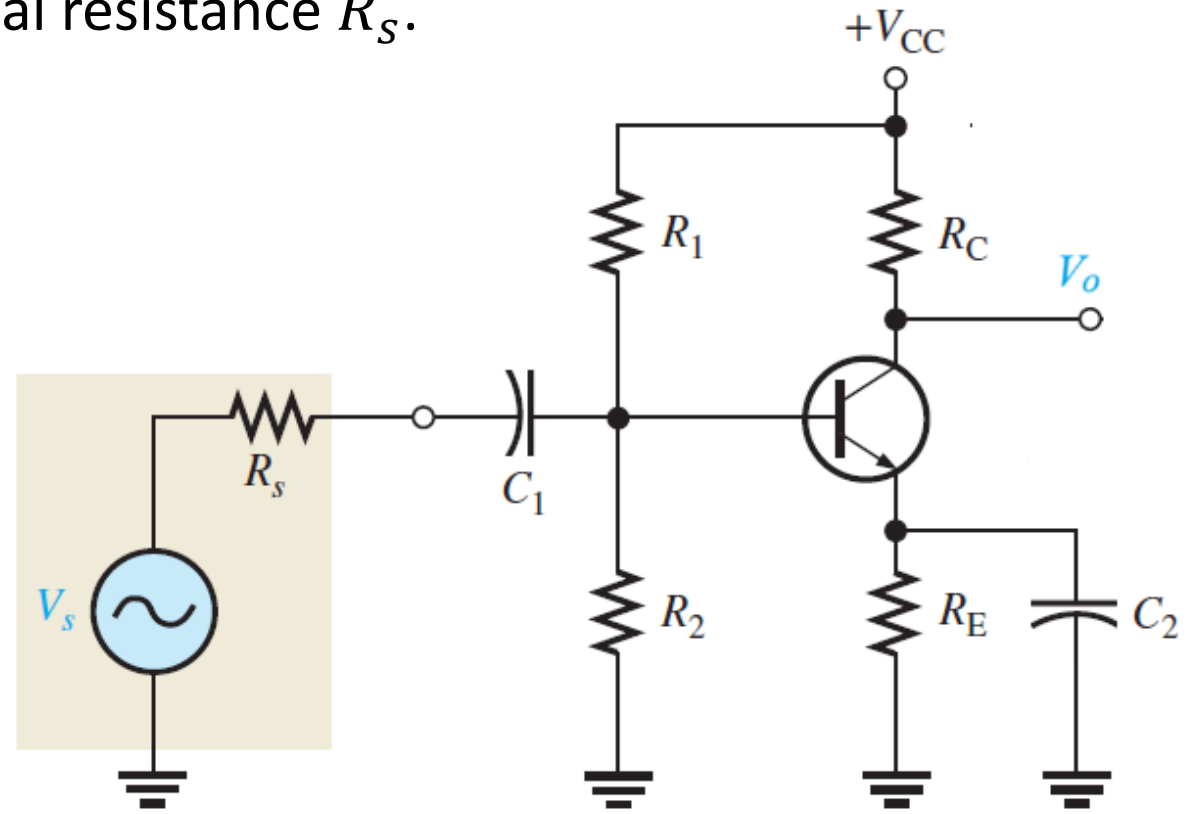
It is important that through these exercises you could determine the more precise values of the components used in the amplifier circuit.

The BJT amplifier is then enhanced further with bypass capacitor for more voltage gain of the amplifier and swamping resistor to stabilise the operating condition of the amplifier.

We need to determine also the other components that will be required for realising common-emitter BJT amplifier with feedback resistor and bypass emitter capacitor.

Exercise 2 – Design of BJT Amplifier with Emitter Bypass Capacitor and Input Voltage Source

Extend further the example design of BJT amplifier including the emitter bypass capacitor and an input voltage source with an internal resistance R_s.



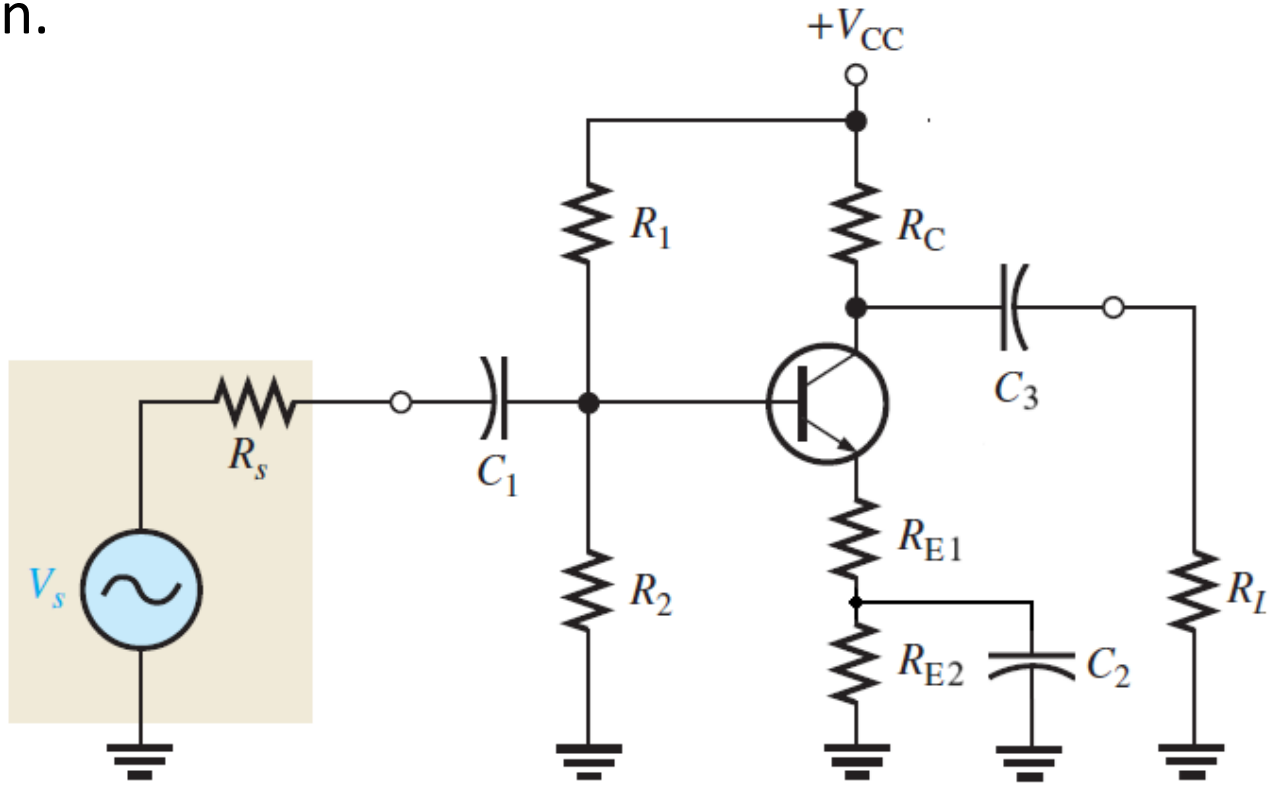
a. Calculate the value of the emitter bypass capacitor if the frequency of the operation of the BJT amplifier is constant down to 100 Hz. [10 marks]

b. Calculate the actual voltage gain of the amplifier with the emitter bypass capacitor included. [4 marks]

c. If we consider the input loading of the transistor and the input terminal of the amplifier is connected to a voltage source with internal resistance of 10 Ω, calculate the value of input coupling capacitor. Assume that the gains of the BJT, $\beta_{dc} = \beta_{ac}$ = 100. [6 marks]

Exercise 3 – Design of BJT Amplifier with Swamping Resistor, Load Resistor, and Output Coupling Capacitor

- Extend the given amplifier design in the Exercise 2 by adding a swamping resistor at the emitter leg of the transistor.
- This resistor is included to improve the stability of the amplifier gain.



- The AC voltage gain is dependent on r_e' since $A_v = R_C/r_e'$.
- Also, r_e' depends on I_E and on temperature. This causes the gain to be unstable over changes in temperature.

For the BJT amplifier circuit with swamping resistor as shown in the given figure:

a. Calculate the value of the swamping resistor (R_{E1}) at the emitter. Determine the voltage gain of the amplifier after the inclusion of the swamping resistor. [4 marks]

b. If the output of the amplifier is connected to a load resistor of 8 Ω, calculate the value of the coupling capacitor at the output of the amplifier. [4 marks]

c. With the voltage gain of the amplifier as calculated in part (a) and knowing that the values of parasitic capacitances $C_{bc} = 1.2$ pF and $C_{be} = 10$ pF from the datasheet of the BJT, estimate the cut-off frequencies in the input and output terminals of the amplifier at high frequency. [16 marks]