VICTORIA UNIVERSITY OF WELLINGTON TE HERENGA WAKA NEW ZEALAND

XMUT204 Electronic Design

Note 3c: BJT Switches

1. Electrical/Electronic Switches in Circuits

The first application of the BJT that we will cover in the course is its application for switching circuit.

1.1. Introduction

We are well familiar with the use of mechanical ON/OFF switches in circuits which will make/break a circuit, but we often need for one part of a circuit to be able to switch ON/OFF a secondary circuit.

The status of the secondary circuit will this depend on the status of the primary circuit(s). One method to do this is by electromechanical relays:

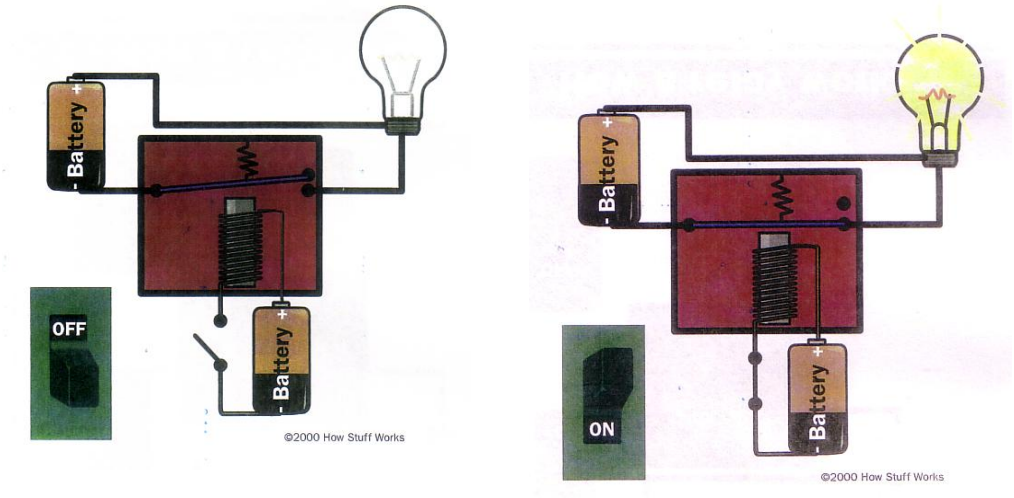


Figure 1: Illustration of mechanical on/off switch circuits.

1.1. The Use of Electrical/Electronic Switches in Circuits

Parts of a typical relay, its contact is either on or off depending on the states of coil.

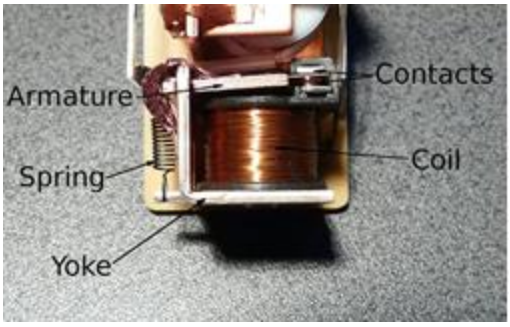


Figure 2: A layout of a typical relay switch.

However, for several reasons, the use of transistors has totally replaced relays as switching elements, particularly in low current applications.

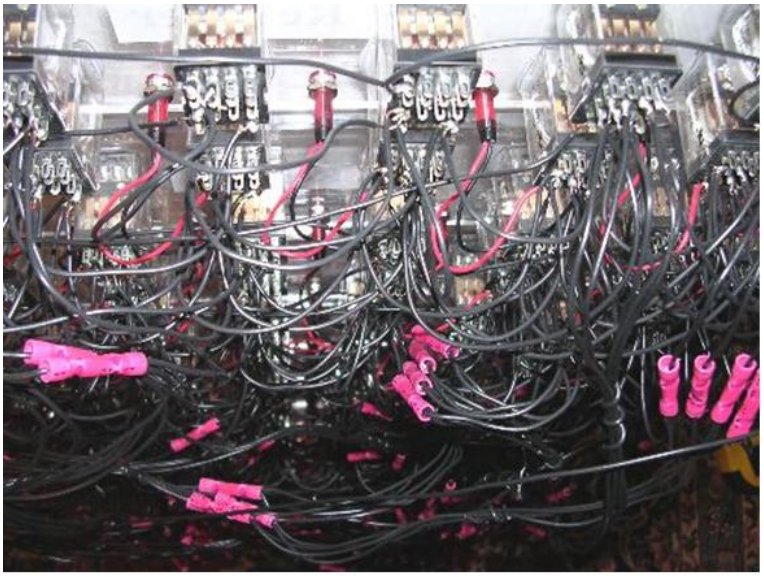
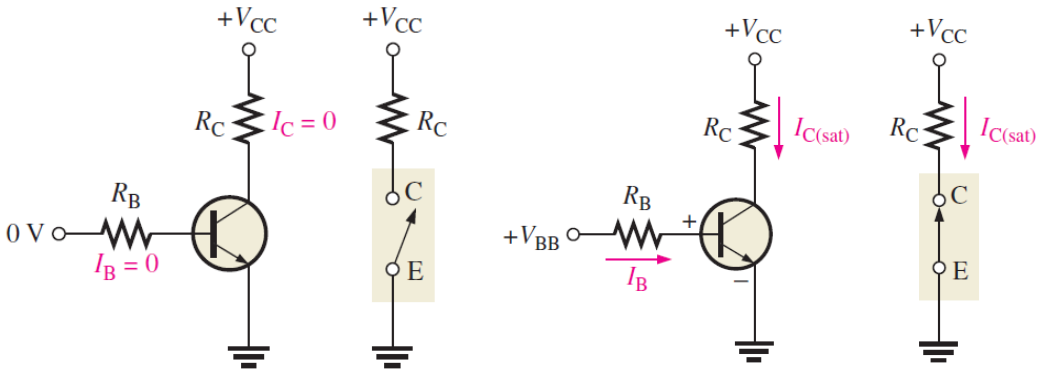


Figure 3: Mechanical switches use in industrial applications.

2. Using the Transistor as a Switch

We can use the transistor as an ON – OFF switch by switching it between the cut-off region (transistor OFF and I_C = 0) and the saturation region (transistor ON and I_C = max).



Transistor OFF, Open switch, Cut-off mode

Transistor ON, Closed switch, Saturation mode

Figure 4: Use of BJT transistors as switches.

To be able to do this efficiently, let's have another look at the output curves of a common emitter NPN transistor.

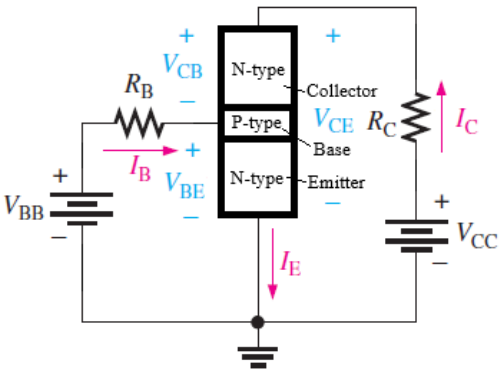


Figure 5: NPN transistor in the common emitter configuration.

As shown above, when an NPN transistor in the common emitter configuration, the base current as set by V_{BB} and R_B provide biasing current to the BJT transistor. This current will turn on the transistor.

As a result, collector current flows in the collector, I_C and emitter, I_E (as set by V_{CC} and R_C) and across the collector and emitter of the transistor, you will observe voltage drop (V_{CE}).

3. The Output Current–Voltage Characteristics

To be able to do biasing efficiently, let's have another look at the output characteristic curves of a common emitter NPN transistor. The following diagram shows a graph of output current vs. voltage characteristics of the switching operation of the BJT transistor.

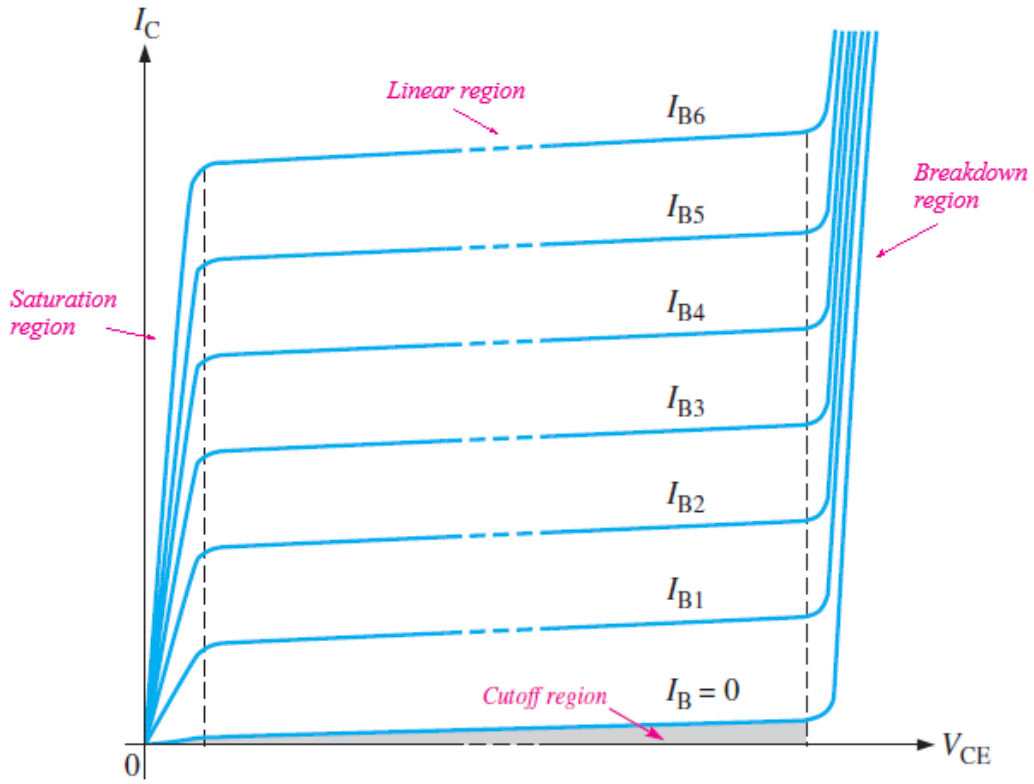


Figure 6: The output I-V characteristics of BJT transistor.

For the **cut-off region**, we have I_B = 0, thus I_C =0 and the whole transistor is OFF. In this condition, V_{BE} < 0.7 V and the BE junction then essentially reverse biased, i.e. open circuit.

For the **active region**, we have V_{BE} = 0.7 V, so the BE junction is forward biased. In this condition, the CB junction is reverse biased, I_B > 0 and we have $I_C = \beta I_B$. As a result, the transistor is ON in the mode typically used for amplification.

But what is the reason for transistor behaviour in the **saturation region**? In this region, we would have V_{BE} = 0.7 V, so the BE junction is forward biased. V_{CE} would be very

small i.e. if this is the case we will have $V_{CE} \sim 0$ V. The BC junction will thus be forward biased i.e. both the junctions are forward biased, and transistor appears as a short. This region is modelled as a constant voltage drop of V_{CE} = 0.2 V. Furthermore, β is smaller than the β value in the active region.

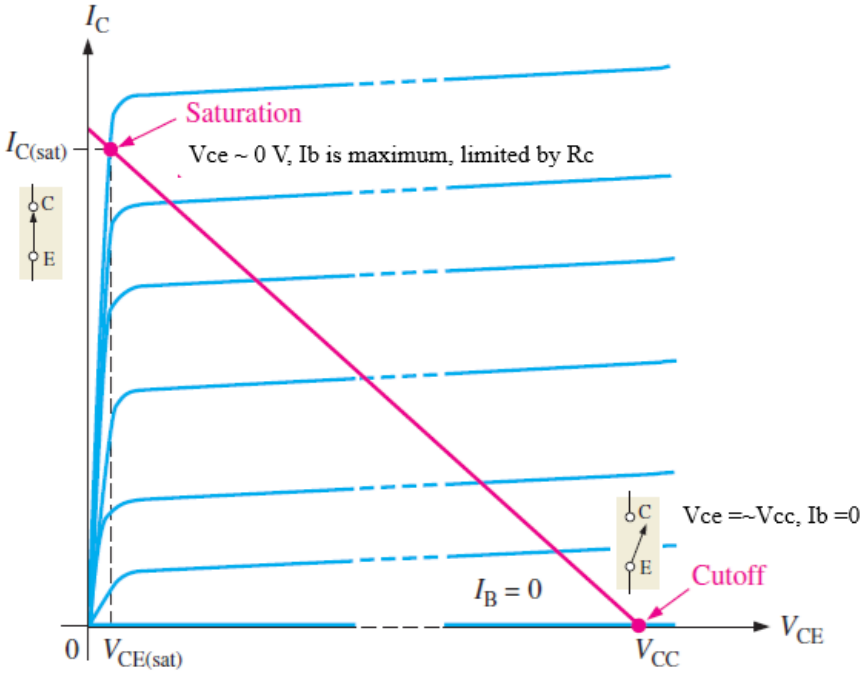


Figure 7: NPN BJT output characteristics.

We need to switch efficiently between the cut-off point and saturation point of operation. As shown in the diagram below, the cut-off and saturation points of the operation of the BJT. Also notice the intersection between this line with curves of the BJT output voltage at various base currents (I_B).

4. **BJT Switching Operation**

The operation of a BJT as a switching device is easy to understand especially if you have already learned how to make a BJT operate in the cut-off and saturation region. A BJT acts like an open switch when it operates in the cut-off region.

In figure below, you can see that the NPN BJT is operating in the cut-off region since the voltage at the base terminal is 0 V. Therefore, the base-emitter junction is not forward-

biased and if we will not consider the leakage current, all the currents, I_B and I_C are zero. You can also see in figure below that the collector and emitter terminals act like an open SPST switch. Since I_C is zero, the voltage across the collector and emitter terminal, $V_{CE(\text{cutoff})}$, is equal to V_{CC}.

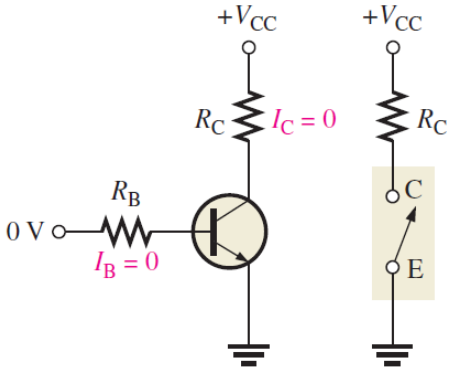


Figure 8. An NPN BJT operating in the cut-off region acts like an open switch.

So, for a BJT to act as an open switch, all you need to do is to make sure that its base-emitter junction is not forward-biased.

Now, for a BJT to act as a closed switch, it needs to operate in the saturation region. In figure below, we have assumed that the NPN BJT is operating in the saturation region. As you can see, the collector and emitter terminals act like a closed SPST switch.

Ideally, there is basically a short between the collector and emitter, and the voltage drop across it should be zero. However, there is a small voltage drop across the collector and emitter terminals which is known as the saturation voltage, $V_{CE(\text{sat})}$.

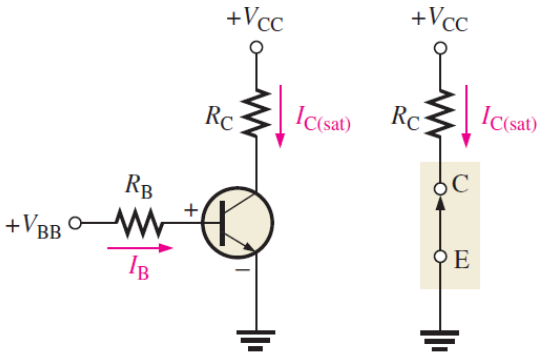


Figure 9. An NPN BJT operating in the saturation region acts like a closed switch.

For a BJT to operate in the saturation region, the base-emitter junction and base-collector junction should be forward-biased, and there should be a sufficient base current to produce the collector saturation current, $I_{C(\text{sat})}$. Using the circuit in figure above, the formula to calculate the $I_{C(\text{sat})}$ is:

$$I_{C(\text{sat})} = \frac{V_{CC} - V_{CE(\text{sat})}}{R_C}$$

The $I_{C(\text{sat})}$ is the current that the load R_C requires. $V_{CE(\text{sat})}$ is specified in the datasheet of the BJT that you are going to use. After calculating $I_{C(\text{sat})}$, the next thing to figure out is the minimum base current, $I_{B(\text{min})}$, needed to make sure to produce $I_{C(\text{sat})}$. You can use this equation to calculate $I_{B(\text{min})}$.

$$I_{B(\text{min})} = \frac{I_{C(\text{sat})}}{\beta_{DC}}$$

To make sure that the BJT is operating in the saturation region, you just need to make sure that I_B is greater than $I_{B(\text{min})}$.

5. What DC Beta to use?

Now, if you know the $V_{CE(\text{sat})}$ of the BJT, the voltage drop across the load and its resistance, you can calculate $I_{C(\text{sat})}$ then calculate $I_{B(\text{min})}$. However, you may wonder, what is the value of β_{DC}?

To make it easier for you to find out, the clue is you can find β_{DC} on the BJT datasheet that you will use. So, let's check the datasheet of a very commonly used NPN general purpose transistor, the 2N3904.

ON CHARACTERISTICS		Symbol	Min	Max	Unit
DC Current Gain (Note 2)		h_{FE}			–
(I_C = 0.1 mAdc, V_{CE} = 1.0 Vdc)	2N3903		20	–	
	2N3904		40	–	
(I_C = 1.0 mAdc, V_{CE} = 1.0 Vdc)	2N3903		35	–	
	2N3904		70	–	
(I_C = 10 mAdc, V_{CE} = 1.0 Vdc)	2N3903		50	150	
	2N3904		100	300	
(I_C = 50 mAdc, V_{CE} = 1.0 Vdc)	2N3903		30	–	
	2N3904		60	–	
(I_C = 100 mAdc, V_{CE} = 1.0 Vdc)	2N3903		15	–	
	2N3904		30	–	

Table 1: The DC beta (i.e. h_{FE}) values of 2N3904 BJT.

If you checked the datasheet of 2N3904, you could find something that is like what is shown in figure above. Since DC beta (β_{DC}) is equivalent to the hybrid parameter (h_{FE}), you may think that this is where you are going to get the value of β_{DC} to solve for $I_{B(\min)}$.

Characteristic	Symbol	Min	Max	Unit
Collector – Emitter Saturation Voltage (Note 2) (I_C = 10 mAdc, I_B = 1.0 mAdc) (I_C = 50 mAdc, I_B = 5.0 mAdc	$V_{CE(sat)}$	 – –	 0.2 0.3	Vdc
Base – Emitter Saturation Voltage (Note 2) (I_C = 10 mAdc, I_B = 1.0 mAdc) (I_C = 50 mAdc, I_B = 5.0 mAdc)	$V_{BE(sat)}$	 0.65 –	 0.85 0.95	Vdc

Table 2. The DC beta (i.e. h_{FE}) values of 2N3904 BJT.

However, h_{FE} in figure below is the current gain of a BJT that is operating as an amplifier or in the active region. The values that you should be checking are values where the BJT is in the saturation condition.

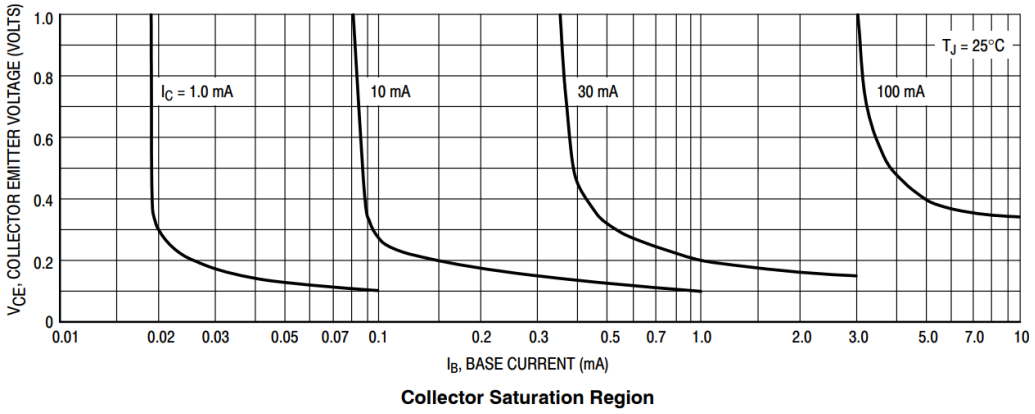


Figure 10. 2N3904 characteristics at saturation region.

In figure below, you can see the different values and information about the 2N3904 operating at saturation region. These are all from the datasheet. Based on this information, you will see that the β_{DC} used in the saturation region for the 2N3904 is 10. Notice that the I_C/I_B ratio is always 10?

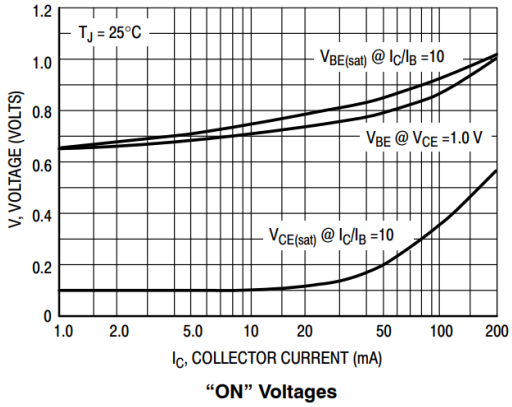


Figure 11. 2N3904 characteristics at saturation region.

Not all BJTs use 10 for β_{DC} though so far, most of the transistors I have used use 10. Darlington BJTs like TIP120 have a 250 I_C/I_B ratio. But, for 2N3904, the guaranteed value of β_{DC} is 10 for it to operate in the saturation region.

Some may use 20 but as we have discussed in the Different Regions of BJT Operation topic, β_{DC} is not constant and it changes with the junction temperature. So, it is better to set β_{DC} at 10.

6. Load Line of BJT Switching

A switch consists of a BJT transistor that is alternately driven between the saturation and cut-off regions. A simple version of the switch is shown in the figure below.

When the input equals $-V_{in}$, the base-emitter junction is reverse biased or off so no current flows in the collector. This is illustrated by the load line shown in the figure.

When the BJT is in cut-off, the circuit (ideally) has the following values:

$$V_{CE} = V_{CC} \text{ and } I_C = 0 \text{ A}$$

This state is like an open switch.

When the input equals $+V_{in}$, the transistor is driven into saturation and the following conditions occur:

$$V_{CE} \tilde{} \, 0 \text{ V and } I_{C(\text{sat})} = V_{CC}/R_C$$

This state is like a closed switch connecting the bottom of R_C to ground.

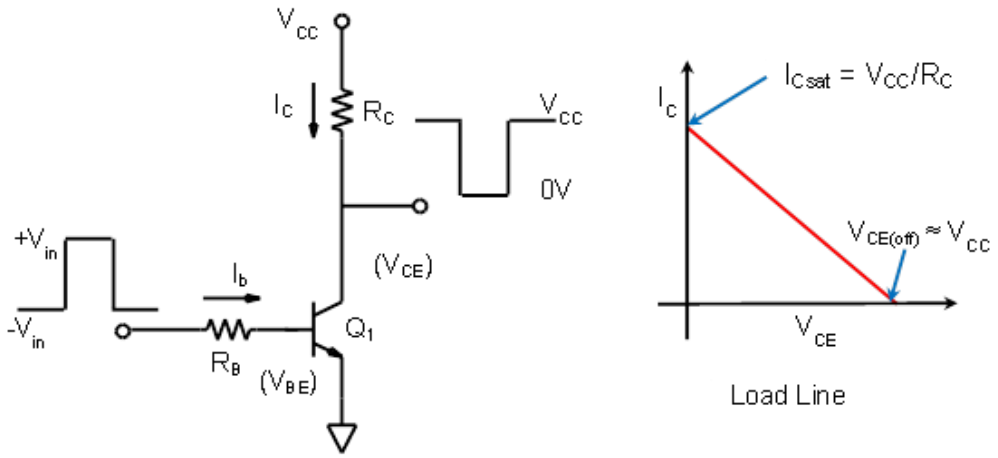


Figure 12: NPN BJT switch application circuit and its load line.

The characteristics for a BJT switch assume that:

- The V_{in} is low enough to drive the transistor into cut-off.
- The $+V_{in}$ must produce enough base current through RB to drive the transistor into saturation.
- The transistor is an ideal component.

These conditions can be assured by designing the circuit so that:

1. The input voltage, $V_{in} = V_{BE}$.
2. The voltages at the input: $+V_{in} = V_{BE} + I_B R_B$ (V_{CC} is a good maximum).
3. The currents, $I_B > I_{C(\text{sat})}/\beta$.

Condition 1 guarantees that the circuit is driven into the cut-off region by the input. Conditions 2 and 3 assure that the transistor will be driven into the saturation region.

An actual BJT switch differs from the ideal switch in several aspects. In practice, even in cut-off there is some leakage current through the transistor.

Also, in saturation, there is always some voltage dropped across the transistor's internal resistance. Typically, this will be between 0.2 and 0.4 V in saturation depending on the collector current and size of the device.

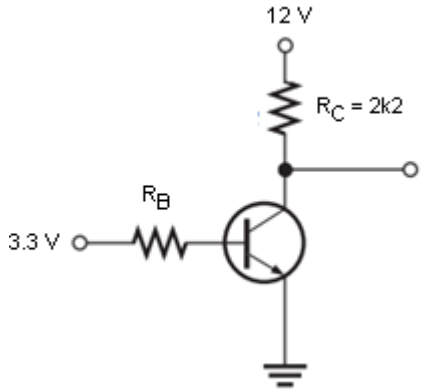
These variations from the ideal are generally minor with a properly sized device, so we can assume near ideal conditions when analysing or designing a BJT switch circuit.

Example 1 – BJT Switching Biasing

For the BJT switching circuit as shown in the figure given below, answer the following questions.

a. What minimum value of I_B is required to saturate this transistor if β_{DC} is 150? Neglect $V_{CE(sat)}$. [4 marks]

b. Describe briefly the significant of this current. Explain what happens when you further increase this current. [2 marks]



Answer

a. Since $V_{CE(\text{sat})}$ is neglected (assumed to be 0 V), the saturation current at the collector is found from:

$$I_{C(\text{sat})} = \frac{V_{CC}}{R_C} = \frac{12\text{ V}}{2.2\text{ k}\Omega} = 5.45\text{ mA}$$

As a result, the minimum current at the base of transistor is:

$$I_{B(\text{min})} = \frac{I_{C(\text{sat})}}{\beta_{DC}} = \frac{5.45\text{ mA}}{150} = 36.3\text{ }\mu\text{A}$$

This is the value of I_B necessary to drive the transistor to the point of saturation.

b. Any further increase in I_B will ensure the transistor remains in saturation, but there cannot be any further increase in I_C.

7. Design with Common Emitter Configuration

Designing a BJT transistor circuit is a complex process that require you to consider the design requirements with a few operating parameters in the circuit and stated preferable conditions of operation.

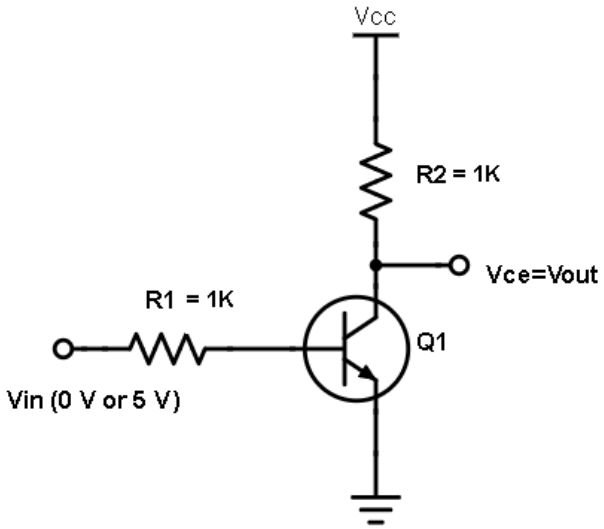


Figure 13: A common emitter BJT transistor circuit.

In above given circuit, considering a common emitter configuration, perform the following heuristic steps for designing a BJT transistor circuit:

Step 1. Assume initially $V_{in} \sim 0$ V (OFF).

So that V_{BE} < 0.7 V, thus the transistor OFF with $I_B = I_C = 0$ A. If $I_B = 0$ A, then there is no voltage drop over the resistor at the collector R_2 and $V_{CE} = V_{out} \sim V_{CC}$ (the transistor is an open circuit as it is OFF). This is *cut-off*.

Step 2. Now increase V_{in} to produce V_{BE} ~ 0.7 V.

As I_B increases, I_C will rapidly increase as $I_C = \beta I_B$ in *active region.* The current I_C will eventually be limited by the value of the resistor at the collector R_2.

Step 3. Keep on increasing I_C.

As I_C increases, the voltage drop over resistor at the collector R_2 will increase. Thus, the voltage drop V_{CE} will decrease and will eventually decrease to *saturation level* ($V_{CE} \sim$ 0.2 V) as the BC junction becomes forward biased.

Step 4. For switch operation, we want to use a binary signal level on V_{in}:

- V_{in} = LO must put transistor in cut-off.
- V_{in} = HI must put transistor in saturation => I_C is a maximum.

Step 5. Typical plot of V_{in} vs I_C.

As shown in the diagram below, when the transistor is turned on at around 600 mV of the input voltage, the collector current starts to flow.

In this case, it is also shown that there is a limit on the collector current is set by the value of the resistor at the collector, R_2 in the circuit. Notice that the region between the turn on and the maximum point is called active region.

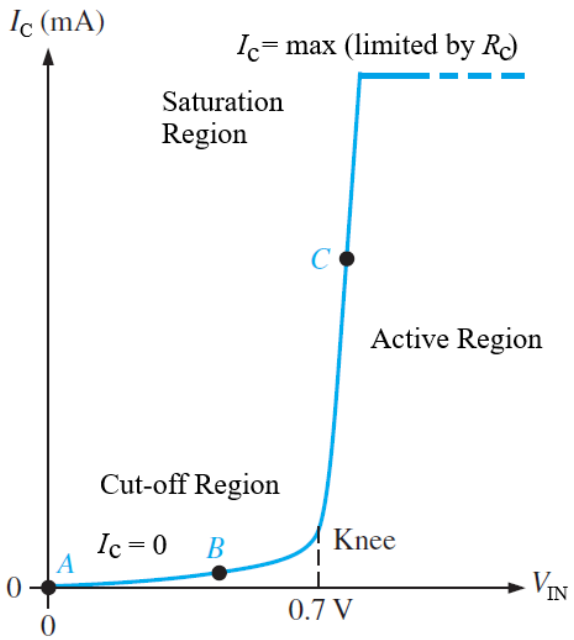


Figure 14: Graph of current I_C vs. voltage V_{in} of BJT.

The diagram given below shows a graph of V_{in} against V_{CE}. Notice that when the BJT transistor is off, V_{CE} is found to be equal to V_{CC} and when the transistor is on it is held to a value of 0.2 V.

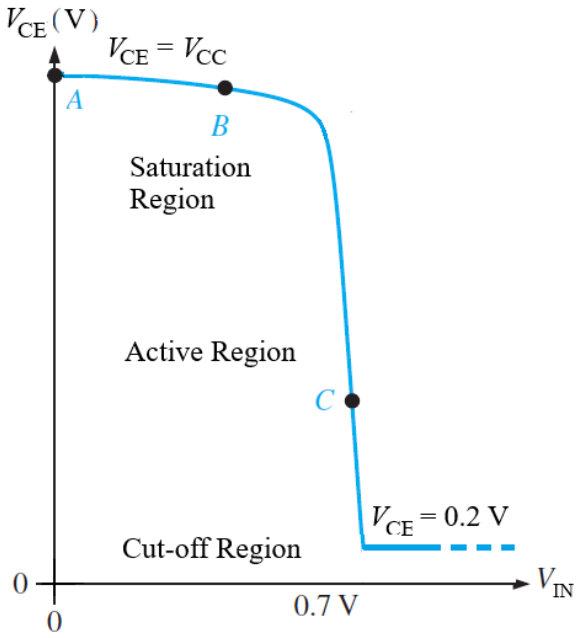


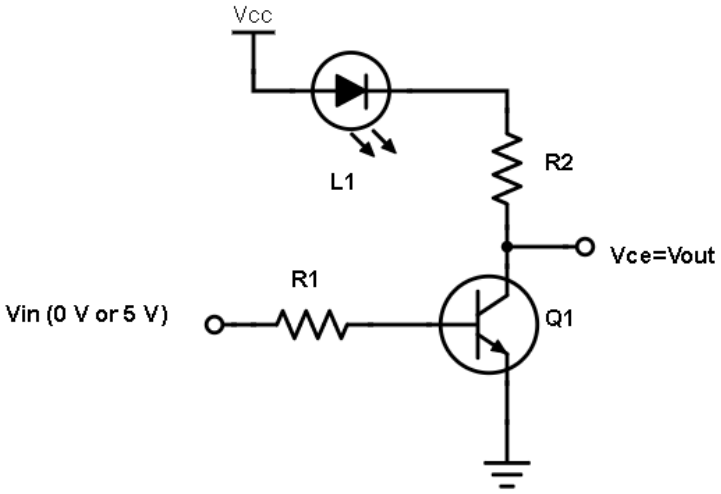
Figure 15: Graph of voltage V_{CE} vs. voltage V_{in} in BJT transistor.

From the plot given before, notice the *inverter* behaviour of this circuit i.e. the output voltage is the inverse voltage of the input.

Example 2 – BJT Switching Circuit

The circuit below must be used to switch on a LED when a 5 V logic signal is used as the input voltage on the base of the transistor.

Calculate sensible values for resistor at the base, R_1 and resistor at the collector, R_2 to ensure that the transistor operates effectively as a switch. [6 marks]



- The circuit is to be supplied with a V_{CC} = 12 V and saturation level voltage across the collector-emitter junction, V_{CE} = 0.2 V.
- The LED needs 20 mA for operation with optimum brightness and has a voltage drop of V_D = 1.8 V over it when forward biased.
- You will be using a microcontroller to provide the input signal (V_{in}) and the output of the microcontroller can provide a maximum current of 8 mA.

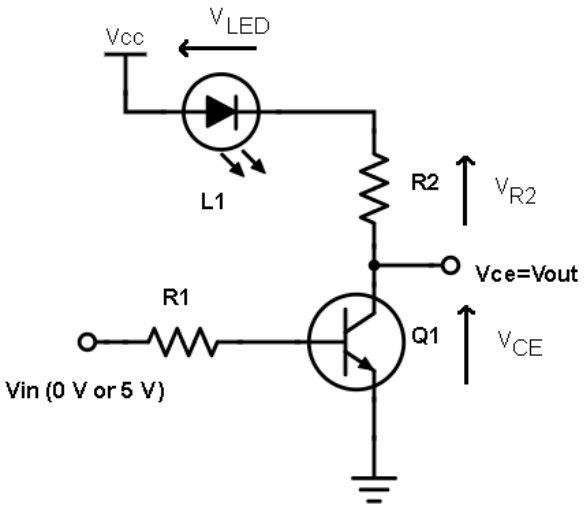
Answer

For the CE loop, we can write a KVL for the saturation case:

$$V_{CC} - I_C R_C - V_D - V_{CE} = 0$$

Entering known values of the circuit parameters into the equation above:

$$12\ \text{V} - (20\ \text{mA})R_2 - 1.8\ \text{V} - 0.2\ \text{V} = 0$$



We need to solve for R_2 to find R_2 = 500 Ω (Do we get a 500 Ω resistor?).

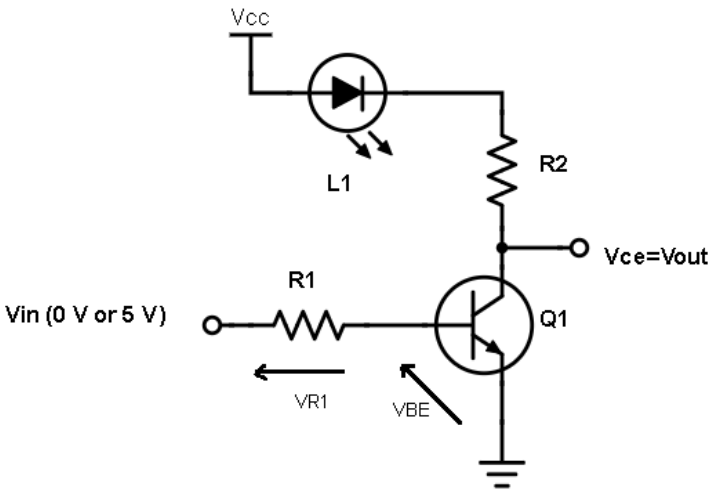
Now, we need to find the base current I_B that will be sufficient to generate this collector current, we have: $I_C = \beta I_B$ with β typically 100 to 500 in the active region.

But we are operating in the saturation region where β is considerably lower, thus take β = 50. We would then need a base current of:

$$I_B = \frac{I_C}{\beta} = \frac{20\ \text{mA}}{50} = 0.4\ \text{mA}$$

The previously calculated value of I_B = 0.4 mA represents the minimum value of base current that would be able to drive the transistor into saturation.

However, when we use a transistor in a switch configuration, we would typically overdrive the transistor to ensure that we are in saturation, i.e. a typical overdrive factor of 10 x can be used. The base current to aim for would thus be I_B = 4 mA.



We can now solve for the resistor at the base, R_1 by looking at the BE current loop:

$$5\ \text{V} - (4\ \text{mA})(R_1) - 0.7\ \text{V} = 0$$

Thus, the resistor at the base of the current, $R_1 \approx 1.1\ \text{k}\Omega$.

This will ensure cut-off or saturation behaviour and I_B will be within the output capability of the microcontroller.

8. BJT Switching Application for Logic Devices

In this section, we will be looking at the use of the BJT to design and construct logic gates. For logic gate design, like BJT switching applications, we consider that there are two states of operation:

- Saturation, or
- Off.

The voltages and resistors are analysed and determined, so the above conditions hold. In short, the transistor now behaves as a switch.

8.1. Logic Gates using BJT

Consider a (NOT) logic gate circuit realised with BJT (note: V_{CC} = 10 V, R_B = 1 kΩ, R_C = 1 kΩ, and V_{BE} = 0.7 V) as shown in the figure below. Notice that V_i is the input voltage and V_o is the output voltage in the circuit. The circuit is connected to V_{CC} = 10 V.

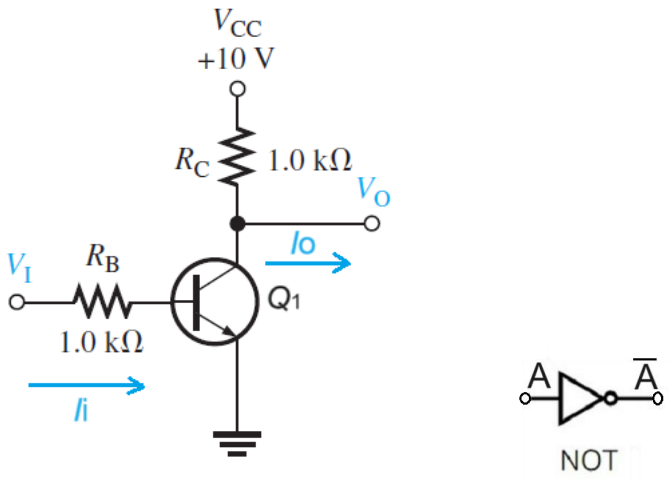


Figure 16: Example 1 of (NOT) logic gate circuit with BJT.

Let the input and output voltages of the circuit correspond to the logic gates listed in the table below.

V_i or V_o (Volt)	Logic Gate
10	1
0	0

Table 3: Input and output voltage and logic gates of example 1 circuit.

Thus, the conditions and states of example 1 logic gate circuit are as shown in the table below.

V_i (Volt)	V_i State	Q_1 State	V_o (Volt)	V_o State
0	0	OFF	10	1
10	1	SAT	0.2	0

Table 4: Conditions and states of example 1 circuit.

The circuit performs the NOT logic function, so it is essentially a NOT logic gate.

To analyse the circuit further, we calculate the current at the input that is:

$$I_B = \frac{V_i - V_{BE}}{R_i} = \frac{10\text{ V} - 0.7\text{ V}}{1\text{ k}\Omega} = 9.3\text{ mA}$$

If we assume the currents in the transistor are related through:

$$I_C = \beta I_i = (100)(9.3\text{ mA}) = 930\text{ mA}$$

Thus

$$V_o = V_{CC} - I_C R_C = 10 - (930\text{ mA})(1\text{ k}\Omega) = -920\text{ V (saturated)}$$

The current that flows at the output is:

$$I_C = \frac{V_{CC} - V_{CE(\text{sat})}}{R_C} = \frac{10\text{ V} - 0.2\text{ V}}{1\text{ k}\Omega} = 9.8\text{ mA}$$

8.2. Design of BJT as Logic Gates

We will be looking further to three more examples of logic gate circuit using BJT in this section.

8.2.1. Example 2: NOT-NOT Logic Gate

Consider the following circuit ($V_{BE(\text{on})} = 0.7\ V; V_{CE(\text{sat})} = 0.2\ V; \beta = 100$) as a second example of a logic gate circuit using BJT.

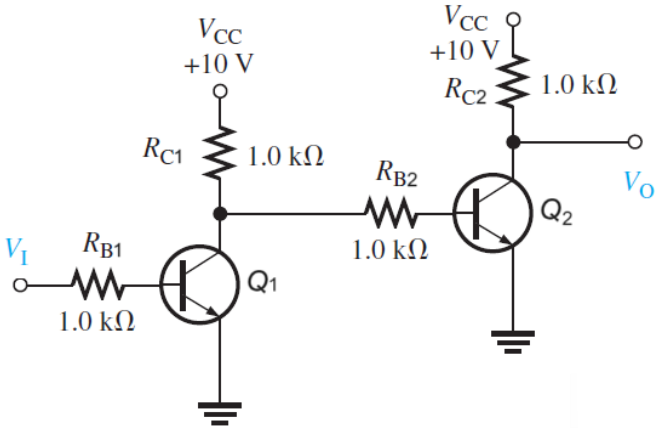


Figure 17: Example 2 of a logic gate circuit with BJT.

The conditions and states of the NOT-NOT logic gate circuit are listed in the table given below.

V_i (Volt)	Q_1 State	V_{C1} (Volt)	Q_2 State	V_{C2}=V_o (Volt)
0	OFF	10	SAT	0.2
10	SAT	0.2	OFF	10

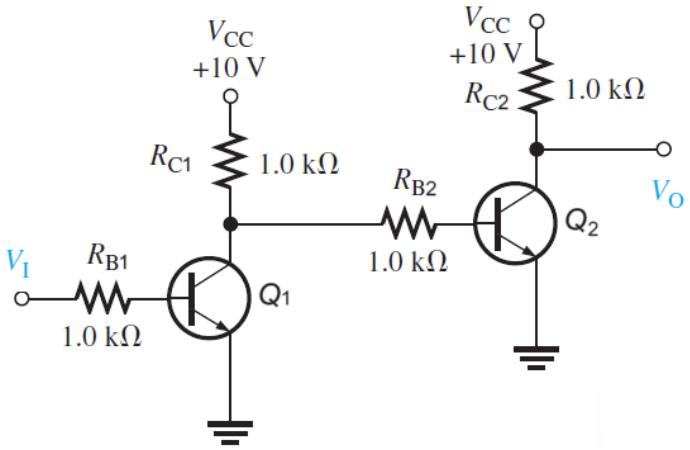
Table 5: Circuit conditions and states of NOT-NOT logic gate.

Assuming high: 8 - 10 V and low: 0 - 1 V, thus the logic states of this logic gate circuit are as shown in the table below.

Logic Input	Logic Output
0	0
1	1

Table 6: Logic states of NOT-NOT logic gate.

The overall operation of the NOT-NOT logic gate circuit is as shown in the figure below.



NOT gate NOT gate

Figure 18: Two NOT gates in the example 2 circuit.

Thus, the logic gates being involved in the operation of the circuit above are outlined as shown in the figure below.

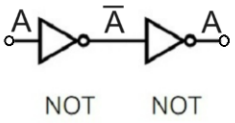


Figure 19: Two NOT gates arranged in series.

8.2.2. Example 3: OR Logic Gate

Consider the circuit given below ($V_{BE(\text{on})} = 0.7\ \text{V};\ \beta = 100$) for the third example of a logic gate circuit using BJT. It is a logic gate with 2 inputs and 2 outputs.

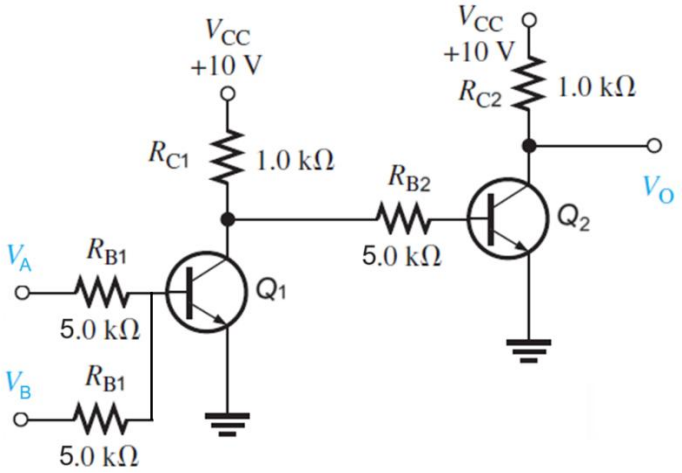


Figure 20: Example 3 of OR logic gate circuit with BJT.

The conditions and states of the OR logic gate circuit are listed in the table below:

V_A (Volt)	V_B (Volt)	Q_1 State	Q_2 State	V_o (Volt)
0	0	OFF	SAT	0.2
0	10	SAT	OFF	10
10	0	SAT	OFF	10
10	10	SAT	OFF	10

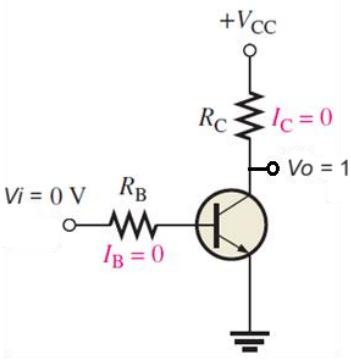
Table 7: Conditions and states of OR logic gate.

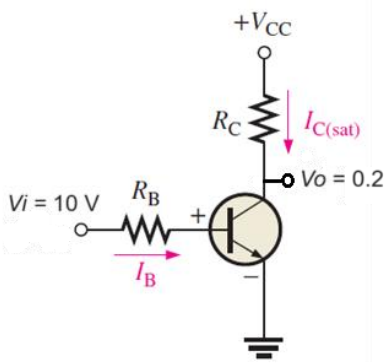
The logic states of the OR logic gate circuit are as shown in the table below.

A	***B***	***Z***
0	0	0
0	1	1
1	0	1
1	1	1

Table 8: Logic states of OR logic gate.

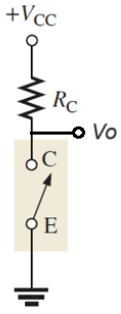
Considering the logic states given in the table above, this is a signature of the operation of an OR logic gate. In summary, when we realise the transistor as a switch, knowing V_{CC} = 10 V and $V_{CE(\text{sat})}$ = 0.2 V, their switching operation are as shown in the figure below.

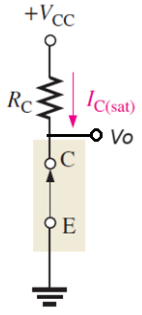




$V_i = 0 \rightarrow Q_1$ (OFF)

$V_i = 10\text{ V} \rightarrow Q_1$ (SAT; ON)





$V_o = V_{CC}$

$V_o = 0.2\text{ V} \cong 0\text{ V}$

Figure 21: Circuit and switching operation of OR logic gate.

8.2.3. Example 4: NAND Logic Gate

For the fourth example of a logic gate circuit with BJT, consider two transistors in series as shown in the figure below (knowing V_{CC} = 10 V and $V_{CE(\text{sat})}$ = 0.2 V).

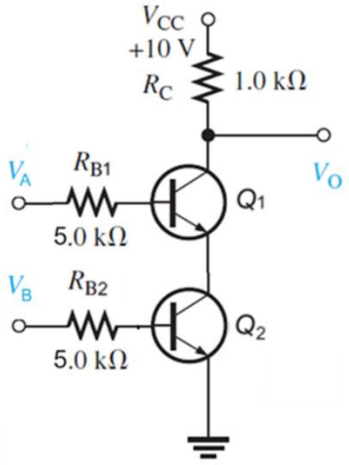
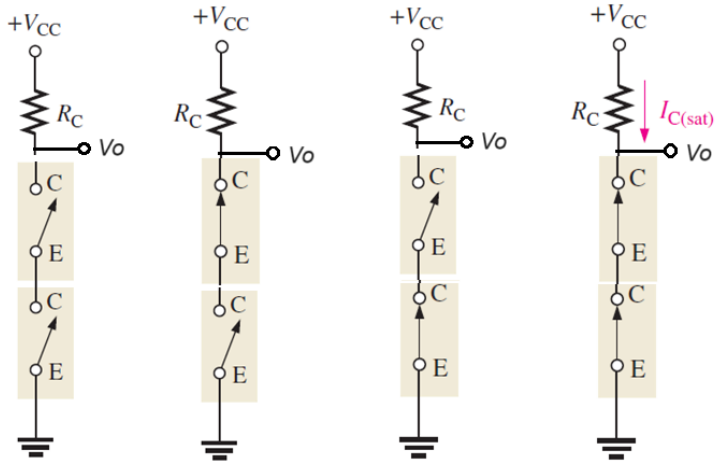


Figure 22: Example 4 of NAND logic gate circuit with BJT.

The switching operation of this example 4 logic gate circuit is as shown in the figure below. It seems that the circuit behaves like a NAND gate.



V_A (Volt)	V_B (Volt)	Q_1 State	Q_2 State	V_o (Volt)
0	0	OFF	OFF	10
10	0	SAT	OFF	10
0	10	OFF	SAT	10
10	10	SAT	SAT	0

A	B	Z
0	0	1
0	1	1
1	0	1
1	1	0

Figure 23: Circuit, switching operation, and logic state of NAND logic gate.

9. Logic Device Families

With just a few diodes, transistors, and passive components, we could construct and realise several logic device circuits. According to their history, we recognise the following logic device families:

- Diode Logic (DL).
- Resistor-Transistor Logic (RTL).
- Diode-Transistor Logic (DTL).
- Transistor-Transistor Logic (TTL).
- Emitter-Coupled Logic (ECL).
- (Complementary) FET:
  - Complementary Metal Oxide Semiconductor (CMOS).
  - BiCMOS.

9.1. Diode Logic (DL)

The digital logic (DL) is the simplest form of logic and inherently it does not scale. With this scheme, the NOT logic is not possible (i.e. it needs an active element). An example of AND logic circuit using diode circuit is as shown below.

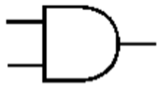


Figure 24: AND Logic gate

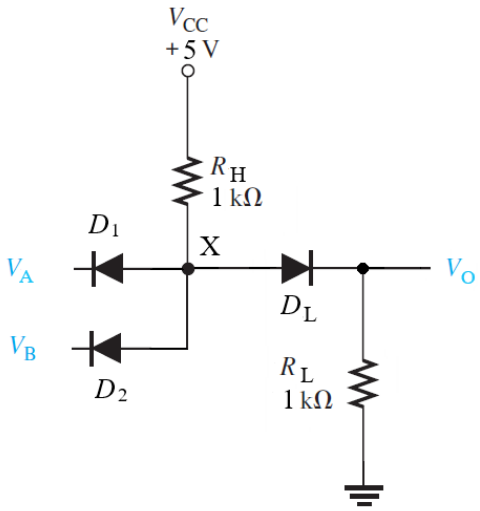


Figure 25: An AND gate realised as a diode logic (DL) circuit.

9.2. Resistor-Transistor Logic (RTL)

The resistor-transistor logic (RTL) replaced the diode switch with a transistor switch. These arrangements could be cascaded and tend to draw large power. The following figure shows an example of RTL's NAND logic circuit.

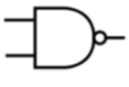


Figure 26: NAND logic gate

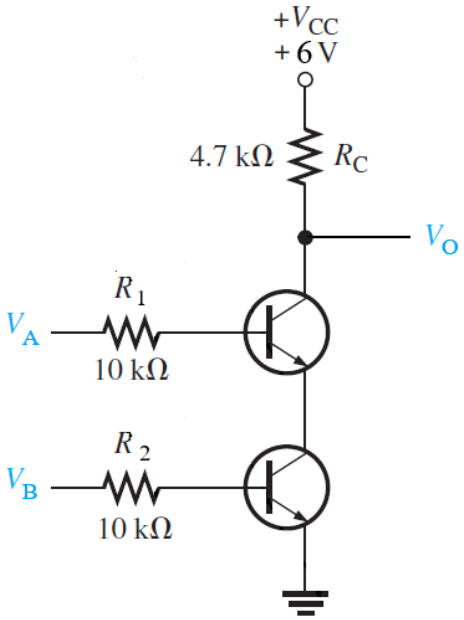


Figure 27: A NAND gate realised as a resistor-transistor logic (RTL) circuit.

9.3. Diode-Transistor Logic (DTL)

Essentially diode-transistor logic (DTL) is a diode logic with transistor amplification. It has reduced power consumption and is faster than the RTL. An example of its NAND logic circuit is shown below.

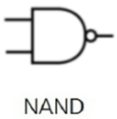


Figure 28: NAND logic gate

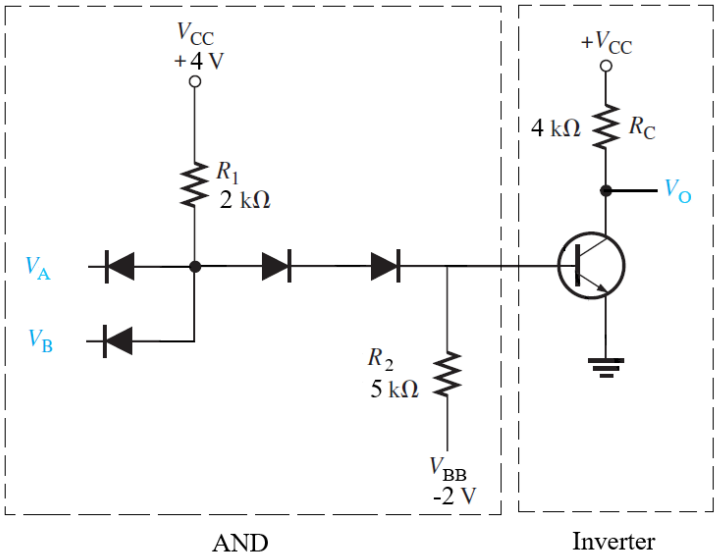


Figure 29: NAND gate realised as a diode-transistor logic (DTL) circuit.

9.4. Transistor-Transistor Logic (TTL)

First, the transistor-transistor logic (TTL) is introduced by Texas Instruments in 1964. It has shaped digital technology in many ways. Now, standard TTL family (e.g. 7400) is obsolete, but newer TTL families are still used (e.g. 74ALS00). Distinct features of TTL are:

- Multi-emitter transistors.
- Totem-pole transistor arrangement.

The following diagrams show two examples of TTL NOT and NOR logic circuits.

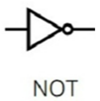


Figure 30: NOT logic gate

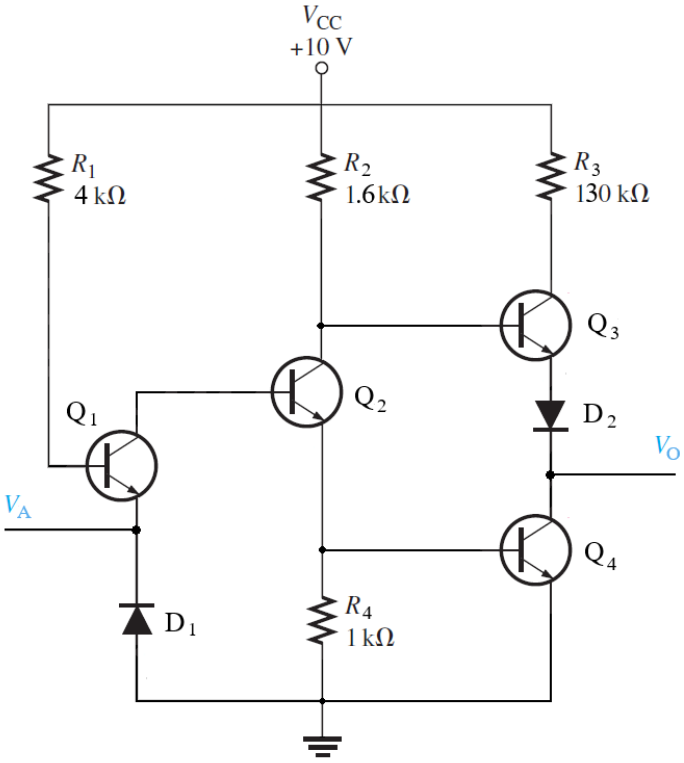


Figure 21: NOT gate realised as a transistor-transistor logic (TTL) circuit.

As shown below, notice that the NOR logic gate is designed around an OR gate and an inverter.

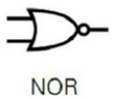


Figure 32: NOR logic gate

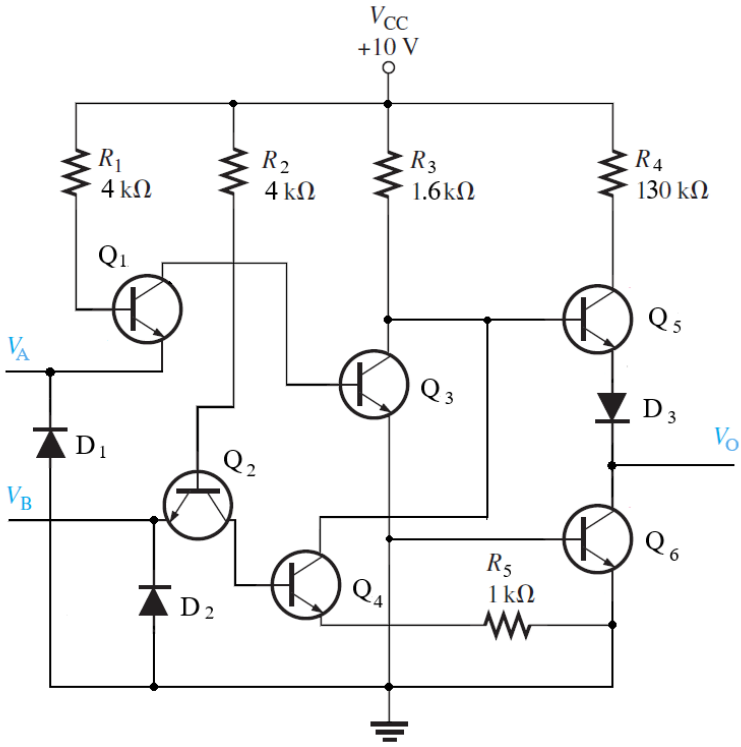


Figure 33: NOR gate realised as a transistor-transistor logic (TTL) circuit.

9.5. Emitter-Coupled Logic (ECL)

ECL is the fastest logic family available (~ 1 ns) (i.e. pros). It is low noise margin and high-power dissipation (i.e. cons) and operated in emitter coupled geometry (i.e. emitter-follower).

In this technology, transistors are biased and operate near their Q-point (i.e. never near saturation). For its logic levels, these are: “0”: –1.7 V. “1”: –0.8 V.

As a result, for such uncommon logic levels, we require extra effort when interfacing these circuits to the TTL/CMOS logic families.

For the logic gate circuit technology with the emitter coupled logic circuit (ECL), we use a NOR logic circuit example as shown in the figure below.

NOR

Figure 34: NOR logic gate with two outputs

The BJT circuit implementation of the NOR logic gate above with ECL technology is as shown in the figure below.

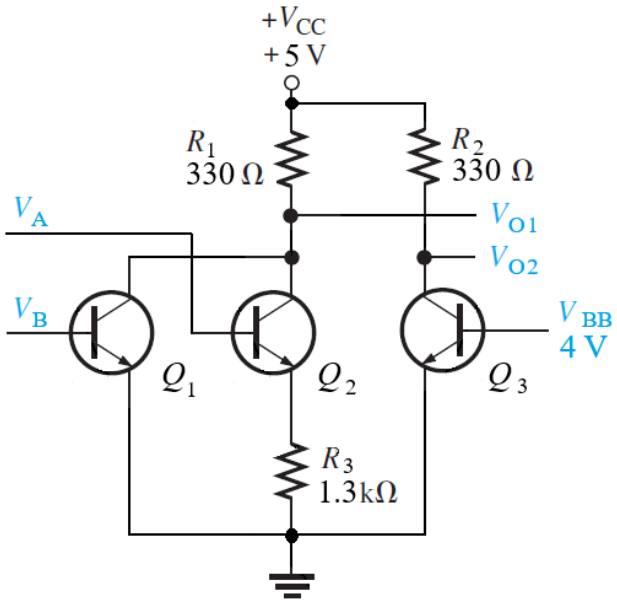


Figure 35: NOR gate realised as an emitter-couple logic (ECL) circuit.

The following table outlines the logic states of NOR logic gate with ECL technology.

X	***Y***	***OUT1***	***OUT2***
0	0	1	0
0	1	0	1
1	0	0	1
1	1	0	1

Table 9: Logic states of NOR logic gate with ECL.

In summary, there are many differences and similarities between the technologies of logic gate using BJT as compared in the table given below.

Specification	**TTL**	**ECL**	**CMOS**
Components	Transistor and passive elements	Transistor and passive elements	MOSFETs
Basic Gate	NAND	OR/NOR	NAND/NOR
Noise Immunity	Strong	Good	Very Strong
Fan-out	10	25	More than 50
t_{PD} (in ns)	1.5 - 30	1 - 4	1 - 210
Noise Margin	Moderate	Low	High
Power/Gate (in mW)	10	40 - 55	0.0025
Clock Rate (in MHz)	35	> 60	10
Figure of Merit	100	40-100	0.7

Table 10: Comparison of technologies/family of logic-gate circuits using BJT.

Note:

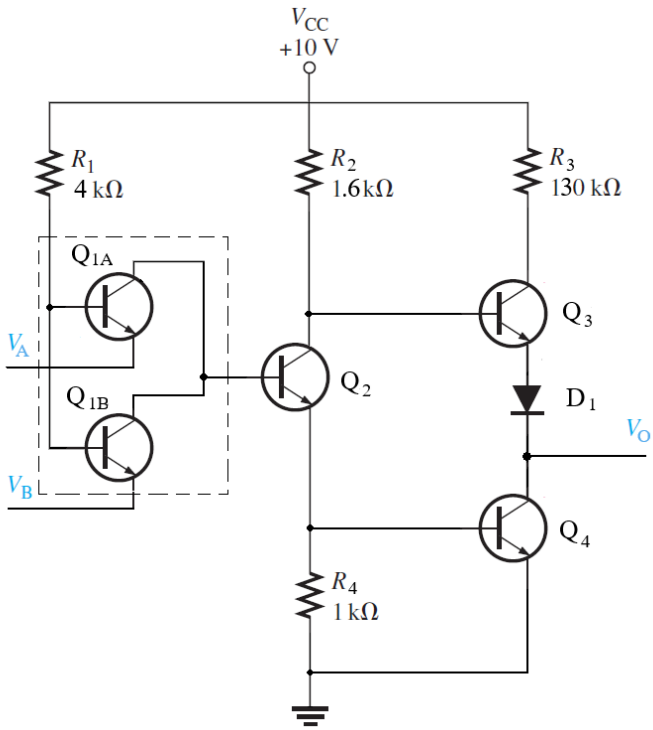
t_{PD} = propagation delay (how long a signal pass through the circuit).

Figure of merit = combination of figures for propagation delay and power dissipation.

The following example shows the operation of a NAND logic gate with TTL technology that illustrate its design and construction.

Example 3 – TTL Based Logic Device

Describe the mechanism of the following TTL NAND logic device as shown in the figure below.



Answer

Transistor Q_3 is cutoff (i.e. act like a high RC) when the output transistor Q_4 is saturated, and Q_3 is saturated (i.e. act like a low RC) when the output transistor Q_4 is cutoff.

Thus, in the given circuit, one transistor is ON at one time. The combination of Q_3 and Q_4 is called TOTEM POLE arrangement. Transistor Q_1 is called input transistor, which is multi emitter transistor, that drive transistor Q_2 which is used to control Q_3 and Q_4. On the other hand, diode D_1 ensures when Q_4 is ON and Q_3 is OFF.

(In some designs) two additional diodes connected to V_A and V_B pins are used to protect Q_1 from unwanted negative voltages.

The conditions and states of the circuit are listed in the table below:

V_A (Volt)	V_B (Volt)	Q_{1A} State	Q_{1B} State	Q_2 State	Q_3 State	Q_4 State	V_O (Volt)
0	0	OFF	OFF	SAT	SAT	SAT	10
10	0	SAT	OFF	SAT	SAT	SAT	10

0	10	OFF	SAT	SAT	SAT	SAT	10
10	10	SAT	SAT	OFF	SAT	OFF	0

The logic function of the logic gate is shown in the table below. This is the operation of a NAND logic gate.

A	***B***	***Z***
0	0	1
0	1	1
1	0	1
1	1	0