1. Common Collector Amplifier

In this chapter, we will cover various other circuits of BJT amplifiers. The first circuit is a common collector (emitter follower) amplifier. This amplifier circuit has two changes from the amplifier with CE with feedback that we discussed previously.

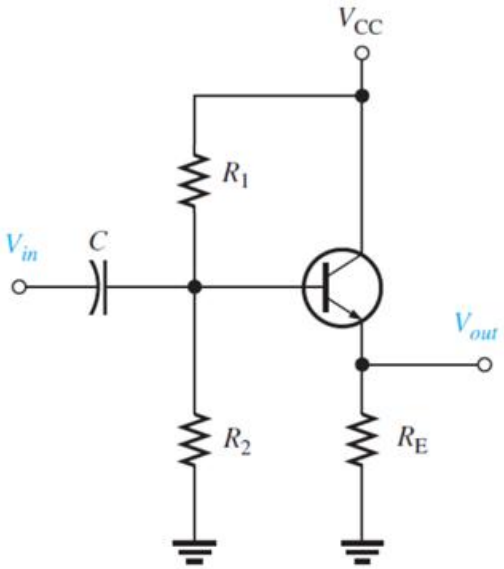


Figure 1: A common collector BJT amplifier circuit

First, the output is now taken at the emitter and second, the collector resistor has been removed.

As a result, the collector connected to positive supply which is at ground for AC signals as there are no AC signals between supply and ground.

As the collector is at ground potential for small signals, it is common to both input and output circuits i.e. hence called a common collector amplifier.

If we use a small signal model, we can again show that the input resistance is:

$$r_{in} \approx R_1 \parallel R_2$$

The output resistance is given by the parallel combination of R_E and the resistance looking back into the emitter (r_e).

$$r_{out} \approx R_E \parallel r_e$$

This value of r_e is typically very low (few ohms) and will thus dominate => amplifier has a very low output impedance.

The small signal voltage gain can be calculated by considering the input signal is applied at the base of the transistor so that:

$$V_i \approx V_b \approx V_e$$

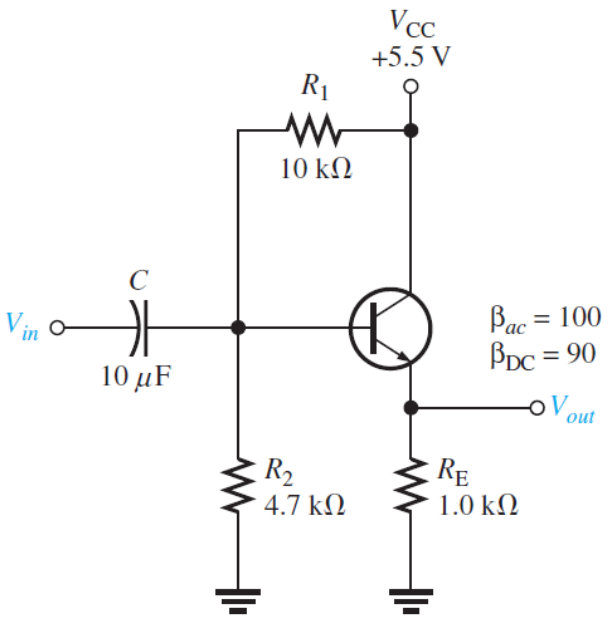
So, that voltage gain is:

$$A_v \approx 1$$

We thus have a unit gain amplifier with low output impedance (emitter follower). This results in **a unity gain buffer.**

Example 1 – Common Collector BJT Amplifier

For the common collector (emitter follower) circuit given below, perform the following tasks:



a. Determine the exact voltage gain for the circuit when it is unloaded. [8 marks]

b. What is the total input resistance in the circuit? What is the DC output voltage? [4 marks]

Answer

a. The amplifier circuit employs a voltage divider biasing configuration, so the voltage at the base is:

$$V_B = \left(\frac{R_2}{R_1 + R_2}\right) V_{CC} = \left(\frac{4.7\ \text{k}\Omega}{10\ \text{k}\Omega + 4.7\ \text{k}\Omega}\right) 5.5\ \text{V} = 1.76\ \text{V}$$

The current that flows in the emitter of the amplifier circuit is:

$$I_E = \frac{V_B - V_{BE}}{R_E} = \frac{1.76\ \text{V} - 0.7\ \text{V}}{1\ \text{k}\Omega} = 1.06\ \text{mA}$$

The AC emitter resistance of the BJT is:

$$r_e' \cong \frac{25\ \text{mV}}{1.06\ \text{mA}} = 23.6\ \Omega$$

The voltage gain of the amplifier circuit is:

$$A_v = \frac{R_E}{R_E + r_e'} = \frac{1\ \text{k}\Omega}{1\ \text{k}\Omega + 23.6\ \Omega} = 0.977$$

b. The total input resistance of the amplifier circuit is:

$$R_{in} = R_1 \parallel R_2 \parallel \beta_{ac}(r_e' + R_E) \cong R_1 \parallel R_2 \parallel \beta_{ac} R_E$$
$$= 10\ \text{k}\Omega \parallel 4.7\ \text{k}\Omega \parallel 100\ \text{k}\Omega = 3.1\ \text{k}\Omega$$

The output voltage of the amplifier circuit is:

$$V_{out} = V_B - V_{BE} = \left(\frac{R_2}{R_1 + R_2}\right) V_{CC} - V_{BE}$$
$$= \left(\frac{4.7\ \text{k}\Omega}{10\ \text{k}\Omega + 4.7\ \text{k}\Omega}\right) 5.5\ \text{V} - 0.7\ \text{V} = 1.06\ \text{V}$$

2. Common Base Amplifier

The base is the common terminal and is at AC ground because of capacitor C_2. The input signal is capacitively coupled to the emitter by C_1. The output is capacitively coupled from the collector to a load resistor by C_3.

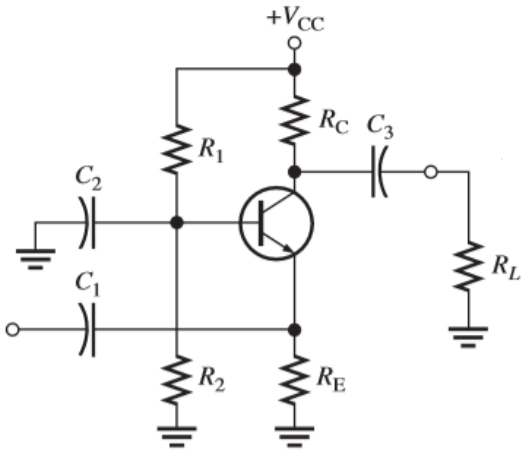


Figure 2: A common base BJT amplifier circuit

The voltage gain from emitter to collector is (if $R_E \gg r_e'$):

$$A_v \approx \frac{R_c}{r_e'}$$

Notice that the gain expression is the same as for the common-emitter amplifier. However, there is no phase inversion from emitter to collector.

The input resistance, looking in at the emitter (if $R_E \gg r_e'$), is

$$R_{in(\text{emitter})} \approx r_e'$$

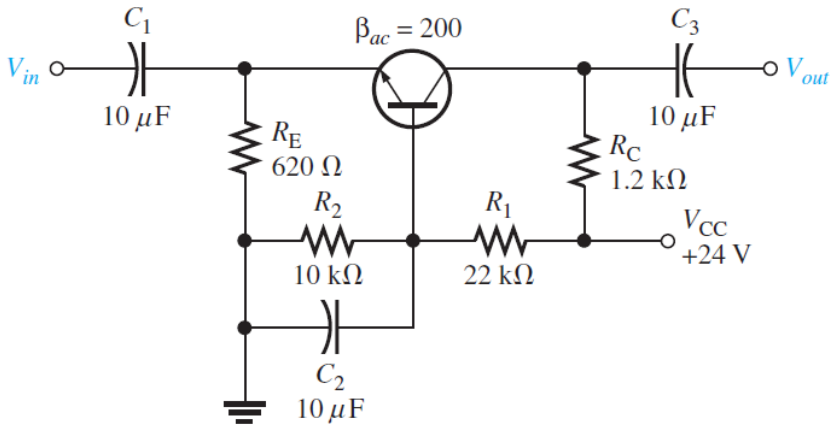
Looking into the collector, the AC collector resistance appears in parallel with R_C. As you have previously seen in connection with the CE amplifier, is typically much larger than R_C, so a good approximation for the output resistance is:

$$R_{out} = R_C$$

Since the current gain is approximately 1 for the common-base amplifier, the power gain is approximately equal to the voltage gain.

Example 2 – Common Base BJT Amplifier

Find $R_{in(\text{emitter})}$, A_v, A_i, and A_p for the unloaded common base BJT amplifier as shown in the figure below. [12 marks]



Answer

The voltage at the emitter is calculated from the following equation.

$$V_E = \left(\frac{R_2}{R_1 + R_2}\right) V_{CC} - V_{BE} = \left(\frac{10\ \text{k}\Omega}{22\ \text{k}\Omega + 10\ \text{k}\Omega}\right) 24\ \text{V} - 0.7\ \text{V} = 6.8\ \text{V}$$

Thus, the current that flows in the emitter is:

$$I_E = \frac{V_E}{R_E} = \frac{6.8\ \text{V}}{620\ \Omega} = 10.97\ \text{mA}$$

Knowing the value of the current in the emitter, the resistance at the emitter is calculated as:

$$R_{in(\text{emitter})} = r'_e = \frac{25\ \text{mV}}{I_E} = \frac{25\ \text{mV}}{10.97\ \text{mA}} = 2.28\ \Omega$$

As a result, the voltage, current, and power gains of the amplifier circuit are:

- Voltage gain:

$$A_v = \frac{R_C}{r'_e} = \frac{1.2\ \text{k}\Omega}{2.28\ \Omega} = 526$$

- Current gain:

$$A_i \cong 1$$

- Power gain:

$$A_p = A_i A_v = (1)(526) = 526$$

3. Cascaded Amplifiers

If more gain is required than can be supplied by a single gains stage, several stages can be connected (cascaded) in series. As shown in the figure below, the total amplification factor of cascaded amplifier is

$$A_{V(\text{tot})} = A_{V1} A_{V2}$$

Where:

A_{V1} = Amplification factor of 1st stage.

A_{V2} = Amplification factor of 2nd stage.

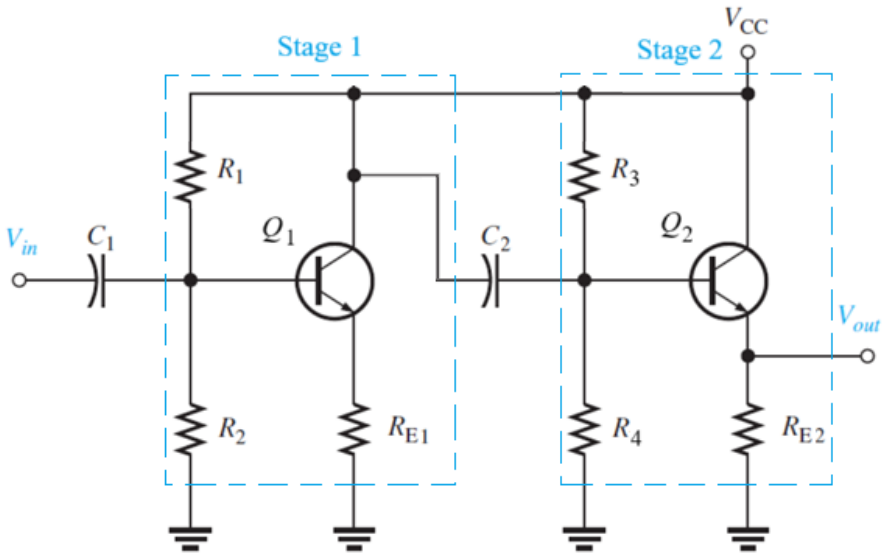


Figure 3: Cascaded amplifier circuit

3.1. Capacitively Coupled Multistage Amplifier

As shown in the figure below, notice that both stages of the cascaded amplifier circuit are identical common-emitter amplifiers with the output of the first stage capacitively coupled to the input of the second stage.

Capacitive coupling prevents the DC bias of one stage from affecting that of the other but allows the AC signal to pass without attenuation because X_C > 0 V at the frequency of operation. Notice, also, that the transistors are labeled Q_1 and Q_2.

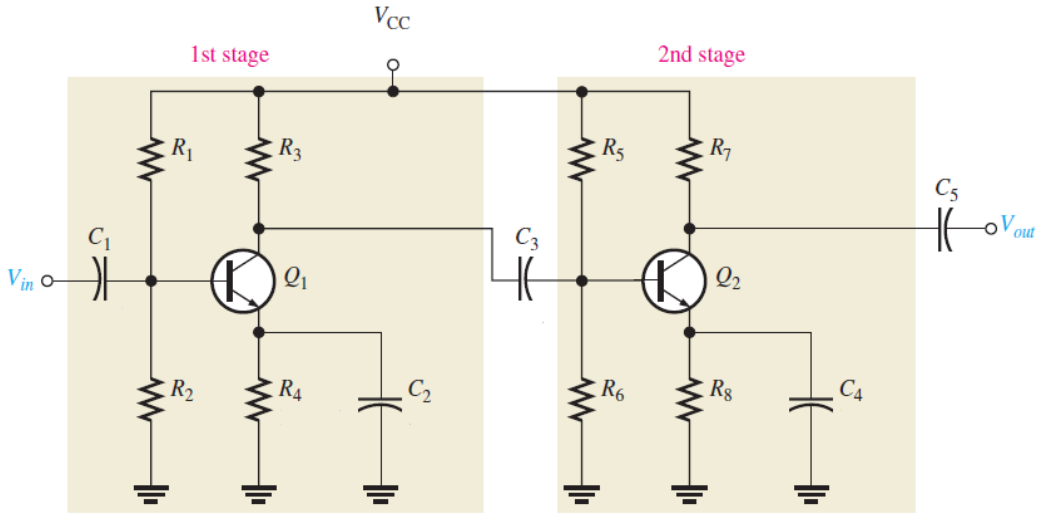


Figure 4: Capacitively coupled multistage amplifier circuit

In determining the voltage gain of the first stage, you must consider the loading effect of the second stage. Because the coupling capacitor C_3 effectively appears as a short at the signal frequency, the total input resistance of the second stage presents an AC load to the first stage.

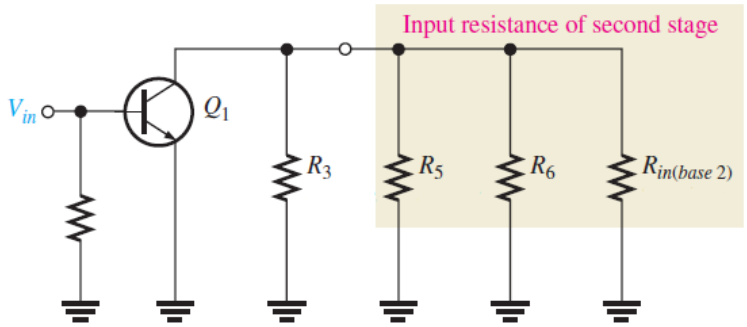


Figure 5: AC equivalent of first stage of capacitively coupled multistage amplifier, showing loading from second stage input resistance.

Looking from the collector of Q_1, the two biasing resistors in the second stage, R_5 and R_6, appear in parallel with the input resistance at the base of Q_2. In other words, the signal at the collector of Q_1 "sees" R_3, R_5, R_6, and $R_{in(\text{base2})}$ of the second stage all in parallel to AC ground. Thus, the effective AC collector resistance of Q_1 is the total of all these resistances in parallel.

The voltage gain of the first stage is reduced by the loading of the second stage because the effective AC collector resistance of the first stage is less than the actual value of its collector resistor, R_3. Remember that $A_v = R_c/r_e'$.

Voltage Gain of the First Stage

The AC collector resistance of the first stage is:

$$R_{C1} = R_3 \parallel R_5 \parallel R_6 \parallel R_{in(\text{base2})}$$

Therefore, the base-to-collector voltage gain of the first stage is

$$A_{v1} = \frac{R_{C1}}{r_e'}$$

Voltage Gain of the Second Stage

The second stage has no load resistor, so the AC collector resistance is R_7, and the gain is:

$$A_{v2} = \frac{R_7}{r_e'}$$

Overall Voltage Gain

The overall amplifier gain with no load on the output is:

$$A_{v(\text{total})} = A_{v1}A_{v2}$$

3.2. Direct Coupled Multistage Amplifier

A basic two-stage, direct-coupled amplifier is shown in the figure below. Notice that there are no coupling or bypass capacitors in this circuit. The DC collector voltage of the first stage provides the base-bias voltage for the second stage.

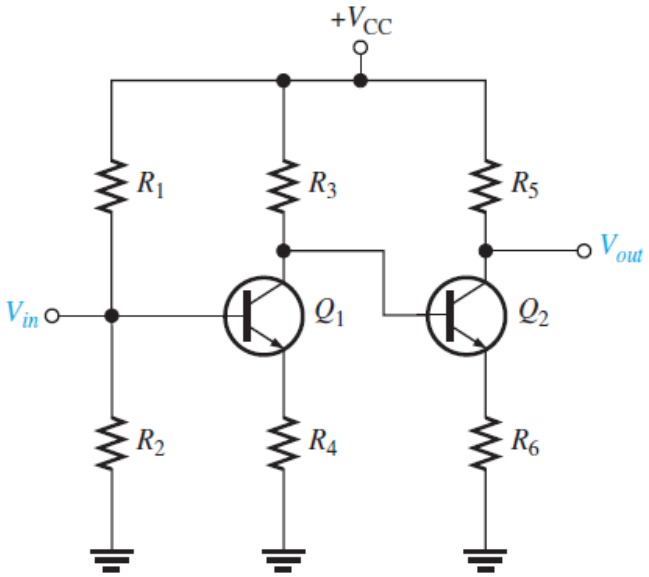


Figure 6: Direct coupled multistage amplifier circuit

Because of the direct coupling, this type of amplifier has a better low-frequency response than the capacitively coupled type in which the reactance of coupling and bypass capacitors at very low frequencies may become excessive. The increased reactance of capacitors at lower frequencies produces gain reduction in capacitively coupled amplifiers.

Direct-coupled amplifiers can be used to amplify low frequencies all the way down to DC (0 Hz) without loss of voltage gain because there is no capacitive reactance in the circuit.

The disadvantage of direct-coupled amplifiers, on the other hand, is that small changes in the DC bias voltages from temperature effects or power-supply variation are amplified by the succeeding stages, which can result in a significant drift in the DC levels throughout the circuit.

4. Darlington Transistors (Pairs)

This is a method to combine two transistors, so that the gain of the first transistor is multiplied by the second transistor, and so that it acts as a single transistor with β equal to the product of the two gains. Note that the voltage offset between base emitter will now be 1.4 V.

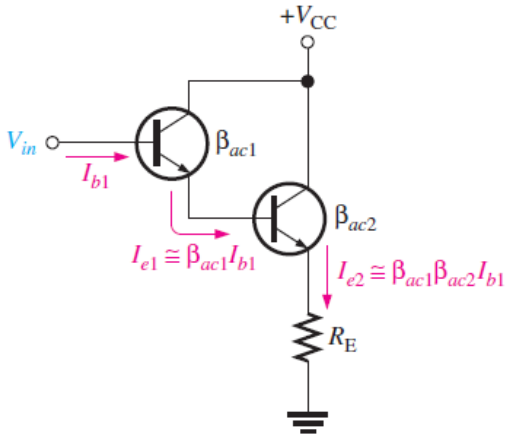


Figure 7: The basic Darlington configuration

This produces a device (single package) with very high gain and high input resistance. This method is commonly used for high gain power transistors.

Example 3 – Multistage BJT Amplifier

For a multistage BJT amplifier circuit with a pair of Darlington transistors given in the figure below, determine the following:

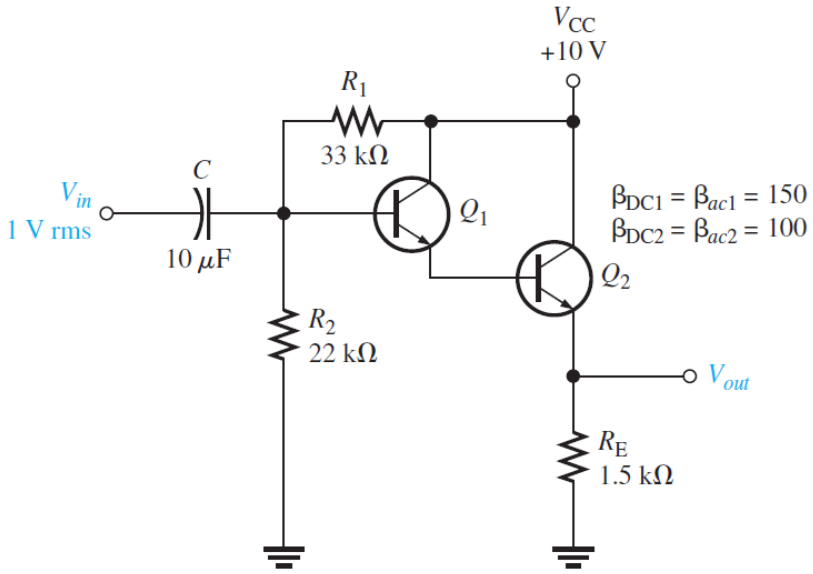
a. The Q_1 and Q_2 DC terminal voltages. [8 marks]

b. The overall β_{ac}. [2 marks]

c. The r_e' for each transistor. [8 marks]

d. Total input resistance. [4 marks]

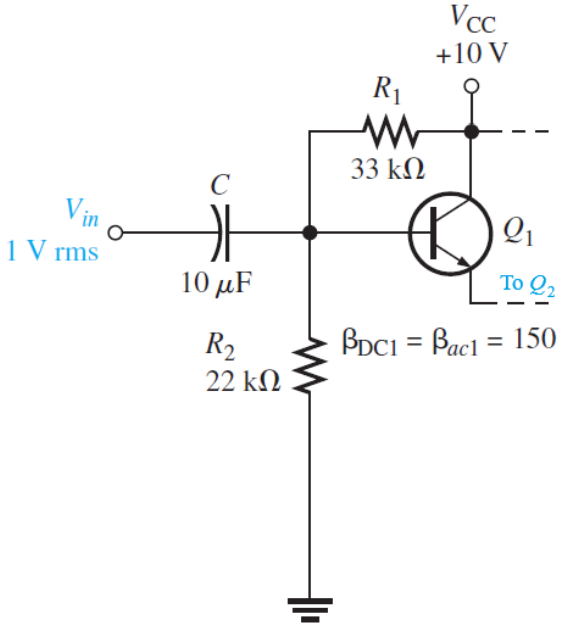
e. Find the overall current gain A_i. [12 marks]



Answer

a. The Q_1 and Q_2 DC terminal voltages of the Darlington pair BJT amplifier circuit are calculated as follows.

The First Transistor Q_1:



For the first transistor, its collector voltage is:

$$V_{c1} = 10\ \text{V}$$

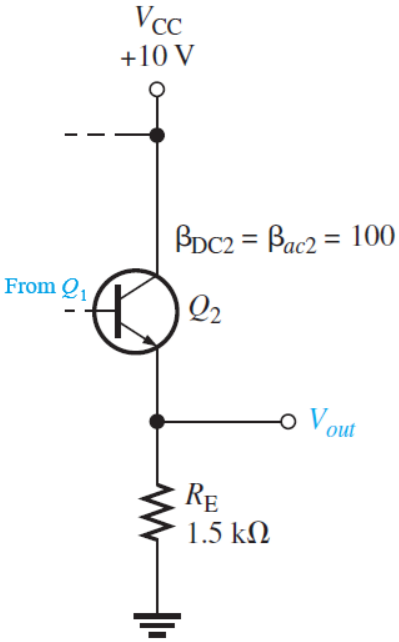
Thus, the base voltage of the first transistor is:

$$V_{B1} = \left(\frac{R_2}{R_1 + R_2}\right) V_{CC} = \left(\frac{22\ \text{k}\Omega}{33\ \text{k}\Omega + 22\ \text{k}\Omega}\right) 10\ \text{V} = 4\ \text{V}$$

As a result, the voltage at the emitter of the first transistor is:

$$V_{E1} = V_{B1} - V_{BE} = 4\ \text{V} - 0.7\ \text{V} = 3.3\ \text{V}$$

The Second Transistor Q_2:



For the second transistor, its collector voltage is:

$$V_{C2} = 10\ \text{V}$$

Thus, the base voltage of the second transistor is:

$$V_{B2} = V_{E1} = 3.3\ \text{V}$$

As a result, the voltage at the emitter of the second transistor is:

$$V_{E2} = V_{B2} - V_{BE} = 3.3\ \text{V} - 0.7\ \text{V} = 2.6\ \text{V}$$

b. The overall AC gain of the Darlington pair BJT amplifier circuit, β_{ac} is calculated as:

$$\beta'_{DC} = \beta_{DC1}\beta_{DC2} = (150)(100) = 15{,}000$$

c. The AC emitter resistance, r'_e for each transistor in the Darlington pair BJT amplifier circuit is calculated as follows.

The First Transistor Q_1:

The current that flows in the emitter of the first transistor is:

$$I_{E1} = \frac{V_{E1} - V_{BE}}{\beta_{DC2}R_E} = \frac{3.3\text{ V} - 0.7\text{ V}}{(100)(1.5\text{k}\Omega)} = 17.3\ \mu\text{A}$$

And

$$r'_{e1} = \frac{25\text{ mV}}{I_{E1}} = \frac{25\text{ mV}}{17.3\ \mu\text{A}} = 1.45\ \text{k}\Omega$$

The Second Transistor Q_2:

The current that flows in the emitter of the second transistor is:

$$I_{E2} = \frac{V_{E2}}{R_E} = \frac{2.6\text{ V}}{1.5\ \text{k}\Omega} = 1.73\ \text{mA}$$

And

$$r'_{e2} = \frac{25\text{ mV}}{I_{E2}} = \frac{25\text{ mV}}{1.73\text{ mA}} = 14.5\ \Omega$$

d. Total input resistance of the Darlington pair BJT amplifier is calculated from the following equation:

$$R_{in} = R_1 \parallel R_2 \parallel R_{in(\text{base1})}$$

As a result, the input resistance at the base is:

$$R_{in(\text{base1})} = \beta_{ac1}\beta_{ac2}R_E = (150)(100)(1.5\ \text{k}\Omega) = 22.5\ \text{M}\Omega$$

Thus, the total input resistance of the amplifier is:

$$R_{in} = 33\ \text{k}\Omega \parallel 22\ \text{k}\Omega \parallel 22.5\ \text{M}\Omega = 13.2\ \text{k}\Omega$$

e. For finding the overall current gain A_i of the Darlington pair BJT amplifier circuit, we need to determine the currents that flow in the input and the output.

The resistance at the base of the amplifier circuit is:

$$R_{in(\text{base})} = \beta_{ac1}\beta_{ac2}R_E = (150)(100)(1.5\ \text{k}\Omega) = 22.5\ \text{M}\Omega$$

The total input resistance of the amplifier circuit is:

$$R_{in} = R_1 \parallel R_2 \parallel R_{in(\text{base})} = 33\ \text{k}\Omega \parallel 22\ \text{k}\Omega \parallel 22.5\ \text{M}\Omega = 13.2\ \text{k}\Omega$$

Thus, the AC current that flows in the input of the amplifier circuit is:

$$I_{in} = \frac{V_{in}}{R_{in}} = \frac{1\ \text{V (rms)}}{13.2\ \text{k}\Omega} = 75.8\ \mu\text{A (rms)}$$

The AC current that flows in the base of the transistor Q_1 is:

$$I_{in(\text{base1})} = \frac{V_{in}}{R_{in(\text{base1})}} = \frac{1\ \text{V (rms)}}{22.5\ \text{M}\Omega} = 44.4\ \text{nA (rms)}$$

The AC current that flows in the emitter (output) of the amplifier circuit is:

$$I_e \cong \beta_{ac1}\beta_{ac2}I_{in(\text{base1})} = (150)(100)(44.4\ \text{nA}) = 667\ \mu\text{A (rms)}$$

As a result, the current gain of the amplifier circuit is:

$$A_i' = \frac{I_e}{I_{in}} = \frac{667\ \mu\text{A}}{75.8\ \mu\text{A}} = 8.8$$

5. Transistor as a Constant Current Source

The constant current through the base will also ensure a constant emitter voltage, which will ensure a constant current through the load e.g. current sink or current source.

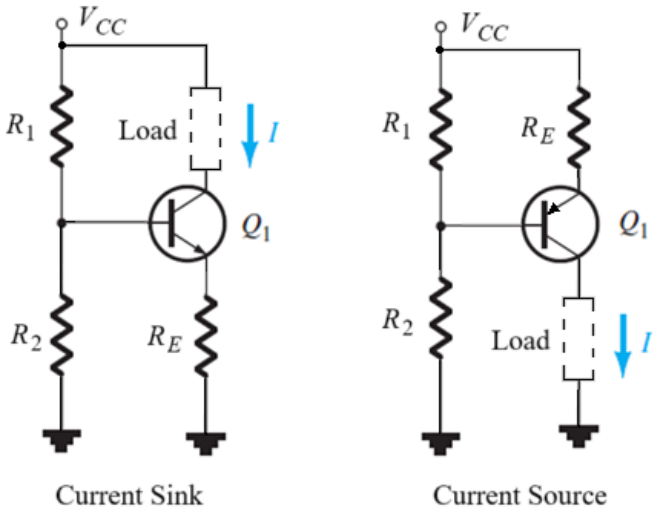


Figure 8: Transistor as constant current source

We can improve circuit by using Zener diode in the place of R_2 to ensure a constant emitter voltage.

6. Current Mirror

A current mirror can be considered as a constant current source in which the current produced is equal to some input current.

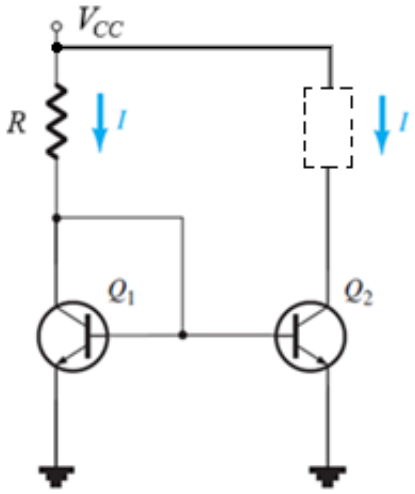
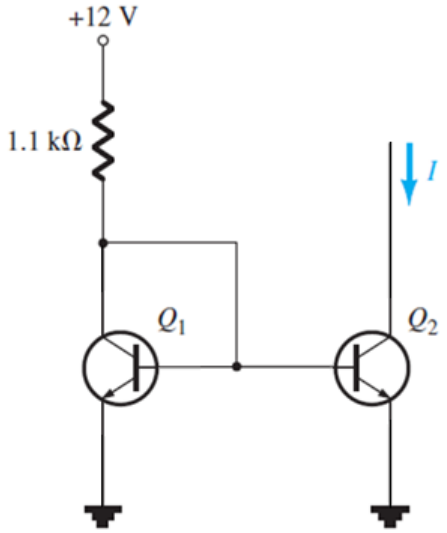


Figure 9: Current mirror circuit

As illustrated in the diagram given above, current mirror can create equal currents in the circuit. If any load is connected to the current mirror circuit as illustrated in the figure below, the amount of the current that flows in the load will be identical in term of its magnitude with the current that flows in the resistor (R). So, depending on the value of this resistor that you placed in the circuit, you could determine the amount of current that flows in the load.

Example 4 – BJT Current Source Circuit

Calculate the mirrored current I in the circuit shown in the figure below. [5 marks]



Answer

For the given current mirror circuit, assuming identical transistors Q_1 and Q_2, the current I in the circuit must be equal to $I_{control}$, so:

$$I = I_{control}$$

Thus

$$I = \frac{V_{CC} - V_{BE}}{R} = \frac{12\ \text{V} - 0.7\ \text{V}}{1.1\ \text{k}\Omega} = 10.27\ \text{mA}$$

7. Differential Amplifier

Differential amplifiers produce an output signal that is proportional to the difference between two input signals while ignoring the signal component that is common to both signals.

The two transistors share the current that flows through the single emitter resistor i.e. with perfectly matched transistors and resistors and equal input voltages the outputs (v_3 and v_4) will be equal (zero differential).

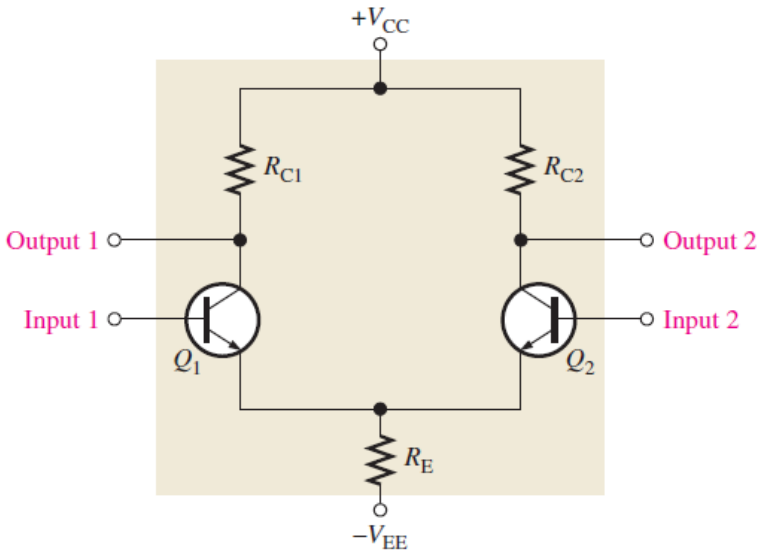


Figure 10: Differential amplifier circuit

If the input voltage on v_1 now rises, the current through R_E will be split unevenly with more of the current going through T_1.

This will lead to a voltage difference between v_3 and v_4. This forms the principle of operation for bipolar operational amplifiers (op amps).

7.1. Single-Ended Differential Input

In the single-ended differential input, one input is grounded and the signal voltage is applied only to the other input.

When the signal voltage is applied to input 1 as illustrated in the figure below, an inverted, amplified signal voltage appears at output 1 as shown. Also, a signal voltage appears in

phase at the emitter of Q_1. Since the emitters of Q_1 and Q_2 are common, the emitter signal becomes an input to Q_2, which functions as a common-base amplifier. The signal is amplified by Q_2 and appears, non-inverted, at output 2.

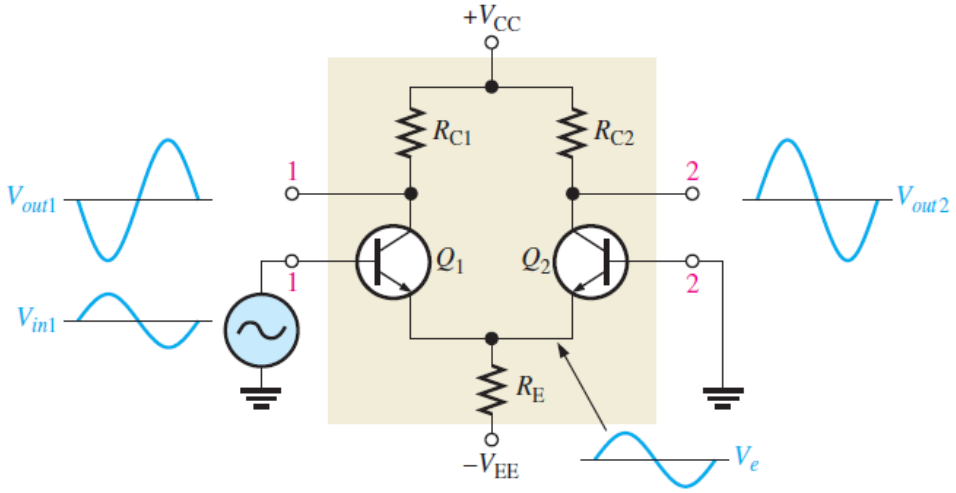


Figure 11: Single-ended differential input operation – output at node 2

The signal is applied to input 2 with input 1 grounded, as shown in the figure below, an inverted, amplified signal voltage appears at output 2. In this situation, Q_1 acts as a common-base amplifier, and a non-inverted, amplified signal appears at output 1.

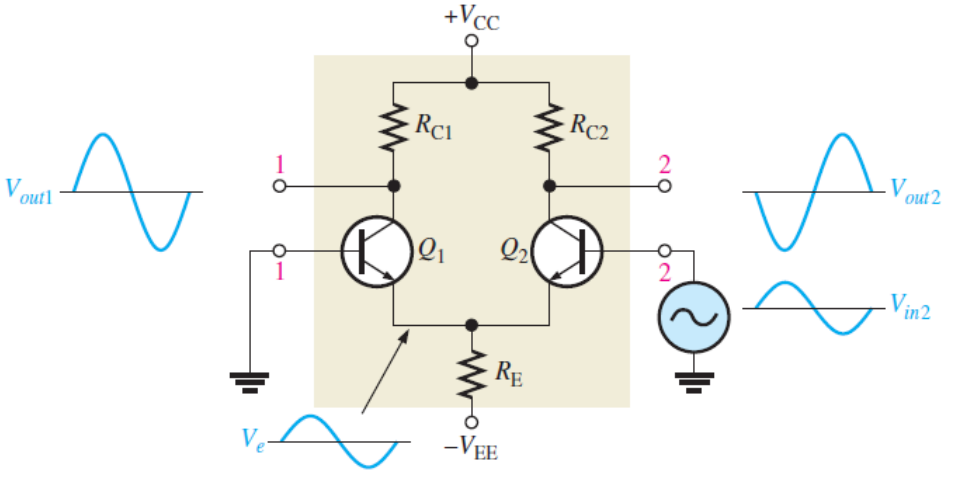


Figure 12: Single-ended differential input operation – output at node 1

7.2. Double-Ended Differential Input

In the double-ended differential input configuration, two opposite-polarity (out-of-phase) signals are applied to the inputs, as shown in the figure below.

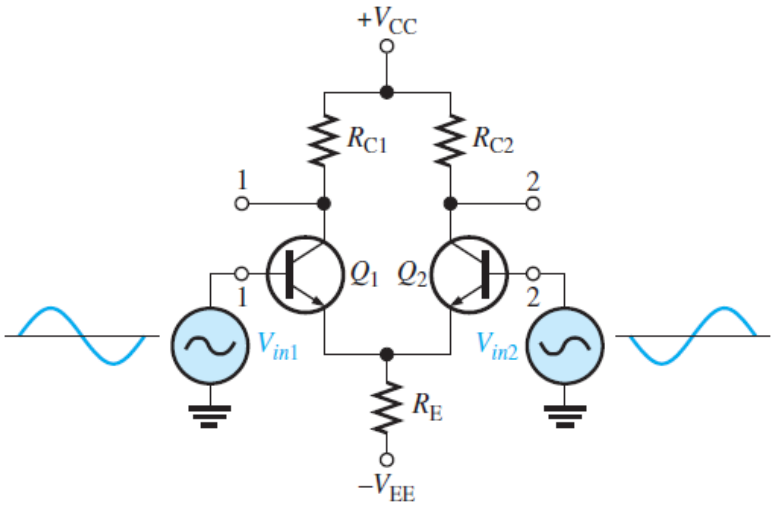


Figure 13: Differential inputs (180 out of phase)

Figure below shows the output signals due to the signal on input 1 acting alone as a single-ended input.

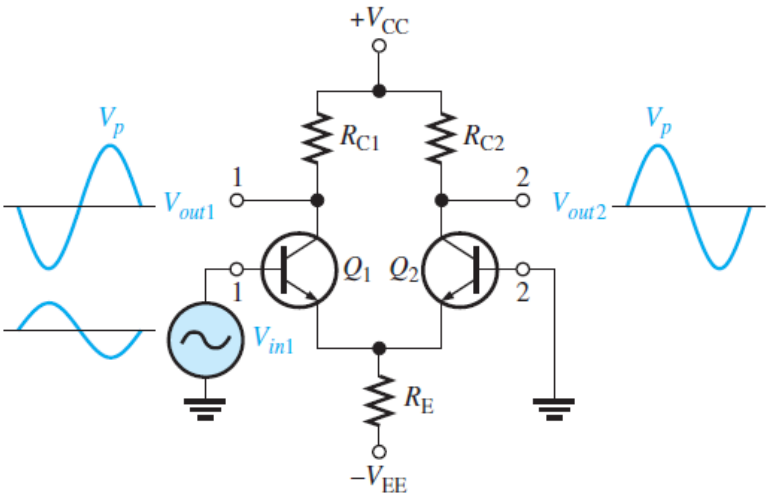


Figure 14: Differential inputs - outputs due to V_{in1}

Figure below shows the output signals due to the signal on input 2 acting alone as a single-ended input. Notice in the above and below circuit arrangements that the signals on output 1 are of the same polarity. The same is also true for output 2.

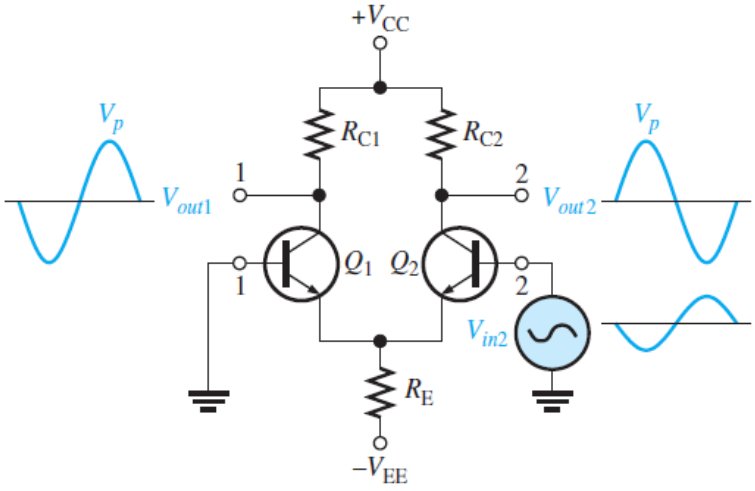


Figure 15: Differential inputs - outputs due to V_{in2}

By applying the superposition theorem and summing both output 1 signals and both output 2 signals, you get the total output signals, as shown in the figure below.

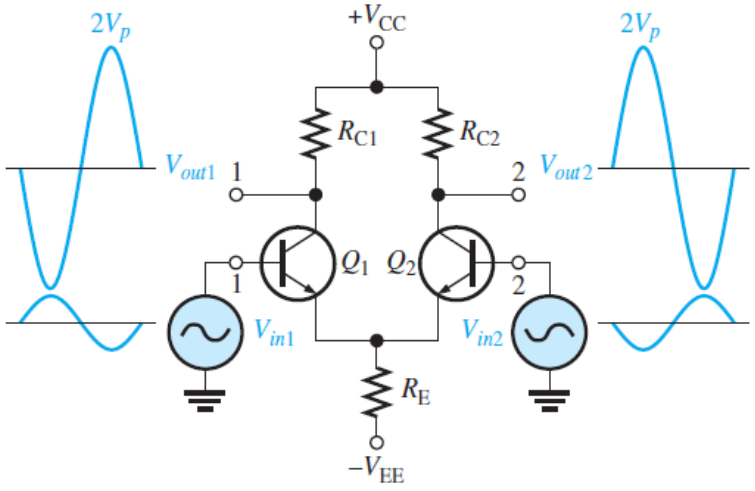


Figure 16: Differential inputs - total outputs

7.3. Common Mode Inputs

In the common mode input, two signal voltages of the same phase, frequency, and amplitude are applied to the two inputs, as shown in the figure below.

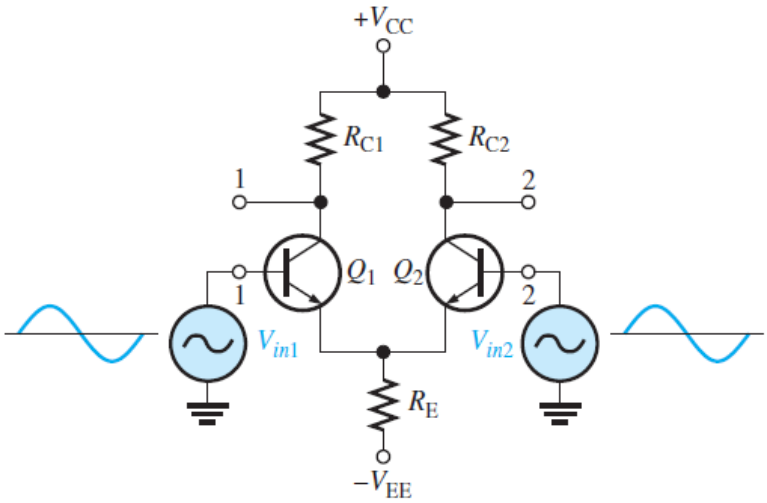


Figure 17: Common-mode inputs (in phase)

The output signals due to the signal on only input 1, as shown in the figure below.

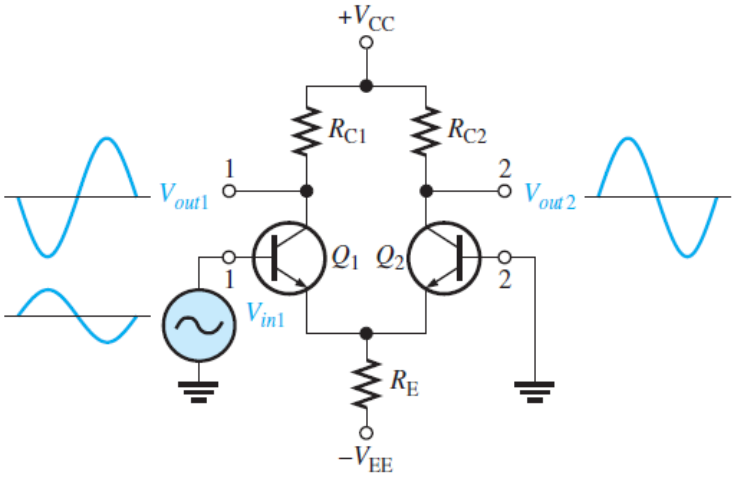


Figure 18: Common-mode inputs - outputs due to V_{in1}

As shown in the figure below, the output signals due to the signal on only input 2. Notice that the corresponding signals on output 1 are of the opposite polarity, and so are the ones on output 2.

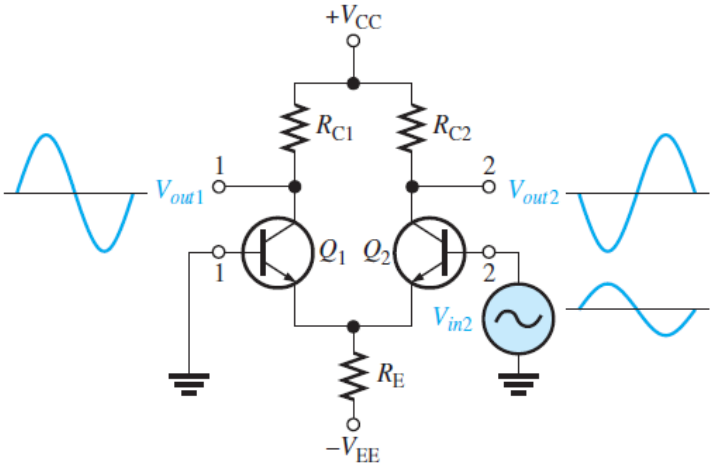


Figure 19: Common-mode inputs - outputs due to V_{in2}

When the input signals are applied to both inputs, the outputs are superimposed and they cancel, resulting in a zero-output voltage, as shown in Figure below. This action is commonly termed as common-mode rejection.

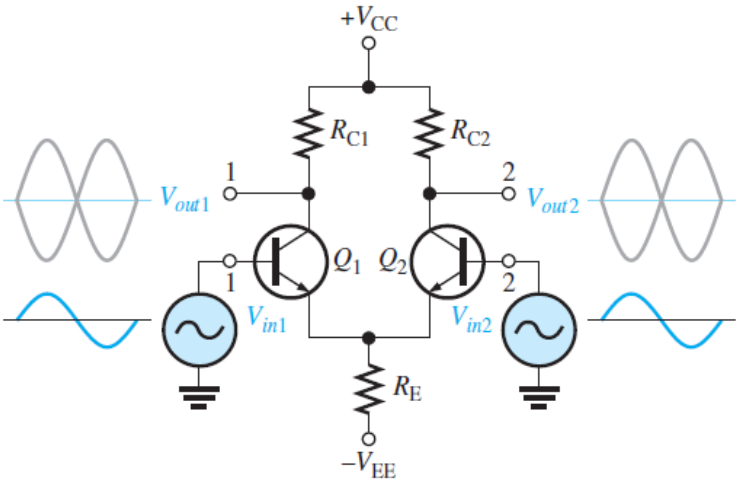


Figure 20: Common-mode inputs - outputs due to V_{in1} and V_{in2} cancel because they are equal in amplitude but opposite in phase. The resulting outputs are 0 V AC.

The common-mode rejection means that this unwanted signal will not appear on the outputs and distort the desired signal. Common-mode signals (noise) generally are the result of the pick-up of radiated energy on the input lines from adjacent lines, the 60 Hz power line, or other sources.

Ideally, a differential amplifier provides a very high gain for desired signals (single-ended or differential) and zero gain for common-mode signals.

Practical differential amplifiers, however, do exhibit a very small common-mode gain (usually much less than 1), while providing a high differential voltage gain (usually several thousand). The higher the differential gain with respect to the common-mode gain, the better the performance of the differential amplifier in terms of rejection of common-mode signals.

Hence, we have a measure of the differential amplifier's performance in rejecting unwanted common-mode signals is the ratio of the differential voltage gain A_{dm} to the common-mode gain, A_{cm}. This ratio is the common-mode rejection ratio, CMRR.

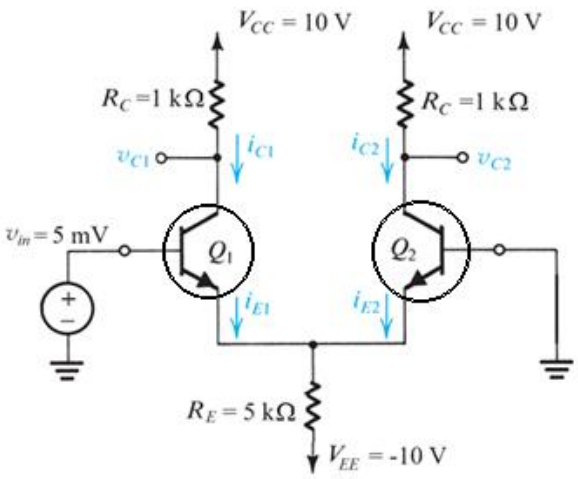
$$\text{CMRR} = \frac{A_{dm}}{A_{cm}}$$

The higher the CMRR, the better. A very high value of CMRR means that the differential gain A_{dm} is high and the common-mode gain A_{cm} is low. The CMRR is often expressed in decibels (dB) as:

$$\text{CMRR} = 20 \log\left(\frac{A_{dm}}{A_{cm}}\right)$$

Example 5 – BJT Differential Amplifier Circuit

For the differential amplifier circuit given below, considering identical transistors used in the circuit, the DC gain of the BJT is $\beta_{Q1} = \beta_{Q2} = 100$ and V_{BE} = 0.7 V. Due to high DC gain of the transistors, assume that currents $I_{C1} = I_{C2} = I_{E1} = I_{E2}$.



Calculate the following circuit parameters of the differential amplifier:

a. The input impedance (Z_{in}) if terminal voltage V_T = 25 mV. [8 marks]

b. The AC output voltage if the output is taken across the terminals v_{C1} and v_{c2}. [6 marks]

Answer

a. For the given differential amplifier circuit, the tail current is:

$$I_T = \frac{V_{CC}}{R_E} = \frac{10\text{ V}}{5\text{ k}\Omega} = 2\text{ mA}$$

Assuming identical transistors, the current that flows in the emitter is:

$$I_{E1} = I_{E2} = \frac{I_T}{2} = \frac{2\text{ mA}}{2} = 1\text{ mA}$$

If terminal voltage, V_T = 25 mV, the AC emitter internal resistance is:

$$r_e' = \frac{25\text{ mV}}{I_E} = \frac{25\text{ mV}}{1\text{ mA}} = 25\ \Omega$$

The input impedance of the differential amplifier is:

$$Z_{in} = 2\beta r_e' = 2(100)(25\ \Omega) = 5\text{ k}\Omega$$

b. As currents $I_E = I_C$, the voltage at the collector is:

$$V_C = V_{CC} - I_C R_C = 10\text{ V} - (1\text{ mA})(1\text{ k}\Omega) = 9\text{ V}$$

For the given common emitter leg of the circuit, the AC voltage gain is:

$$A_v = \frac{R_C}{r_e'} = \frac{1\ \text{k}\Omega}{25\ \Omega} = 40$$

Considering V_{in} = 5 mV, the AC output voltage is:

$$V_{out} = A_v V_{in} = 40(5\ \text{mV}) = 200\ \text{mV}$$

8. Phase Splitter

The circuit given in the diagram below produce two output signals that are inverted with respect to each other.

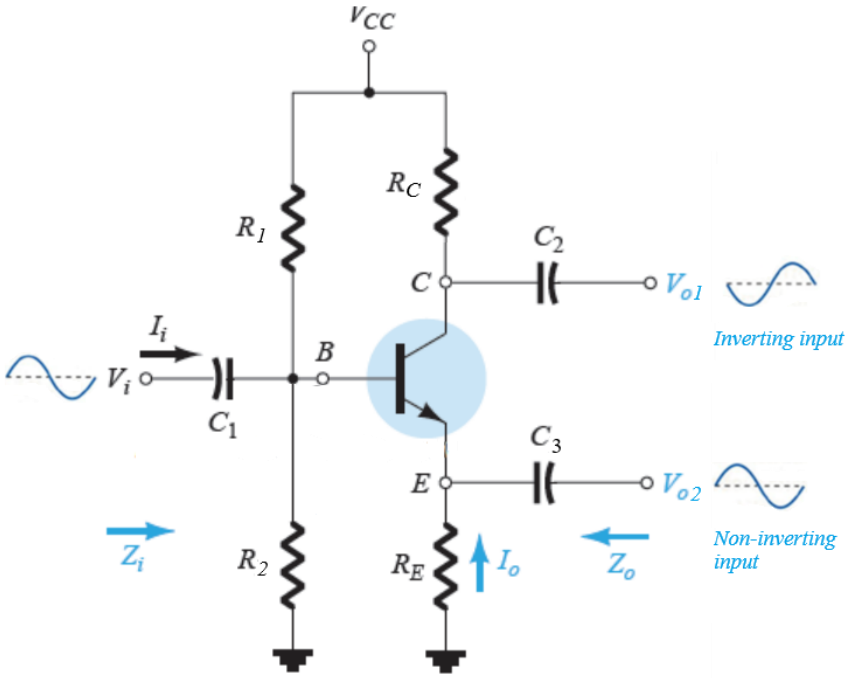


Figure 21: Phase splitter circuit

By taking outputs from both emitter and collector, we have combined an inverting amplifier and a non-inverting amplifier into a single stage.

We can make R_E = R_C to give a voltage gain of -1 for inverting output. This results in two signals are of identical amplitude but opposite in phase.

9. Voltage Regulator

The emitter follower (i.e. common collector amplifier) as discussed before produces a voltage that is determined by its input voltage (i.e. -0.7 V offset). It also has a low output resistance, so that it will not be significantly affected by the load connected to it.

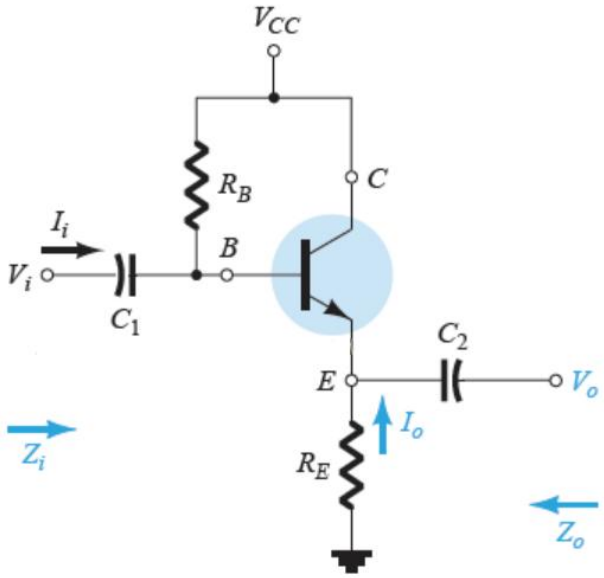


Figure 22: Voltage follower

We can then be used as voltage regulator i.e. use of a Zener diode on input which together with resistor forms a voltage reference for the base input.

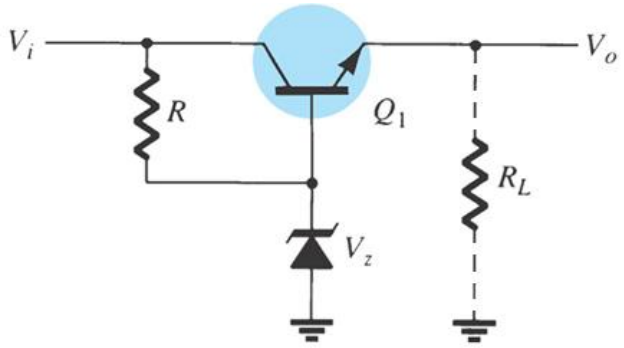


Figure 23: Basic voltage regulators using an NPN transistor

In practice, with op amp as error-detector differential amplifier, there are two types of series voltage regulator: series voltage regulator and shunt voltage regulator.

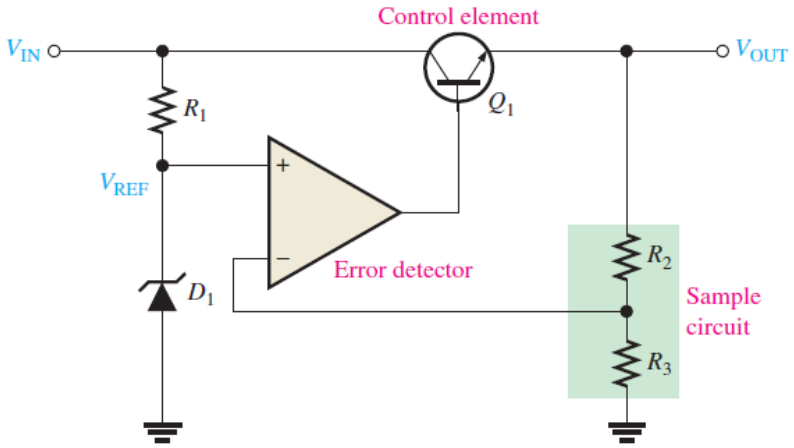


Figure 24: Series voltage regular circuit

As shown above, a series voltage regulator has its switching transistor in series with the load.

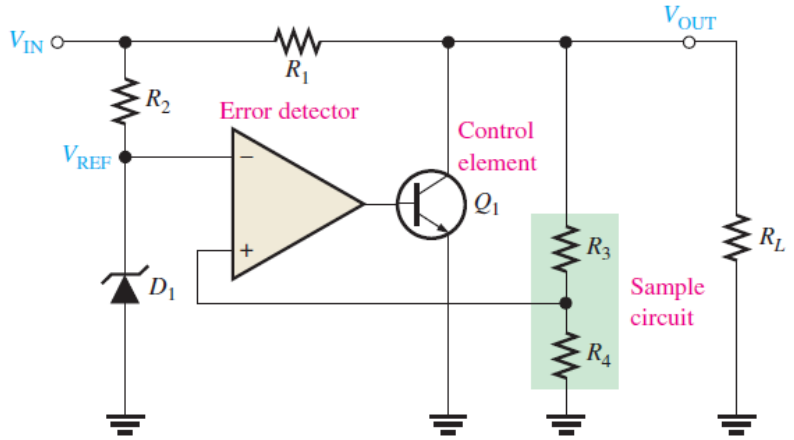


Figure 25: Parallel voltage regulator circuit

On the other hand, in a parallel voltage regulator circuit, its switching transistor is in parallel with the load.

10. Switches and Logic Gates

We use of BJT as a switch already discussed earlier and we use cut-off and saturation regions of operation.

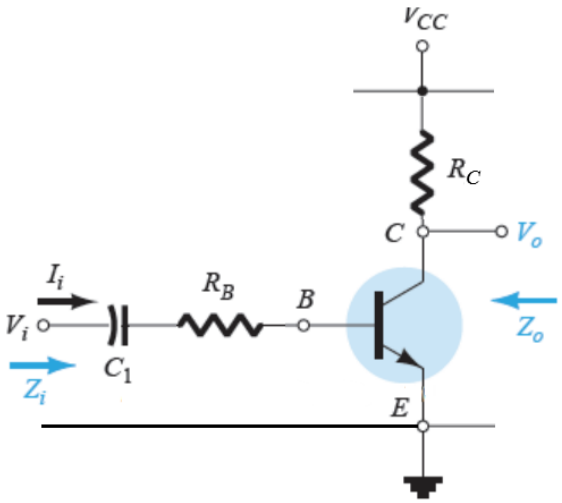


Figure 26: A simple inverter circuit

As shown in the figure above, a simple inverter circuit could be realised by arranging BJT as a common emitter amplifier circuit. The inversion nature of common-emitter configuration makes the output signal of the amplifier (V_o) as the amplified and inverted version of the input signal (V_i).

The following circuit shows a more realistic NAND gate with BJT transistor. With this more complex logic circuit, several BJTs are arranged in stages forming a cascaded arrangement of the transistors.

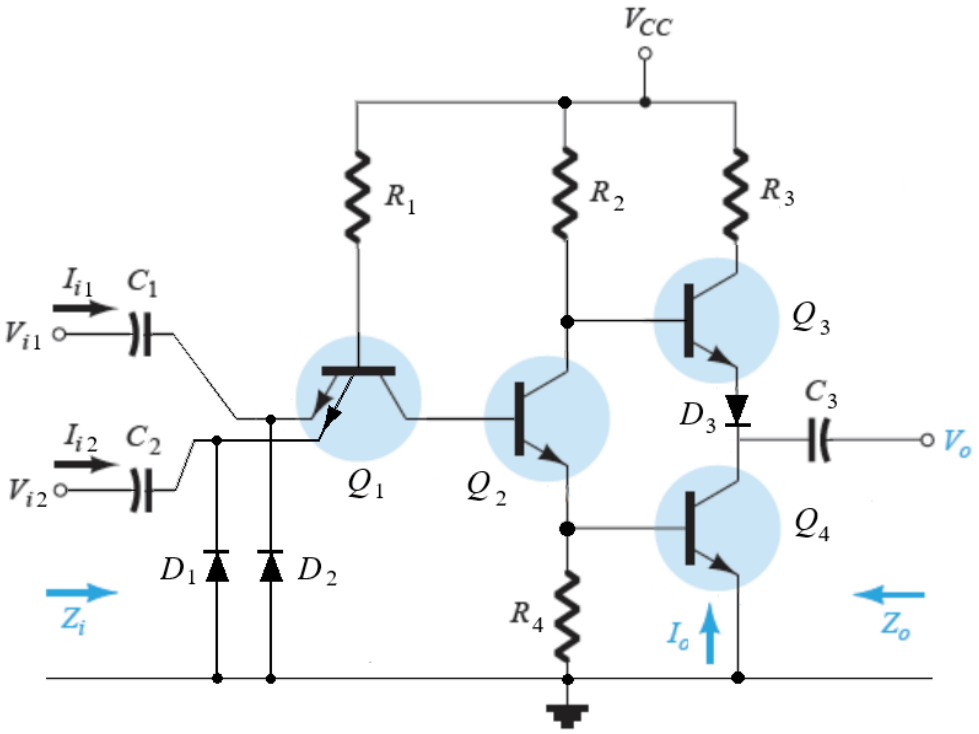


Figure 27: A more realistic NAND gate circuit

In the input stage, when both of the signals are "High" voltage at the inputs of the circuit e.g. A and B, transistor T_1 is on. But, if only one of the input signals is "High" or when both are "Low", T_1 is off. In this stage, diodes D_1 and D_2 are functioning as pull-up diode preventing any negative voltages to enter the circuit.

A	B	X
0	0	1
0	1	1
1	0	1
1	1	0

Table 1: Logic table of NAND gate circuit

Then, in the subsequent buffer stage, when transistor T_1 is on, then transistor T_4 is on whereas T_3 is off. On the other hand, when T_1 is off, transistor T_3 is on and transistor T_4 is off. Notice that in this logic gate circuit, transistor T_1 is dealing with the input signals whereas transistor T_2 is acting as a buffer between the input and the output.

At the output stage of the circuit, when transistor T_2 is on, both of T_3 and T_4 transistors are on. In the output stage, the role of diode D_3 is to provide biasing for transistors T_3 and T_4. So, when transistor T_2 is on, only transistor T_4 is on, not both of transistors T_3 and T_4 and when transistor T_2 is off, only transistor T_3 is on whereas T_4 is off.