VICTORIA UNIVERSITY OF WELLINGTON
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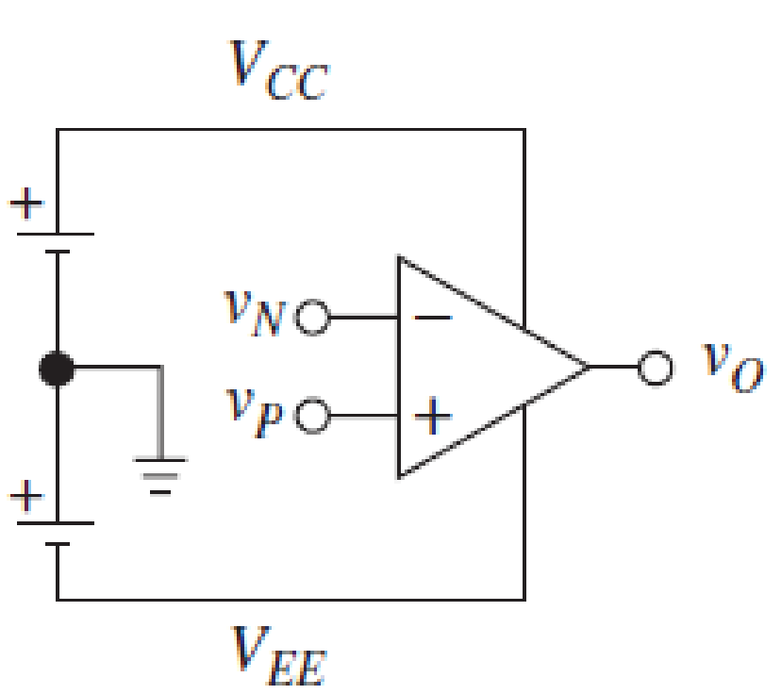
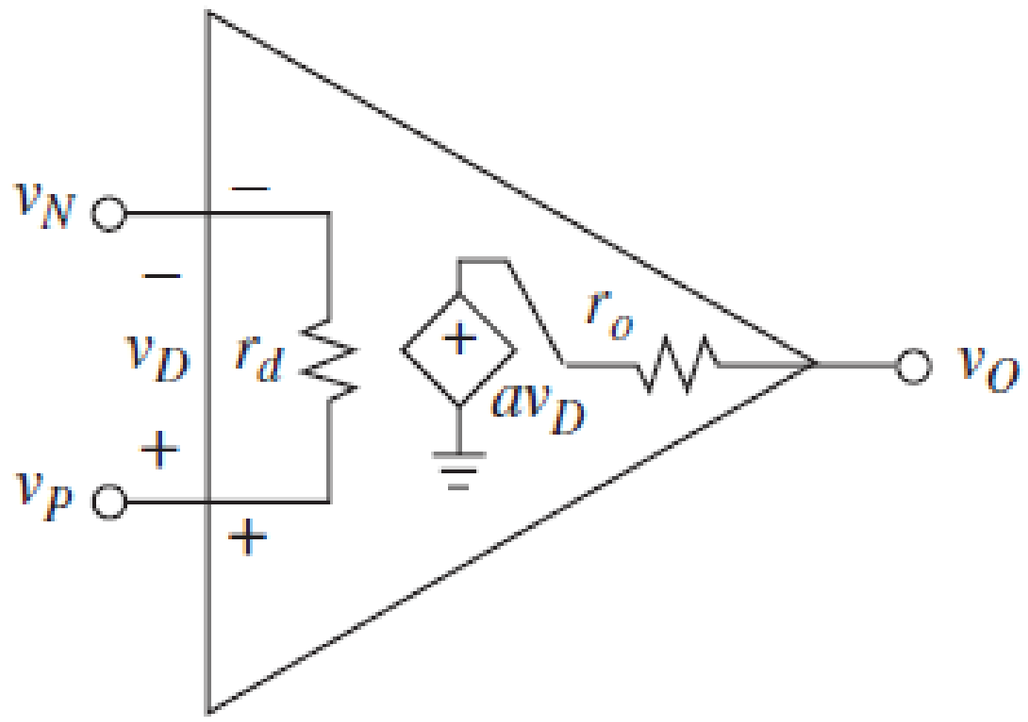
Static Limitations

XMUT303 Analogue Electronics

Topics

1. Static imperfections.
2. Input offset voltage.
3. Input bias and offset currents.
4. Nulling.
5. Monte Carlo analysis.





Static Imperfections

- Static limitation: imperfection and limitation of op-amp due to input-referred errors, noticeable in high DC gain applications.
- Examples topics are input offset voltage, input bias current, and input offset current.
- Related other topics such as CMRR and gain non-linearity.

Static Imperfections

- Input offset voltage: voltage required between the inputs of the op-amp to make the output zero.
- Input bias current: a small current flows into both inputs to bias the input transistors of the op amp.
- Input offset current: difference between input bias current at inverting and non-inverting inputs of the op amp.
- Nulling: Effort to remove or null the input voltage or current imperfections of the op amps.

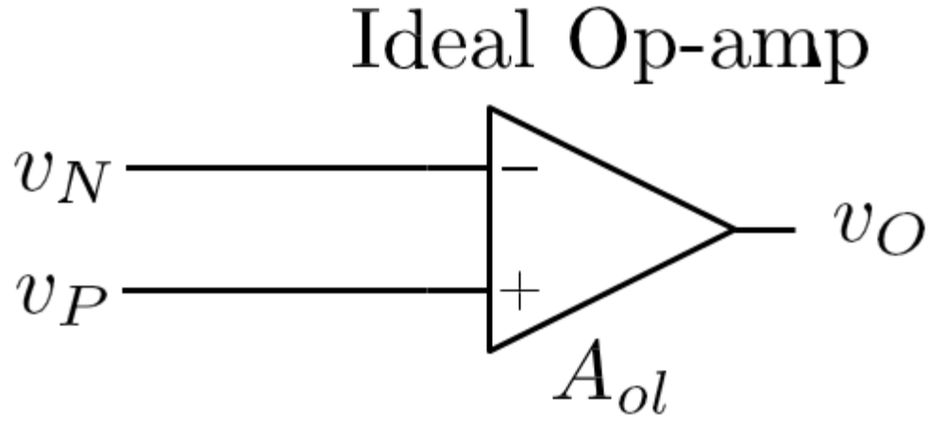
Static Imperfections

- Input bias current, input offset current, and input offset voltage of practical op amps from their manufacturer datasheets.

Op Amp	$\mathbf{V_{OS}}$	$\mathbf{I_B}$	$\mathbf{I_{OS}}$
NE5534	0.5 mV	800 nA	10 nA
LF411	0.8 mV	50 pA	25 pA
LM318	4 mV	150 nA	30 nA
uA741	1 mV	80 nA	20 nA

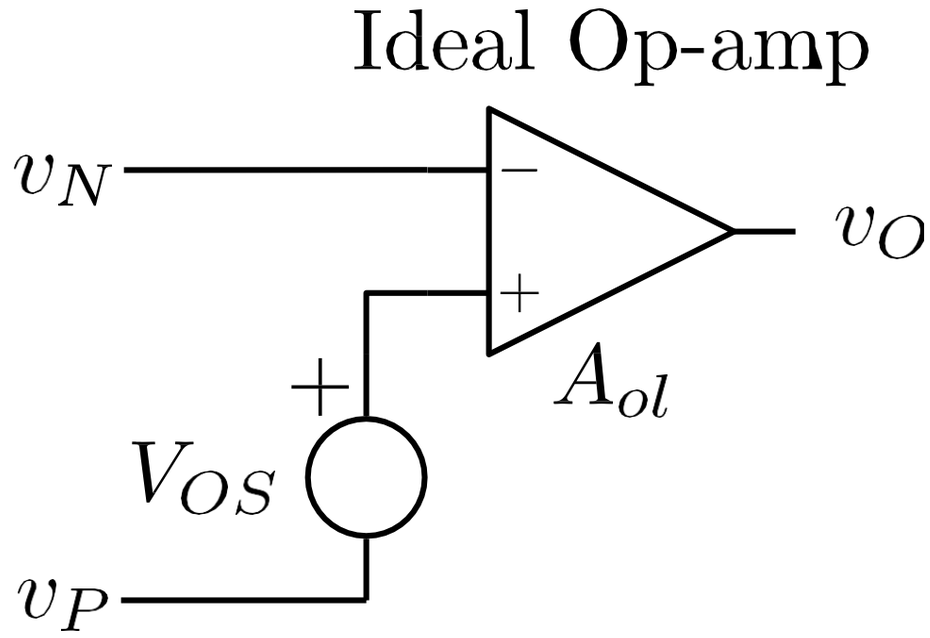
Input Offset Voltage

- Ideally, shorting $V_N = V_P$ should give $V_o = 0$.
- Practical op amp will generally yield $V_o \neq 0$.
- This is due to inherent mismatches between the input stage of op amp.
- To force V_o to zero, a suitable correction voltage must be applied between the pins.



Input Offset Voltage

- Practically, imbalance between V_N and V_p leads to some offset at V_o.



- V_{OS} is the input offset voltage i.e. a tiny voltage source in series with one of op-amp inputs.

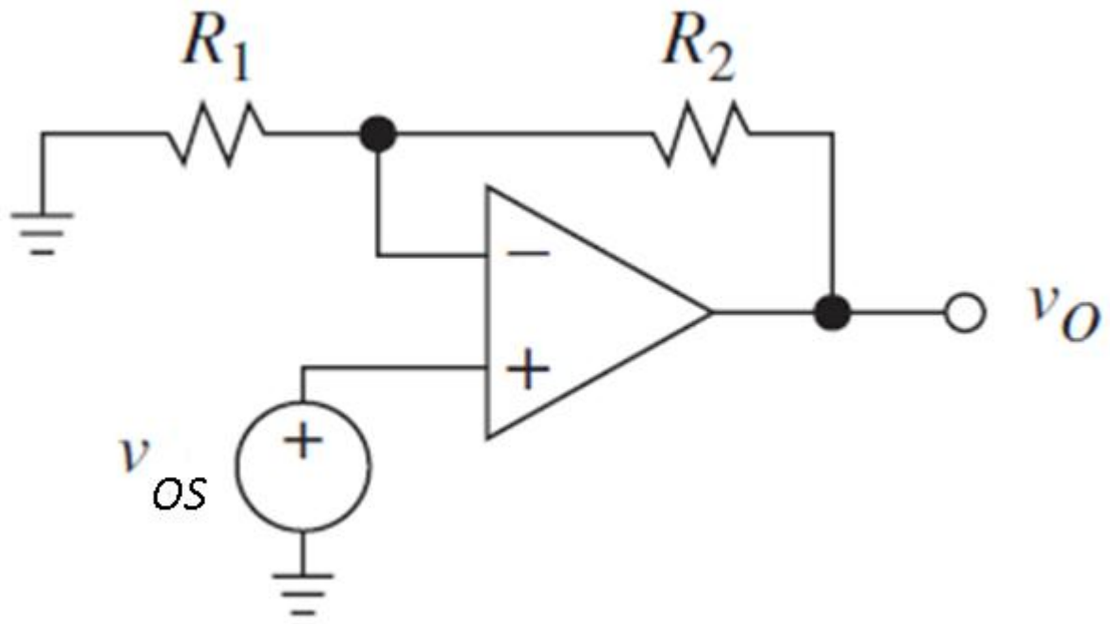
$$V_O = A_{ol}(V_P - V_N + V_{OS})$$

Errors Caused by V_{OS}

- Error voltage added to output voltage as a result offset voltage is multiplied by the DC noise gain.
- The larger the noise gain, the larger the error. For a non-inverting amplifier, this is:

$$E_O = \left(1 + \frac{R_2}{R_1}\right) V_{OS}$$

- For uA741 with 1000 times gain, V_{OS} = 2-6 mV.



Stability of V_{OS}

The offset voltage, V_{OS} experiences drifts with temperature and time:

- Temperature coefficient = $\partial V_{OS}/\partial T$ (µV/K).
- Typical values: 5 µV/°C for general purpose op amp like uA741 and 0.2 µV/°C for low-input voltage op amp such as OP77.
- Some (low-offset) op amps specify drift characteristics in their data sheets.
- Not usually covered for general purpose op amps (i.e. time drift especially).

Common Mode Effects

- Ideally, V_o is only determined by difference between V_P and V_N.

$$V_o = A_{ol}(V_P - V_N) \qquad \text{for} \quad A_{ol} \to \infty$$

- Practically, common-mode voltage also affects V_o.

$$V_o = A_{ol}(V_P - V_N) + A_{CM}\left(\frac{V_P + V_N}{2}\right)$$

Common Mode Response

Common Mode Rejection Ratio (CMRR):

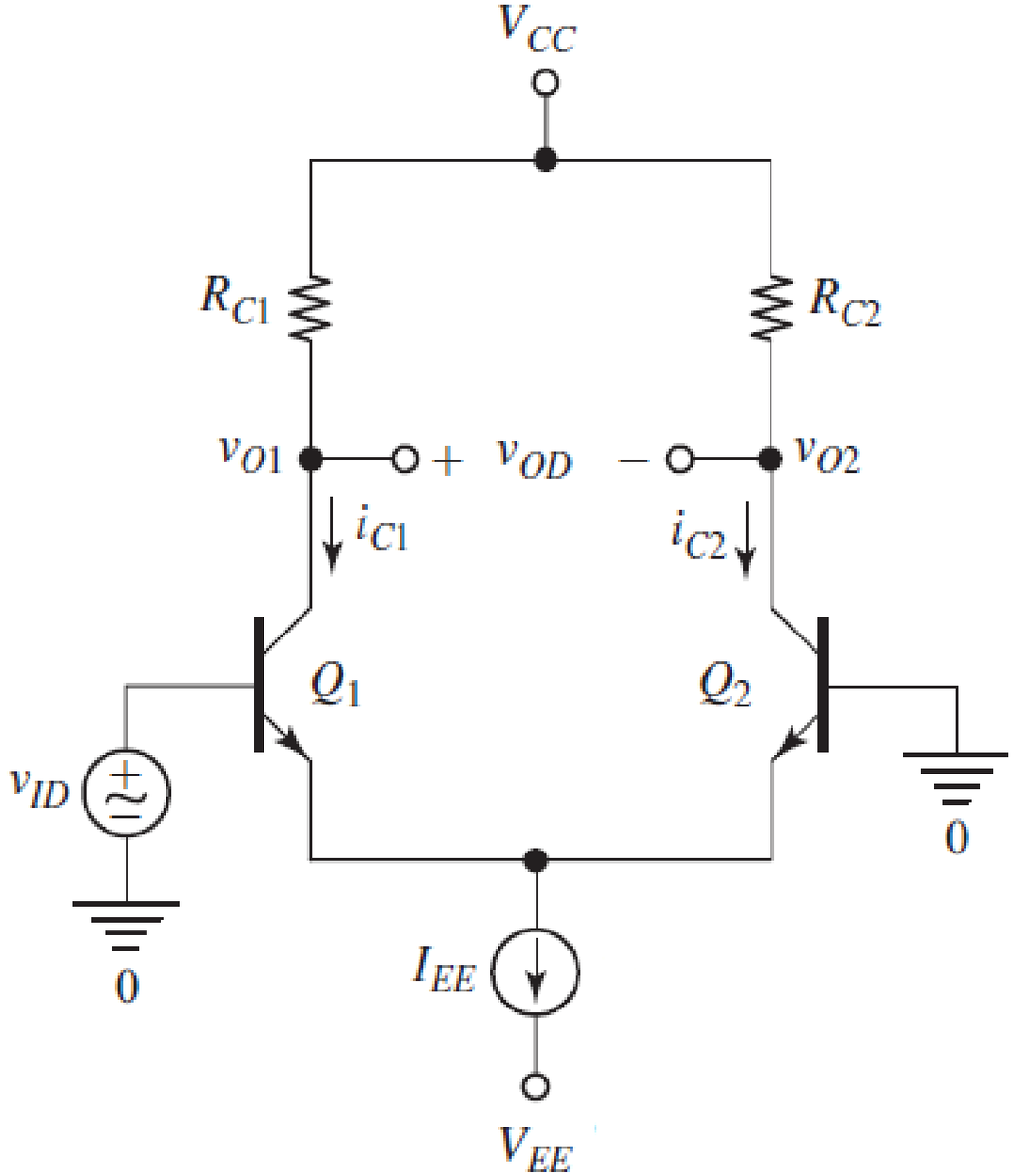
$$\text{CMRR} = \left|\frac{A_{ol}}{A_{cm}}\right|$$

- Ideally CMRR = ∞.
- Practically CMRR ~ 100-120 dB at DC.
- CMRR rolls off above ~ 100 Hz.

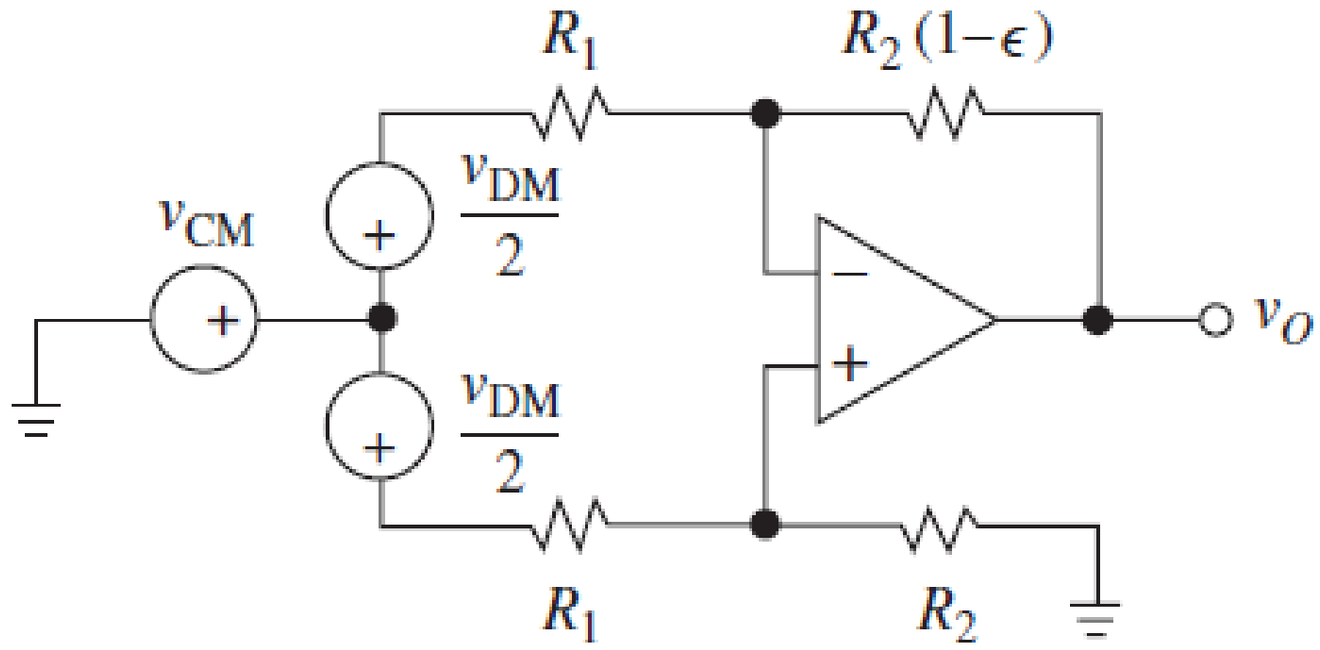
Common Mode Response

Finite CMRR is due to:

- Input stage imbalances.



- External component flaws.



Common Mode Response

- Knowing that:

$$V_{cm} = \frac{(V_P + V_N)}{2} \qquad \text{and} \qquad \text{CMRR} = \frac{A_{ol}}{A_{cm}}$$

- Provided V_{CM} is constant, model as part of V_{OS}.

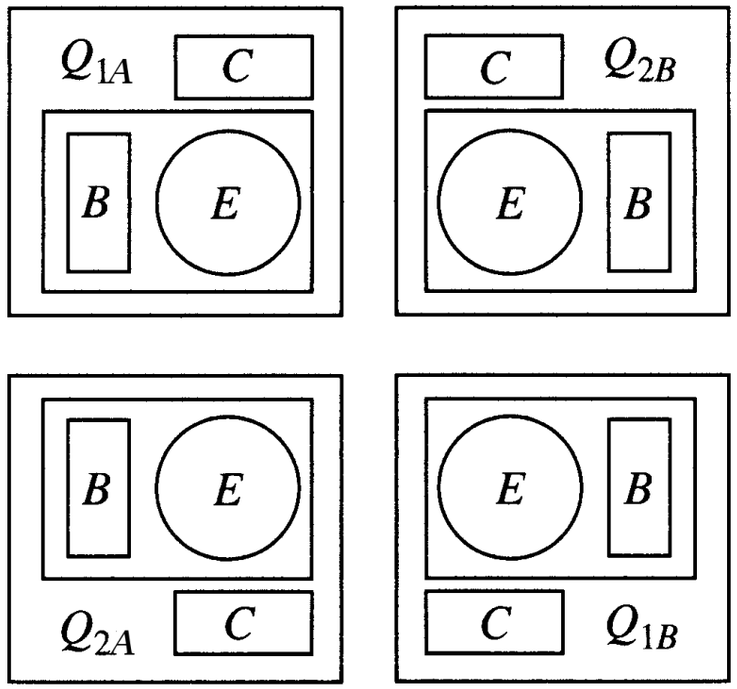
$$V_o = A_{ol}(V_P - V_N + V_{os}) + \left(\frac{A_{ol}}{\text{CMRR}}\right) V_{cm}$$

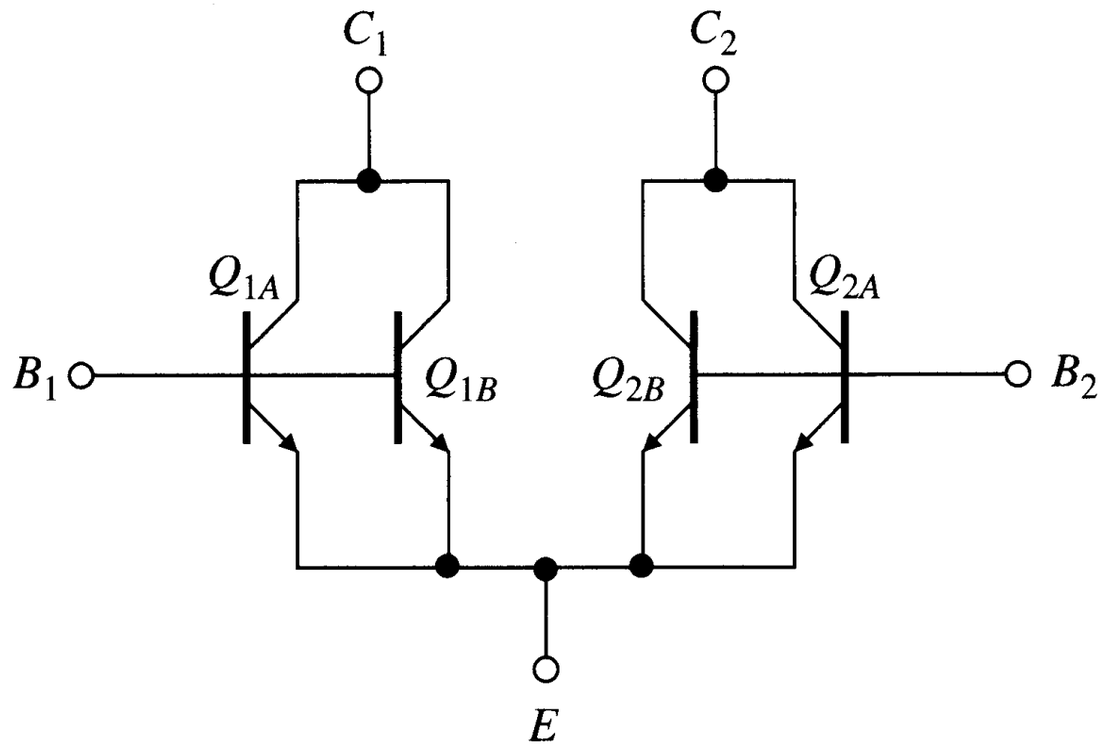
$$= A_{ol}\left(V_P - V_N + V_{os} + \frac{V_{cm}}{\text{CMRR}}\right)$$

- Simplifies calculations, as we already know how to deal with V_{OS}.

Minimising V_{OS}

Interleaved transistors: e.g. alternating in between.



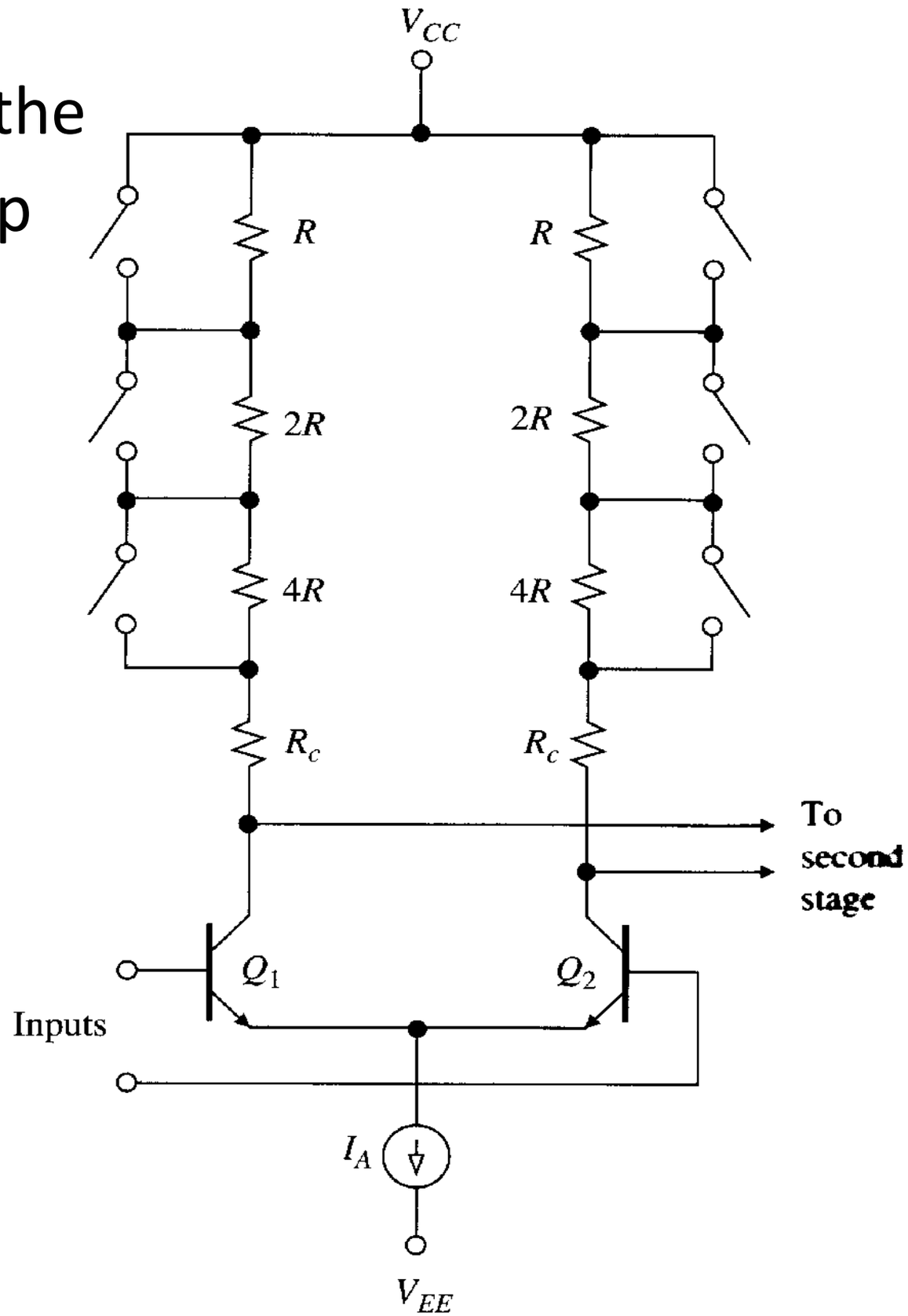


- Minimising the offset by purposeful placement and geometric layout design of complementary components in the device.
- This is also done by grouping or pairing up self-compensated components.

Minimising V_{OS}

Voltage trimming: adjusting the voltage at the input of the op amp by a small amount.

- Perform precision calibration of the differential input.
- Minimising the V_{OS} by providing an internal ladder of resistors network for eliminating the offset.



Minimising V_{os}

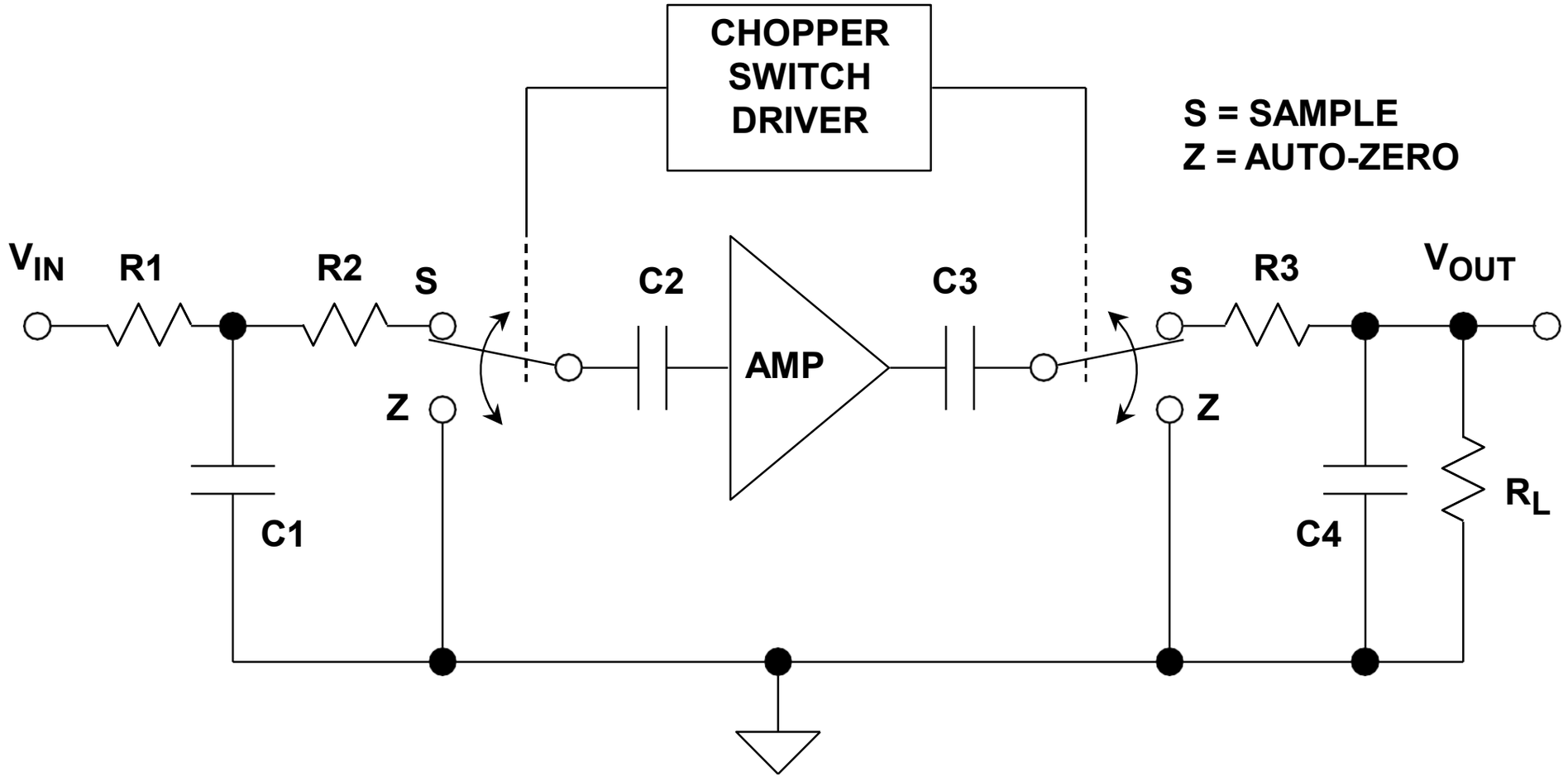
Chopper-stabilised op-amps constantly correct low-frequency errors such as:

- input offset voltage,
- input bias current,
- temperature drift, or
- pink $(1/f)$ noise in the inputs of the amplifier.

	Conventional (with trim-resistor correction)	**Chopper Stabilised**
Offset input error	100 μV - 2 mV	Up to 8 μV
Temperature accuracy (-40°C to 125°C)	0.02 μV/°C	1.5 μV/°C

Minimising V_{OS}

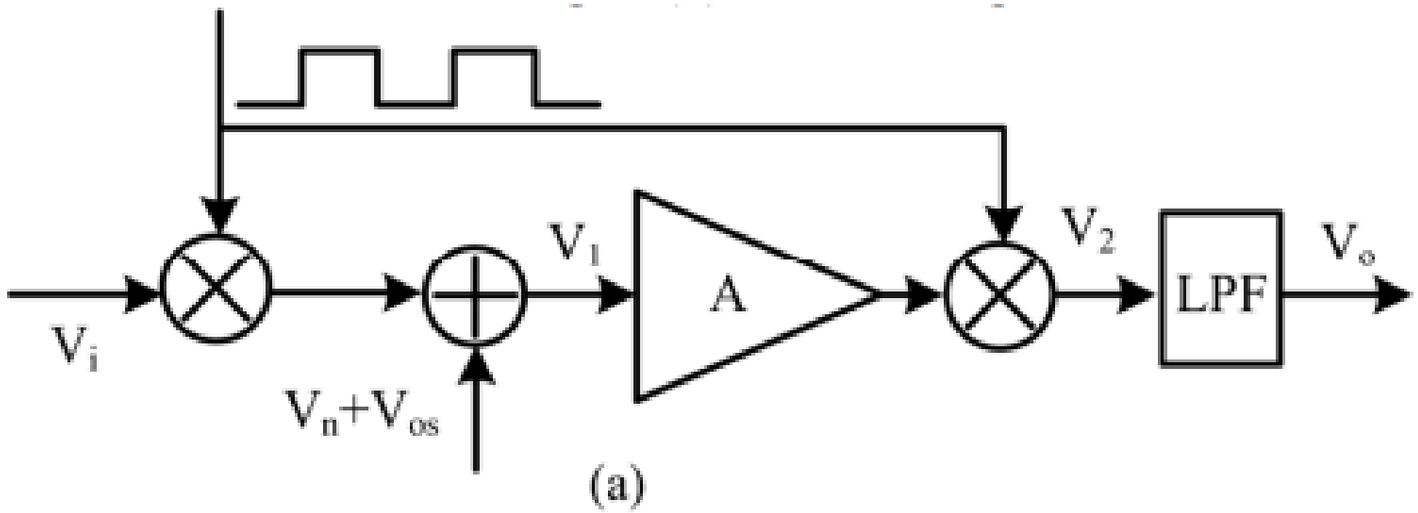
- The best op amps offer offset voltages of 25 µV and 0.1 µV/ºC drift.
- Offset voltage and drift less than these values require a chopper.
- Capacitors C_2 and C_3 are charged to the amplifier input and output offset voltage.



Minimising V_{os}

By looking at the frequency spectra of the chopping circuit, we could see how offset voltage is removed:

- Before chopper: input signal + offset and noise signals.
- After chopper: only input signal.



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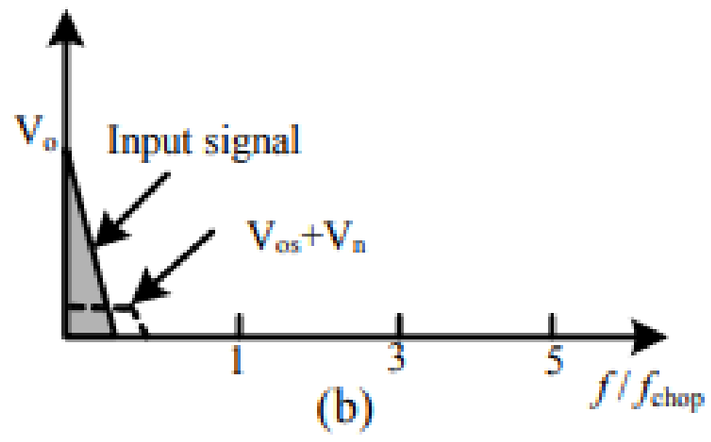

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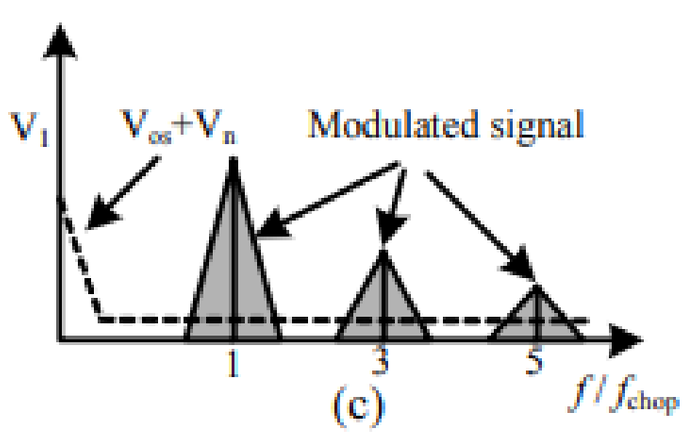
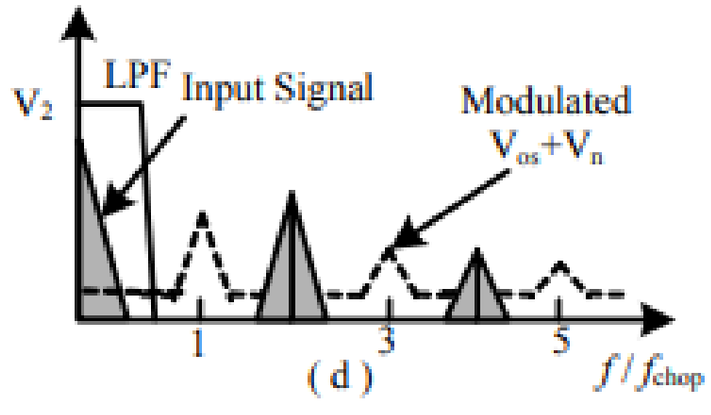


(c)



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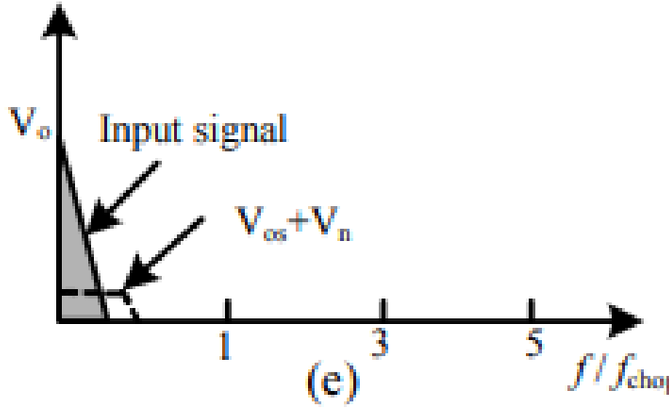
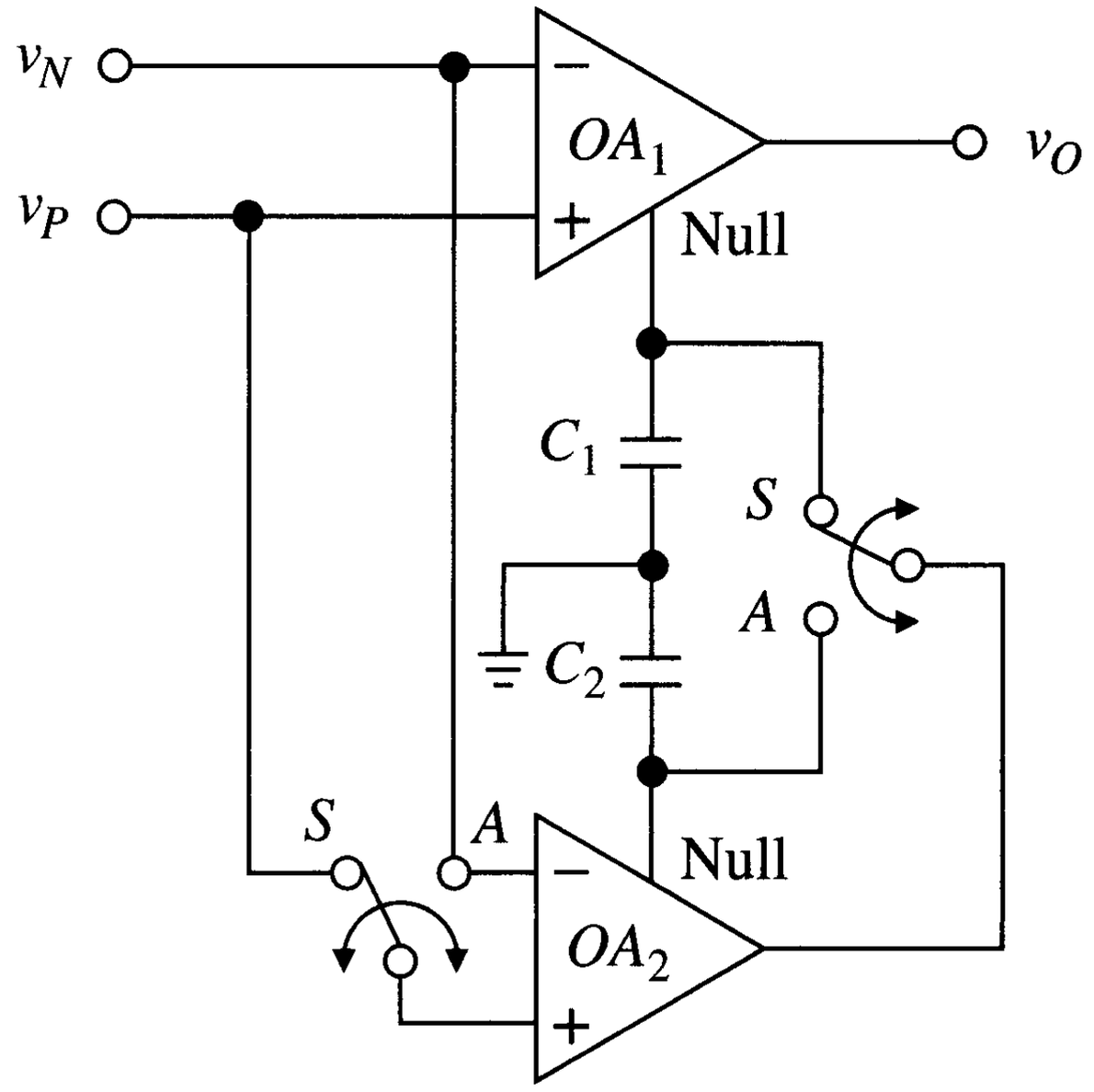


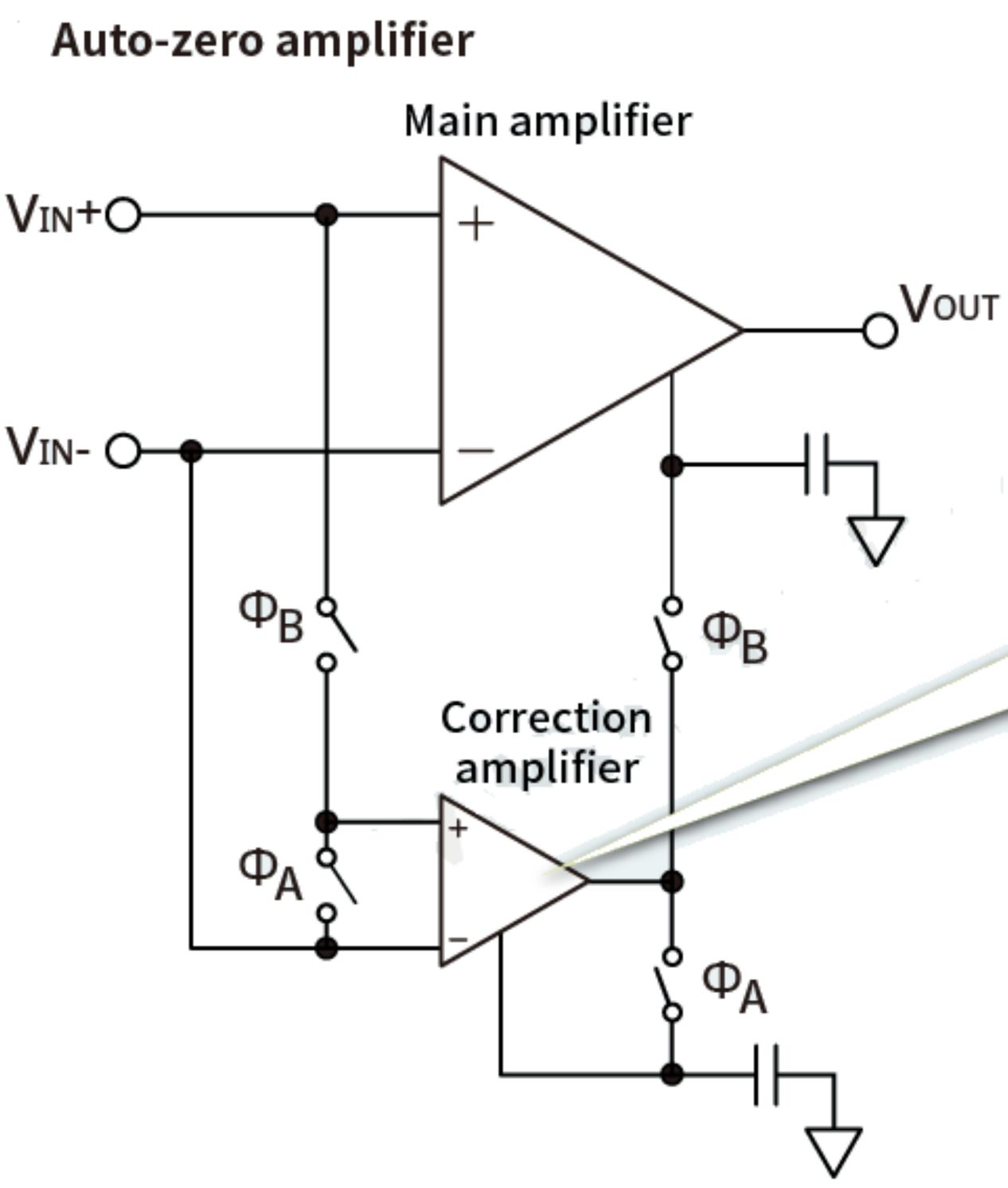
(e)

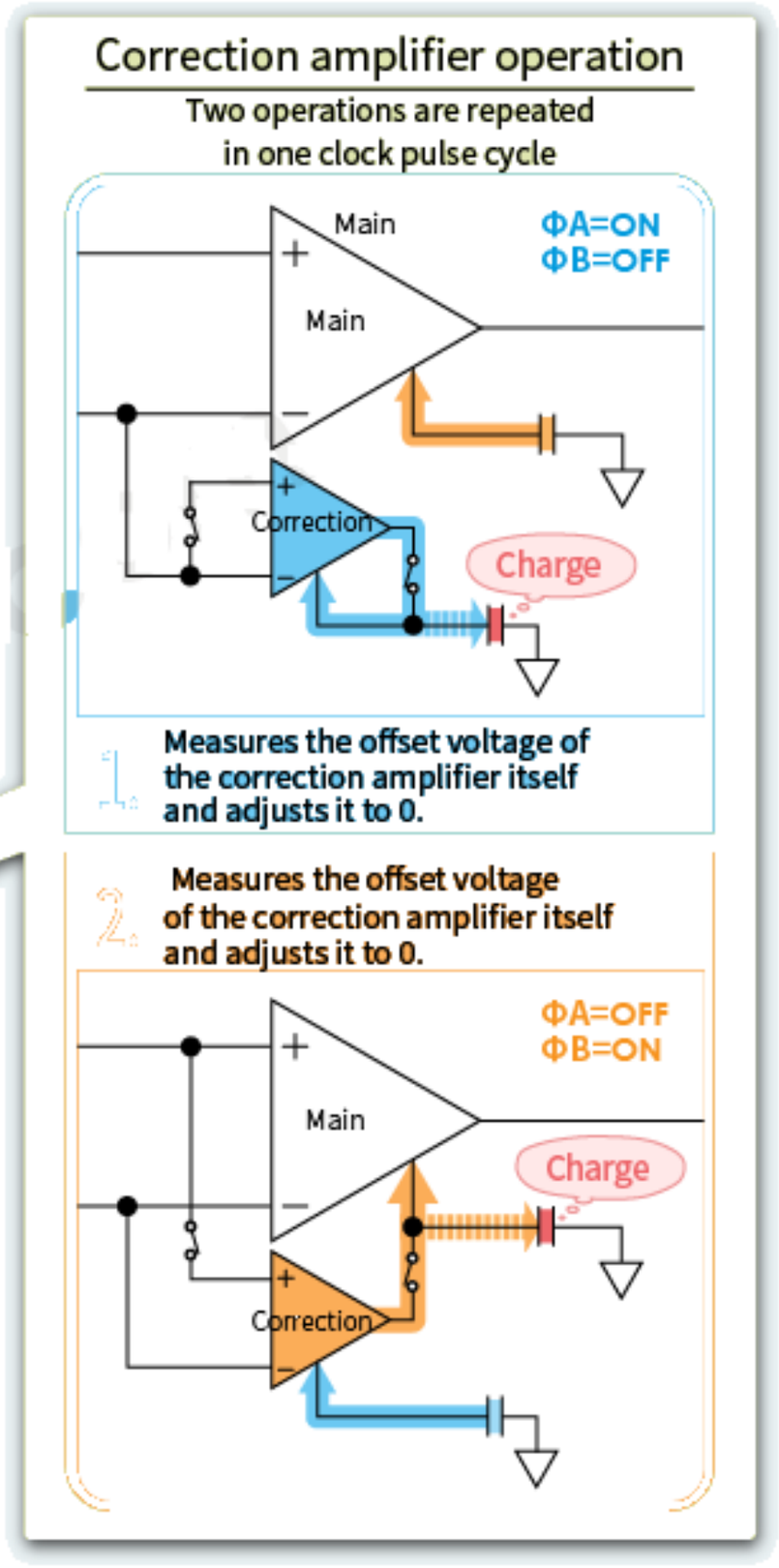
Minimising V_{OS}

- Auto-zero op amps contains internal circuitry that automatically correct offset voltage.
- Nulling amplifier, OA_2, monitors the input offset voltage of main amplifier OA_1.
- OA_2 drives OA_1's output to zero by applying a suitable correcting voltage at its null pin.



Minimising V_{os}





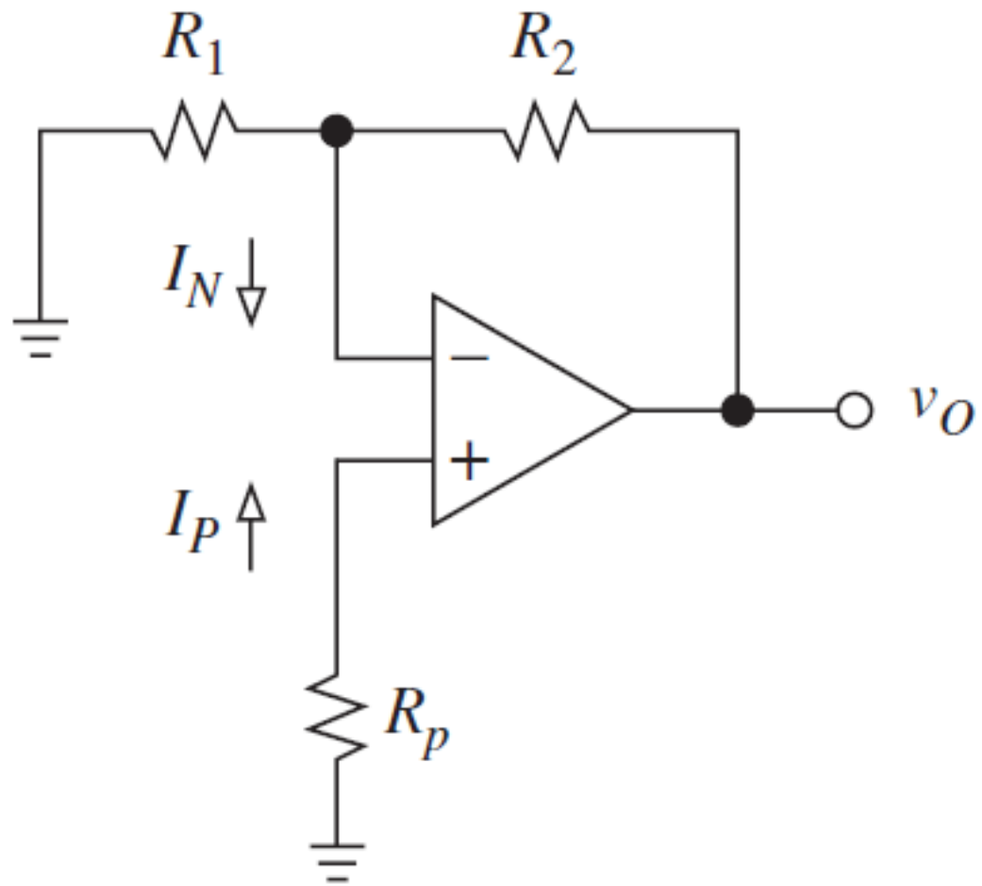
Example 1 of Offset Voltage V_{OS}

In the circuit of the figure below, let R_1 = 22 kΩ and R_2 = 2.2 MΩ, and let the op amp ratings be I_B = 80 nA and I_{OS} = 20 nA.

a. Calculate error voltage at the output E_O for the case R_p = 0. [6 marks]

b. Repeat, but with $R_p = R_1 \parallel R_2$ in place. [2 marks]

c. Repeat part (b), but with all resistances simultaneously reduced by a factor of 10. [2 marks]



Example 1 of Offset Voltage V_{OS}

d. Repeat part (c), but with the op amp replaced by one with I_{OS} = 3 nA. [2 marks]

e. Comment on the results obtained in parts (b) - (d) for reducing the error. [2 marks]

Example 1 of Offset Voltage V_{OS}

Solution

a. The DC noise gain is calculated from:

$$A = 1 + \frac{R_2}{R_1} = 1 + \frac{2.2\times10^6}{22\times10^3} = 101\ \text{V/V}$$

Moreover, since the value of R_2 is 100 times of R_1, a parallel of R_1 and R_2 is approximately:

$$R_p = (R_1 \parallel R_2) \cong 22\ \text{k}\Omega$$

With R_p = 0, the error is due to the input bias current, we have the error at the output voltage to be:

$$E_O = 101(R_1 \parallel R_2)I_N \cong 101(R_1 \parallel R_2)I_B$$
$$\cong 101(22\times10^3)(80\times10^{-9}) \cong 175\ \text{mV}$$

Example 1 of Offset Voltage V_{OS}

b. With $R_p = R_1 \parallel R_2 \cong 22\ \text{k}\Omega$ in place, the error is dominated by the input offset current, it is:

$$E_O \cong 101(22\times10^3)(\pm20\times10^{-9}) = \pm44\ \text{mV}$$

where we write "$\pm$" to reflect the fact that I_{OS} may be of either polarity.

c. Like part (b), with all resistances reduced by a factor of 10 (e.g. R_1 = 2.2 kΩ, R_2 = 220 kΩ, and R_p = 2.2 kΩ), we get the error in the output voltage to be:

$$E_O = 101(2.2\times10^3)(\pm\ 20\times10^{-9}) \cong \pm\ 4.4\ \text{mV}$$

Example 1 of Offset Voltage V_{OS}

d. Like part (c), with the op amp replaced by a better op amp with I_{OS} = 3 nA, the error in the output voltage is:

$$E_O = 101(2.2\times10^3)(\pm\ 3\times10^{-9}) \cong \pm\ 0.7\ \text{mV}$$

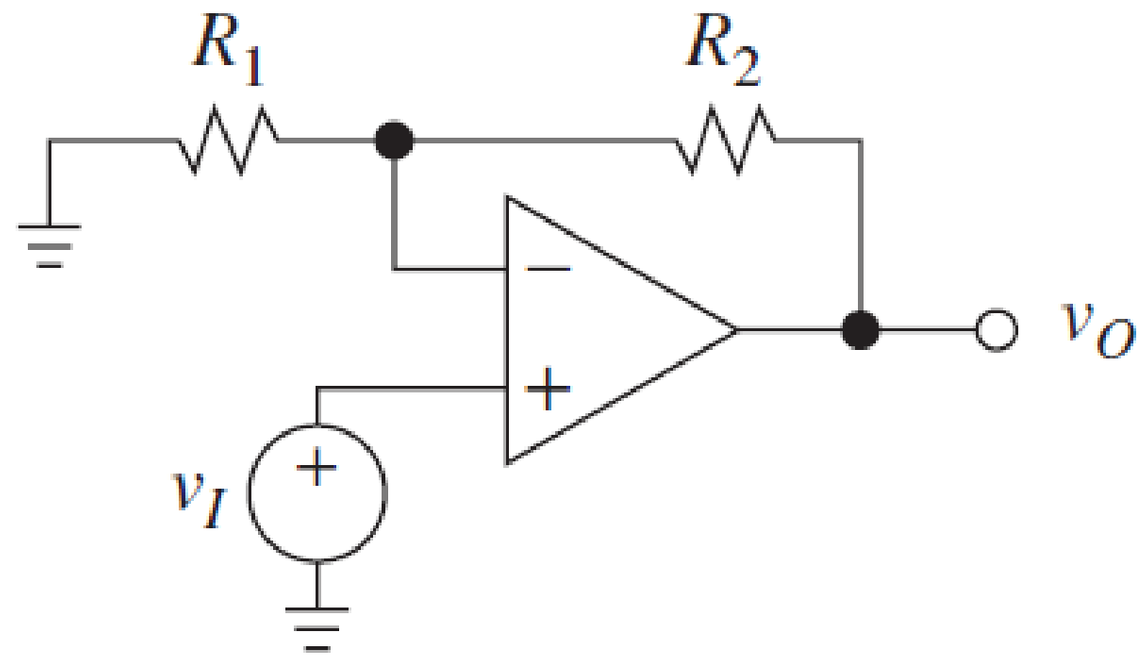
e. Summarising, with R_p in place, error in the output voltage E_O is reduced by 4; scaling the resistances reduces E_O by an additional factor of 10; finally, using a better op amp reduces it by yet another factor of 7.

Example 2 of Offset Voltage V_{OS}

A noninverting amplifier with a closed-loop gain of 1000 is designed using an op amp having an input offset voltage of 3 mV and output saturation levels of ±13 V.

a. What is the maximum amplitude of the sine wave that can be applied at the input without the output clipping?

[2 marks]



b. If the amplifier is capacitively coupled, what would the maximum possible amplitude be? [2 marks]

Example 2 of Offset Voltage V_{OS}

Solution

a. If the maximum output is 13 V, the maximum input is:

$$V_I(\max) = \frac{V_O}{A_v} = \frac{13\ \text{V}}{1000} = 13\ \text{mV}$$

At the non-inverting pin of the op amp, of that 3 mV is the offset, leaving a maximum signal amplitude of:

$$V_I'(\max) = V_I(\max) - V_{OS}$$
$$= 13\ \text{mV} - 3\ \text{mV} = 10\ \text{mV}$$

b. If the amplifier is capacitively coupled on the input, we can use superposition for the analysis, adding the DC offset voltage source and the AC input source.

Example 2 of Offset Voltage V_{OS}

Since for the DC source the gain path has an open circuit there will be no current flowing in it, and the output voltage from the offset is equal to the offset voltage, 3 mV.

As a result, the AC source can supply up to:

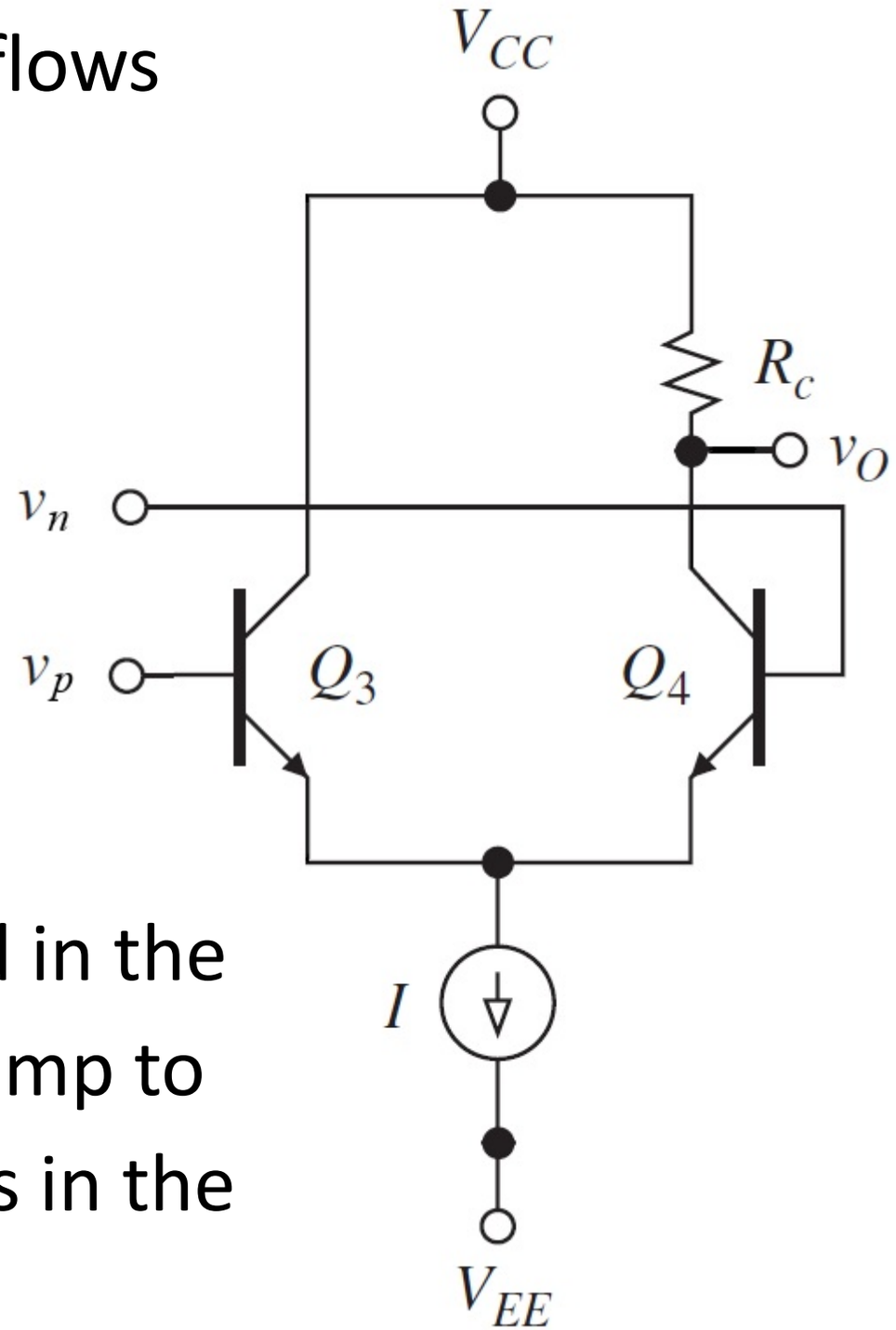
$$V_O'(\max) = V_O(\max) - V_{OS}$$

$$= 13\ \text{V} - 3\ \text{mV} = 12.997\ \text{V}$$

This is effectively 13 V on the output, which corresponds to ≈13 mV on the input. It is okay if input source is an AC signal only.

Input Bias Currents

- Op amp golden rule: no current flows into inputs.
- But, in practice we have:
  - i_{IN} ~ µA for BJTs.
  - i_{IN} ~ 10 pA for FETs.
  - i_{IN} ~ 1 pA for CMOS.



- This is due to DC currents needed in the amplifier's input pins for the op amp to operate (cf. parasitic capacitances in the device) i.e. input bias current.

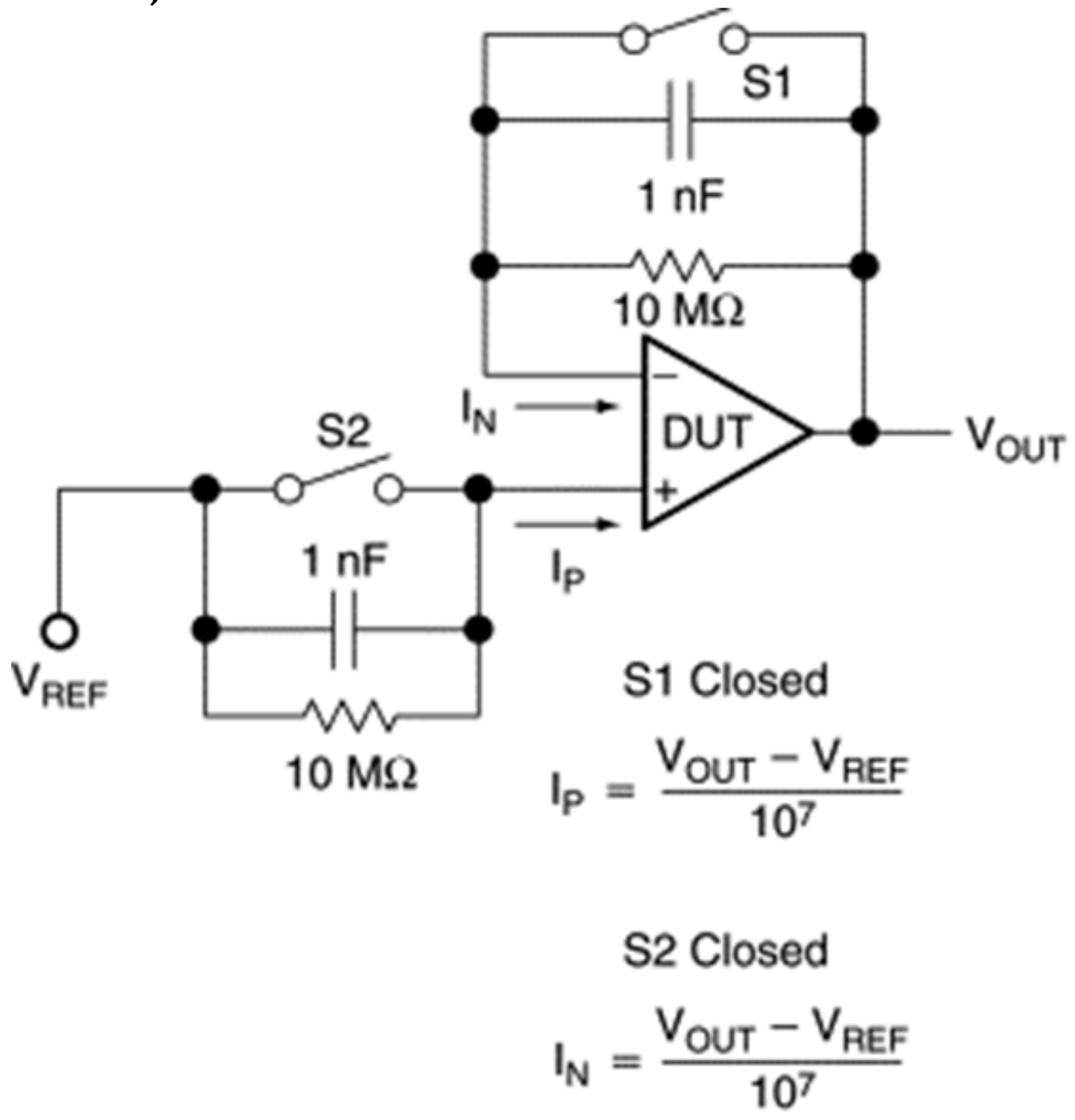
Measure Input-Bias and Offset Currents

- Generally current in the non-inverting input ($I_{N,N}$) is not equal to inverting input ($I_{N,P}$) i.e. input offset current.
- Measured through experimental circuit.
- Bias current:

$$I_B = \frac{(I_N + I_P)}{2}$$

- Offset current:

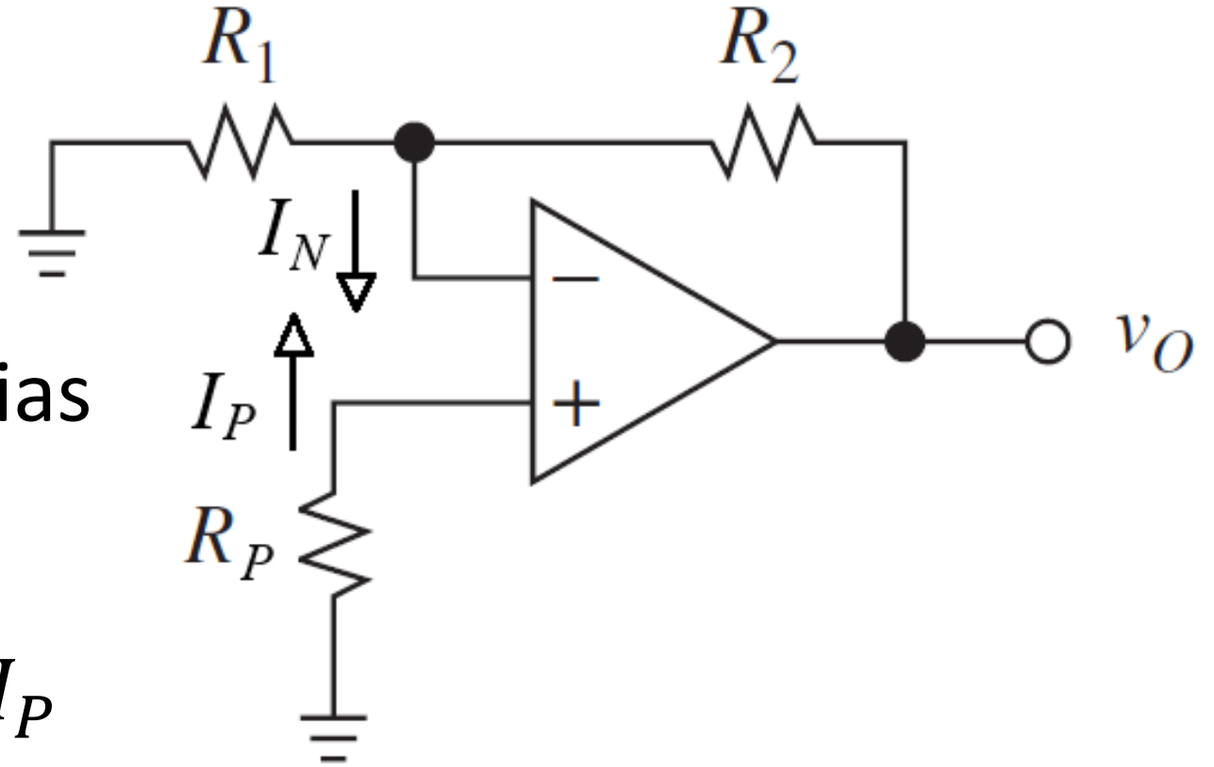
$$I_{OS} = (I_N - I_P)$$



Errors Caused by I_B

- For a given non-inverting amplifier (with bias current):

$$V_O = \left(1 + \frac{R_2}{R_1}\right) V_P + R_2 I_N$$



- When $V_p = -R_p I_p$, for both bias and offset currents:

$$V_O = R_2 I_N - \left(1 + \frac{R_2}{R_1}\right) R_P I_P$$

- Making $(1 + R_2/R_1)$ for inverting and non-inverting parts:

$$V_O = \left(1 + \frac{R_2}{R_1}\right)\left[\left(\frac{R_2}{1 + R_2/R_1}\right) I_N - R_P I_P\right]$$

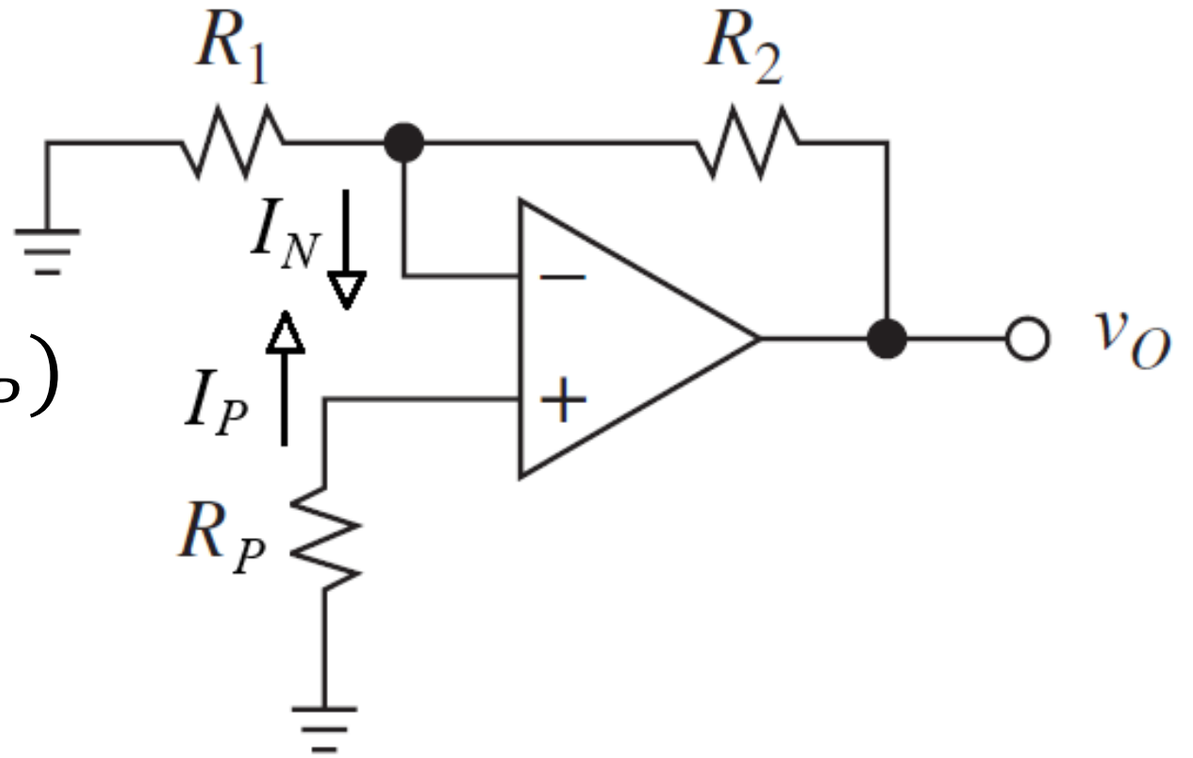
$$= \left(1 + \frac{R_2}{R_1}\right)\left[(R_1 \parallel R_2) I_N - R_P I_P\right]$$

Minimising I_B Errors of Amplifier

- We can minimise error due to I_B by setting resistor $R_P = R_1 \parallel R_2$.

$$V_o = \left(1 + \frac{R_2}{R_1}\right)(R_P I_N - R_P I_P)$$

$$= \left(1 + \frac{R_2}{R_1}\right) R_P I_{OS}$$

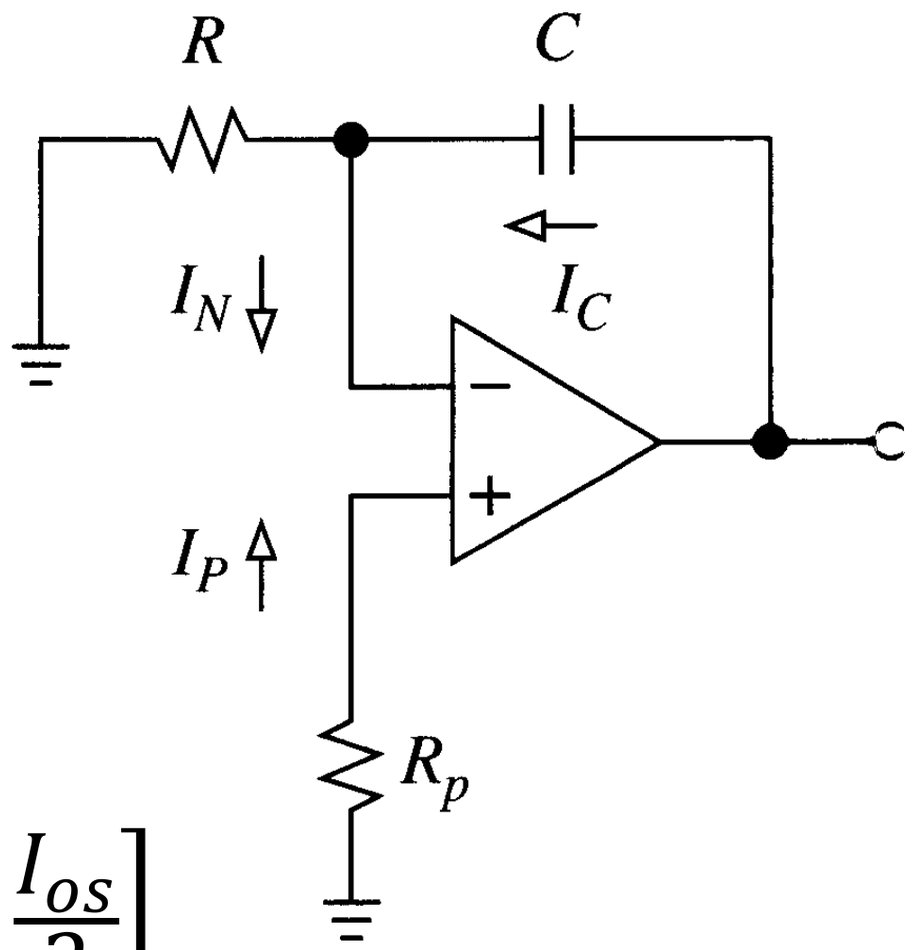


- This leaves the equation with offset current only.
- Similarly, reducing R_1, R_2, and R_P will reduce the offset current error.

Minimising I_B Errors of Integrator

- Integrator circuit:

$$V_o = \frac{1}{RC}\int_o^t V_{in}dt$$



- Assuming constant I_B and I_{OS} :

$$V_o = \left[\frac{(R - R_P)I_B - (R + R_P)\frac{I_{os}}{2}}{RC}\right]t$$

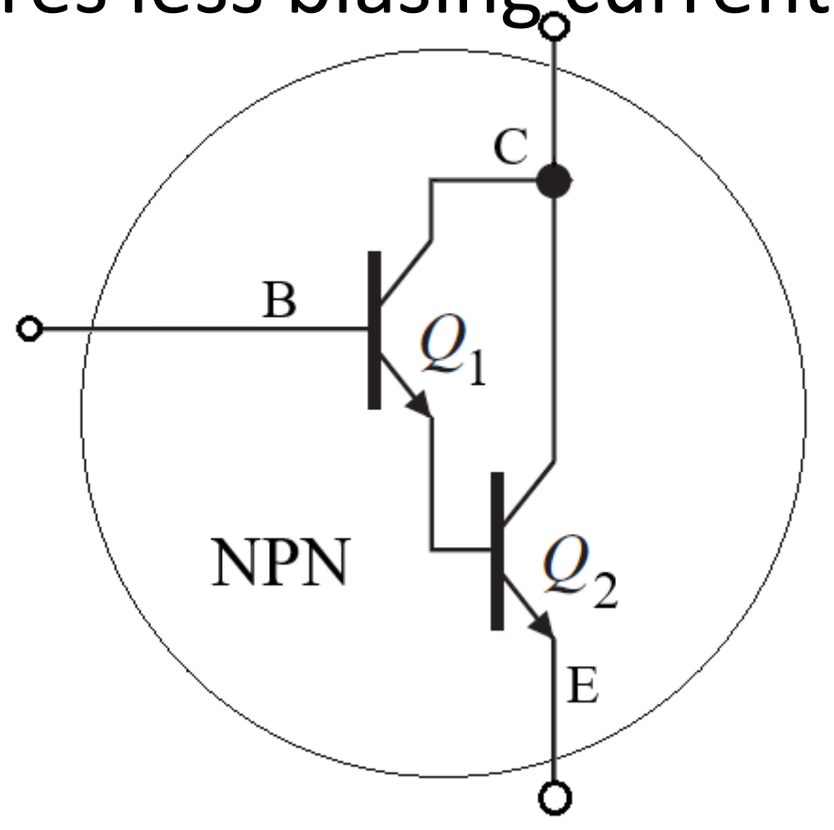
- Minimise bias current error with $R_p = R$, we have only offset current error – reduced with large C.

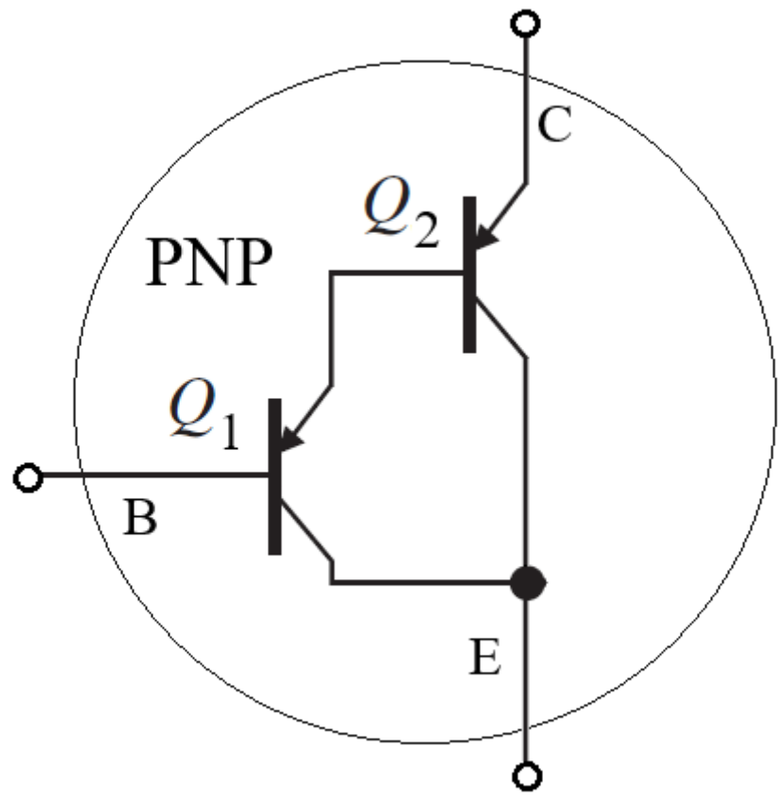
$$V_o = -\left(\frac{RI_{os}}{RC}\right)t = -\left(\frac{I_{os}}{C}\right)t$$

Avoiding I_B Problems

Super beta BJTs:

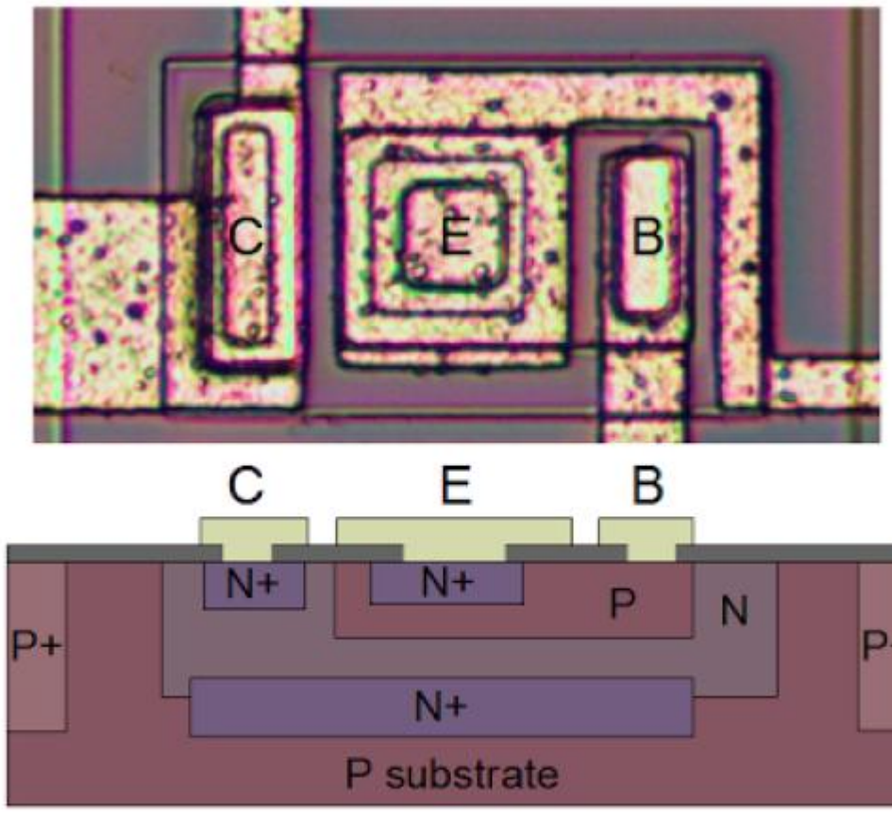
- A super-beta transistor is a single BJT made with a very narrow base region, e.g. LM108 op amp.
- It has very high β ($\sim 10^4$) and provides high-input impedance and ultra-low input bias currents for high-speed applications.
- Minimising I_B as it has a very narrow base structure, so it requires less biasing current.





Avoiding I_B Problems

- Super beta BJT is very similar to arrangement of Darlington pair transistor (e.g. two separate transistors).



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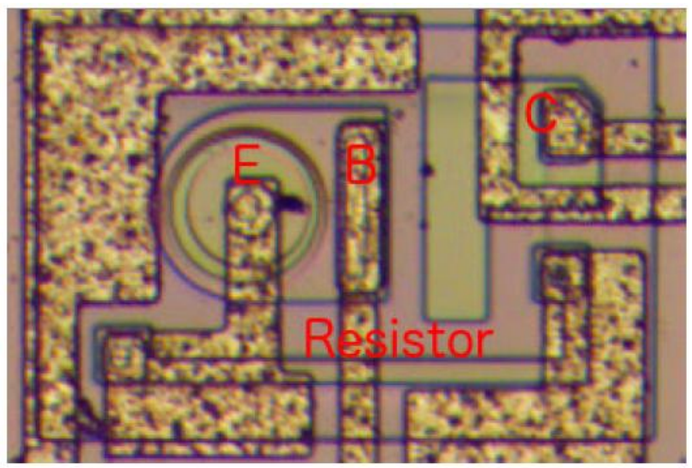


LM108 (10x magnification)

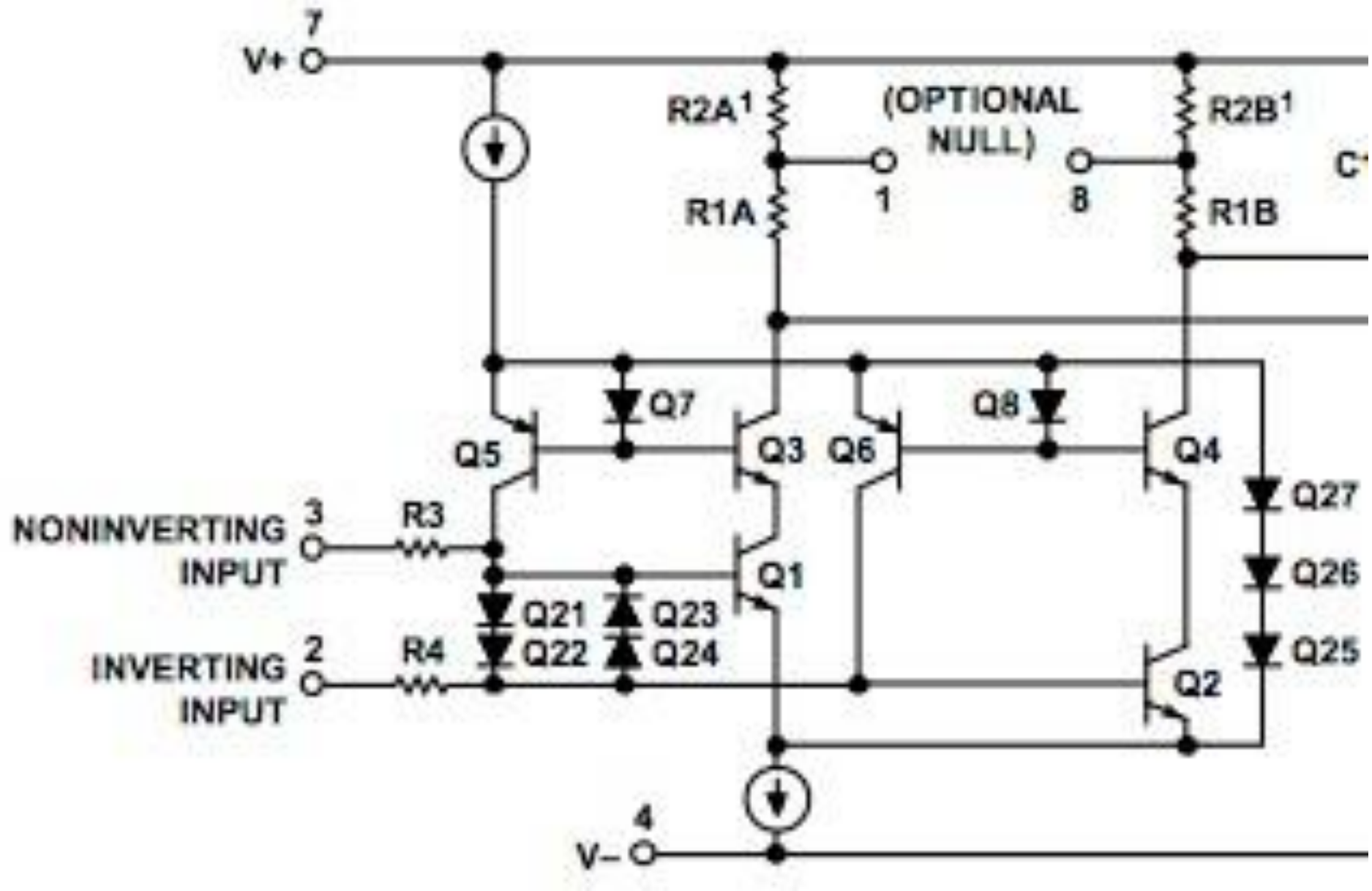
Avoiding I_B Problems

Input bias cancellation:

- "Estimate" required bias currents and supply internally – reduces i_{IN}.
- Minimising I_B by providing internal biasing current compensation network.
  - For example, see the input stage section of OP77.

Avoiding I_B Problems

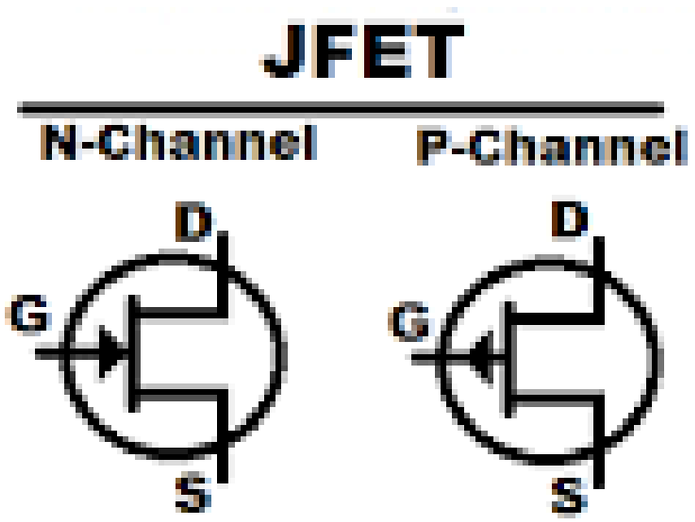
- Input stage section of OP77 has a network of diodes which are implemented in the device for providing the required internal biasing current.

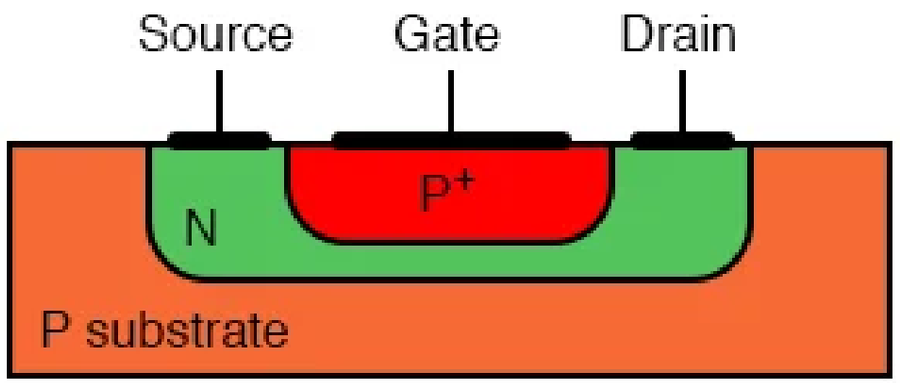


Avoiding I_B Problems

JFET-input op amps:

- Input current (i_{IN}) is reverse current through a PN junction, (cf. i_{BASE} for BJT).
- But biasing current is still needed for controlling the width of the N or P channel.
- e.g. OPA827.

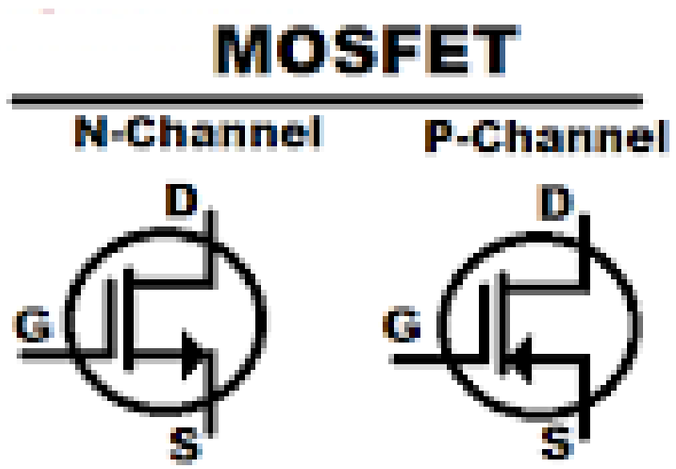


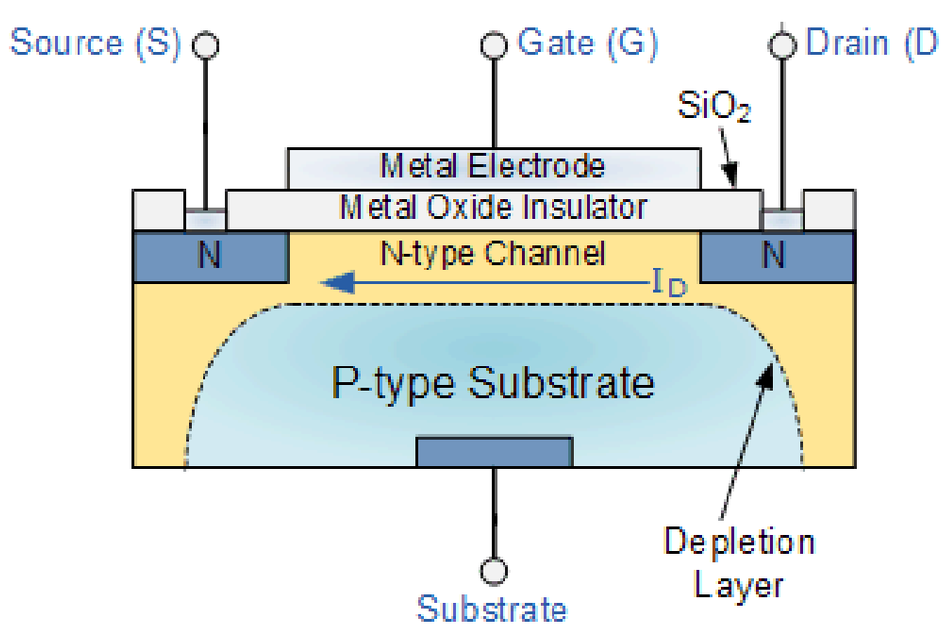


Avoiding I_B Problems

MOSFET op amps:

- It has even lower i_{IN} than JFET.
- Relatively higher impedance due to insulator layer i.e. smaller bias current.
- Further enhanced in the Bi(C)MOS with dual depletion channels i.e. small bias offset.



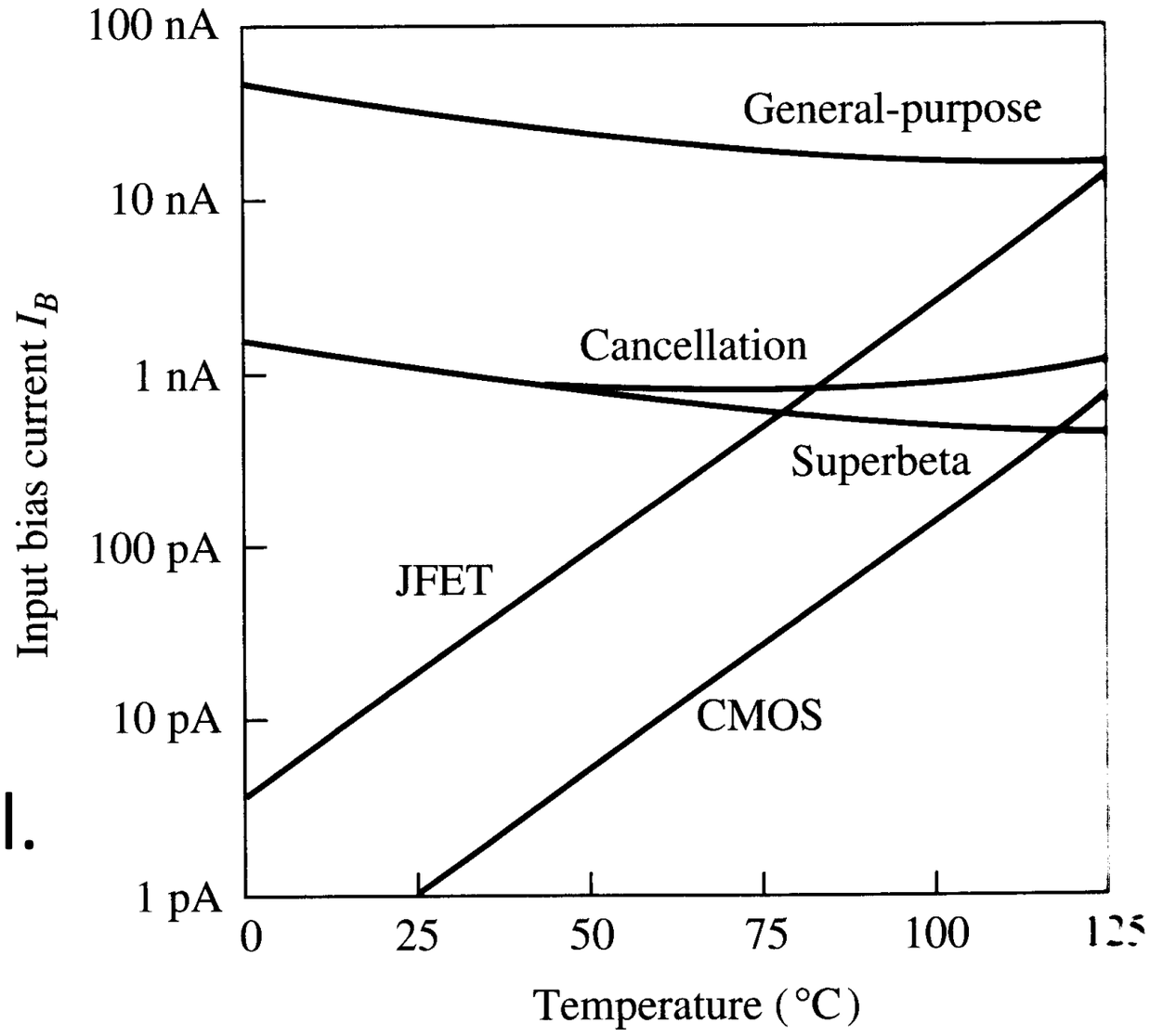


Temperature Dependence of I_B

- Input bias (I_B) is very temperature dependent in the FET:

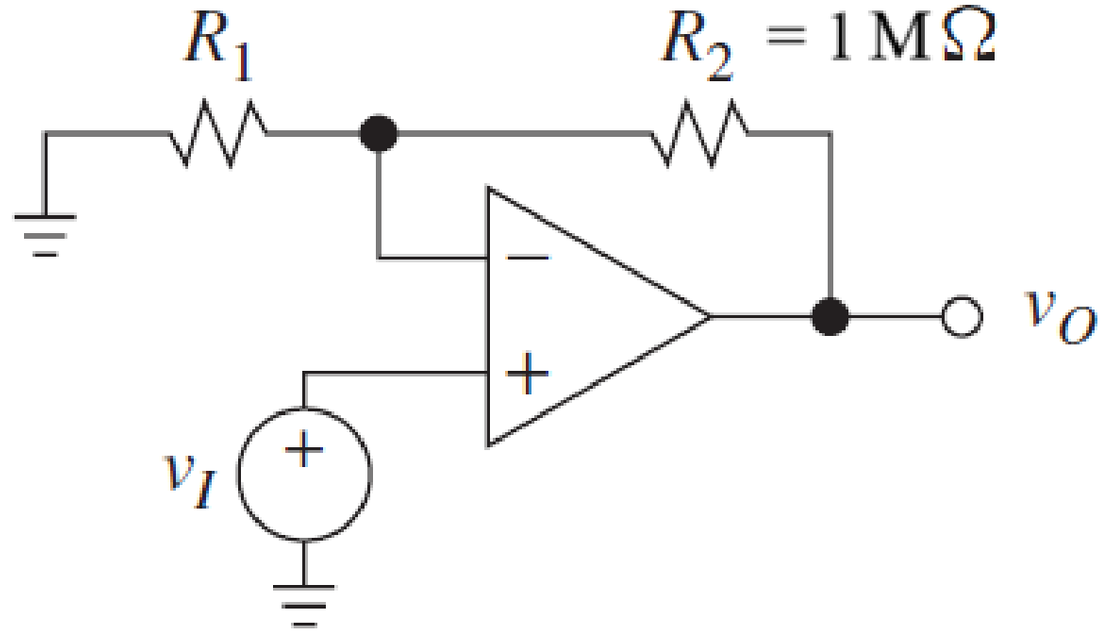
$$I_B(T) \approx I_B(T_0)2^{(T-T_0)10}$$

- I_B ~ doubles for temperature + 10° C.
- So, need to keep the FET cool.



Example of Bias Current I_B

An op amp is connected in a closed loop with gain of +100 utilising a feedback resistor of 1 MΩ.



a. If the input bias current is 100 nA, what output voltage results with the input grounded? [4 marks]

b. If the input offset voltage is ±1 mV and the input bias current as in (a), what is the largest possible output that can be observed with the input grounded? [2 marks]

Example of Bias Current I_B

c. If the bias-current compensation is used, what is the value of the required resistor? If the offset current is no more than one-tenth the bias current, what is the resulting output offset voltage (due to offset current alone)? [4 marks]

d. With the bias-current compensation as in (c) in place what is the largest DC voltage at the output due to the combined effect of offset voltage and offset current? [2 marks]

Example of Bias Current I_B

Solution

a. This is a non-inverting amplifier circuit.

$$A_v = \frac{R_1 + R_2}{R_1} = 100 \qquad \text{thus} \qquad R_2 = 99R_1$$

Since the feedback resistor is R_2 = 1 MΩ, the resistor to ground must be:

$$R_1 = \frac{R_2}{99} = \frac{10^6}{99} = 10.1\ \text{k}\Omega$$

If the input source is grounded, then the inverting input is also at ground and thus all the bias current flows through the feedback resistor, resulting in output voltage:

$$v_o = I_B R_2 = (100\times10^{-9})(1)(10^6) = 0.1\ \text{V}$$

Example of Bias Current I_B

b. With offset voltage, E_o of ± 1 mV, we expect an output:

$$v_o' = A_v E_o = 100 \times (\pm\, 1\ \text{mV}) = \pm\, 0.1\ \text{V}$$

Thus, the maximum output is $v_0 + v_o' = 0.1 + 0.1 = 0.2$ V.

c. The bias compensating resistor, R_B, should be equal to the ground resistor, R_1, thus R_B = 10.1 kΩ. This gives rise to a voltage drop which causes exactly the bias current to flow through R_1, no current through R_2, and zero output voltage. If the offset current is one tenth of the bias current, then the resulting output voltage is one tenth of the output voltage when considering only bias current without compensation, except that it can be either positive or negative, v_o = $\pm$ 0.01 V

Example of Bias Current I_B

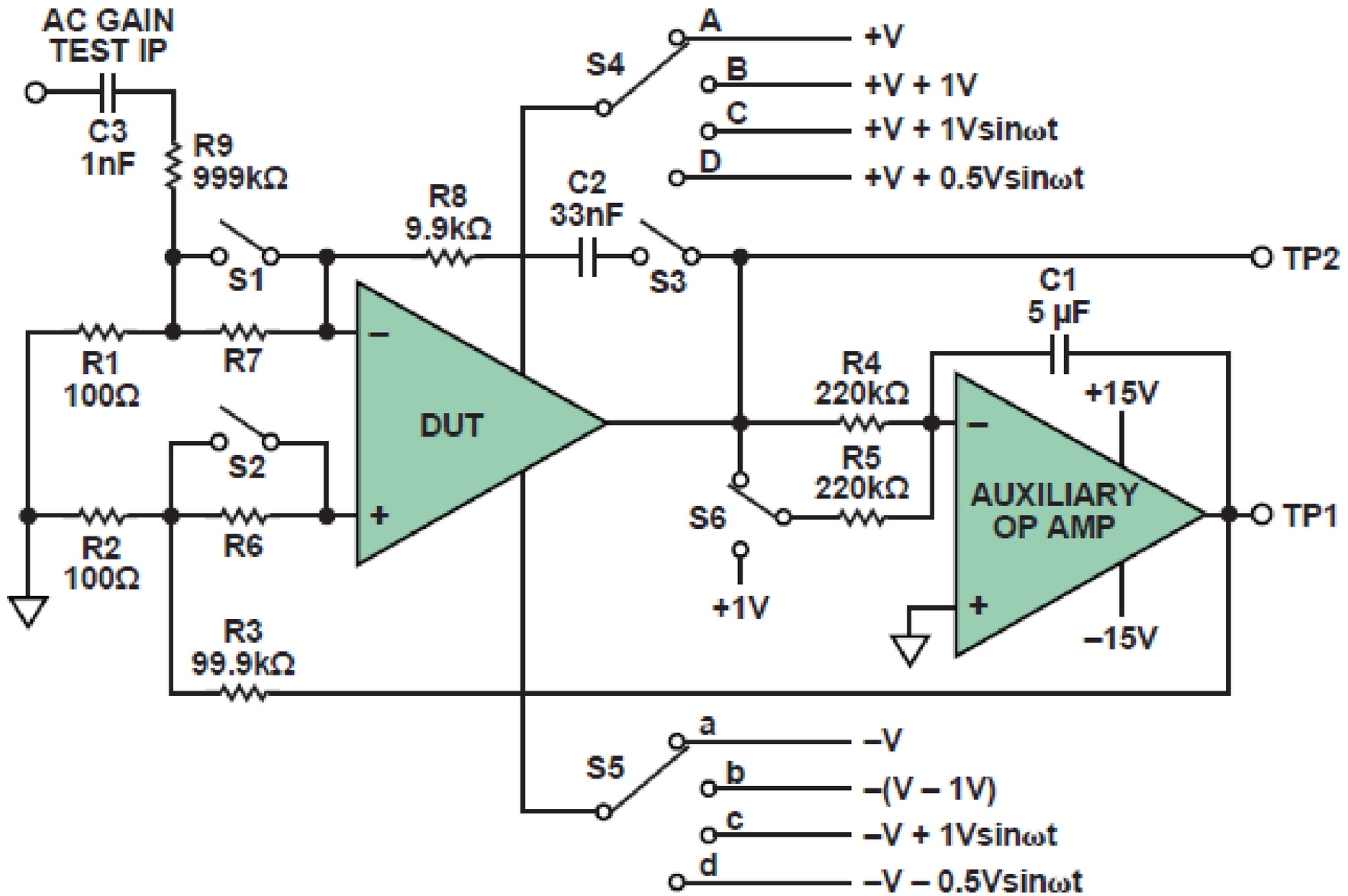
d. The value of the output due to offset voltage is 0.1 V with either sign. The value of output due to offset current is 0.01 V with either sign. The largest value of the combined output is 0.11 V, either positive or negative.

Nulling

- Nulling: number of ways to remove DC (static) errors affecting op amps.
- Methods for performing nulling:
  - Use op amp's built-in offset null circuitry.
  - Add external nulling circuit (e.g. external and block nulling circuits).
  - Use a better op amp.
- Static errors are not static: they drift with time and temperature.

Experimental Circuit for Nulling

- Set up an experimental circuit for nulling process.
- Measuring offset voltage, bias and offset currents, gain, CMRR, PSRR, etc.



Experimental Circuit for Nulling

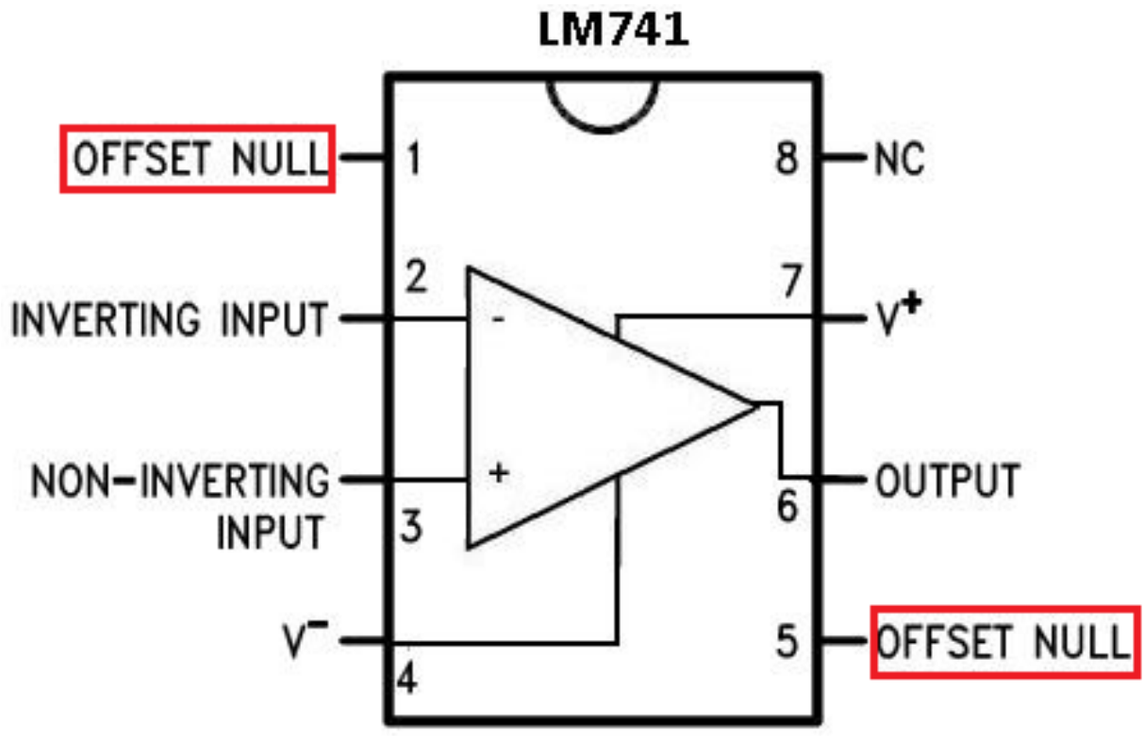
- Mode of operation of the set up depends on arrangement of switches ($S_1 - S_6$)

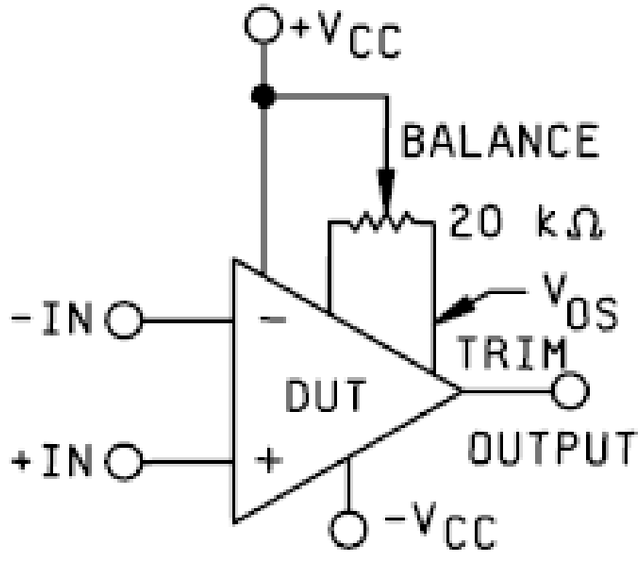
No	**Measurement**	S_1	S_2	S_3	S_4	S_5	S_6
1	Voltage offset	1	1	0	A	a	0
2	Offset and bias current	0/1	0/1	0	A	a	0
3	DC gain	1	1	0	A	a	0/1
4	AC gain	1	1	0	A	A	0
5	DC CMRR	1	1	0	A/B	a/b	0
6	DC PSRR	1	1	0	A/B	a/b	0
7	AC CMRR	1	1	1	C	c	0
8	AC PSRR	1	1	1	D	d	0

Internal Nulling

Many op amps have extra input pins to adjust offsets:

- These deliberately unbalance the input stage to counteract manufacturing imperfections.
- No standard for external circuit required to interface with internal null circuitry.
- Not available for bi- and quad-packages.

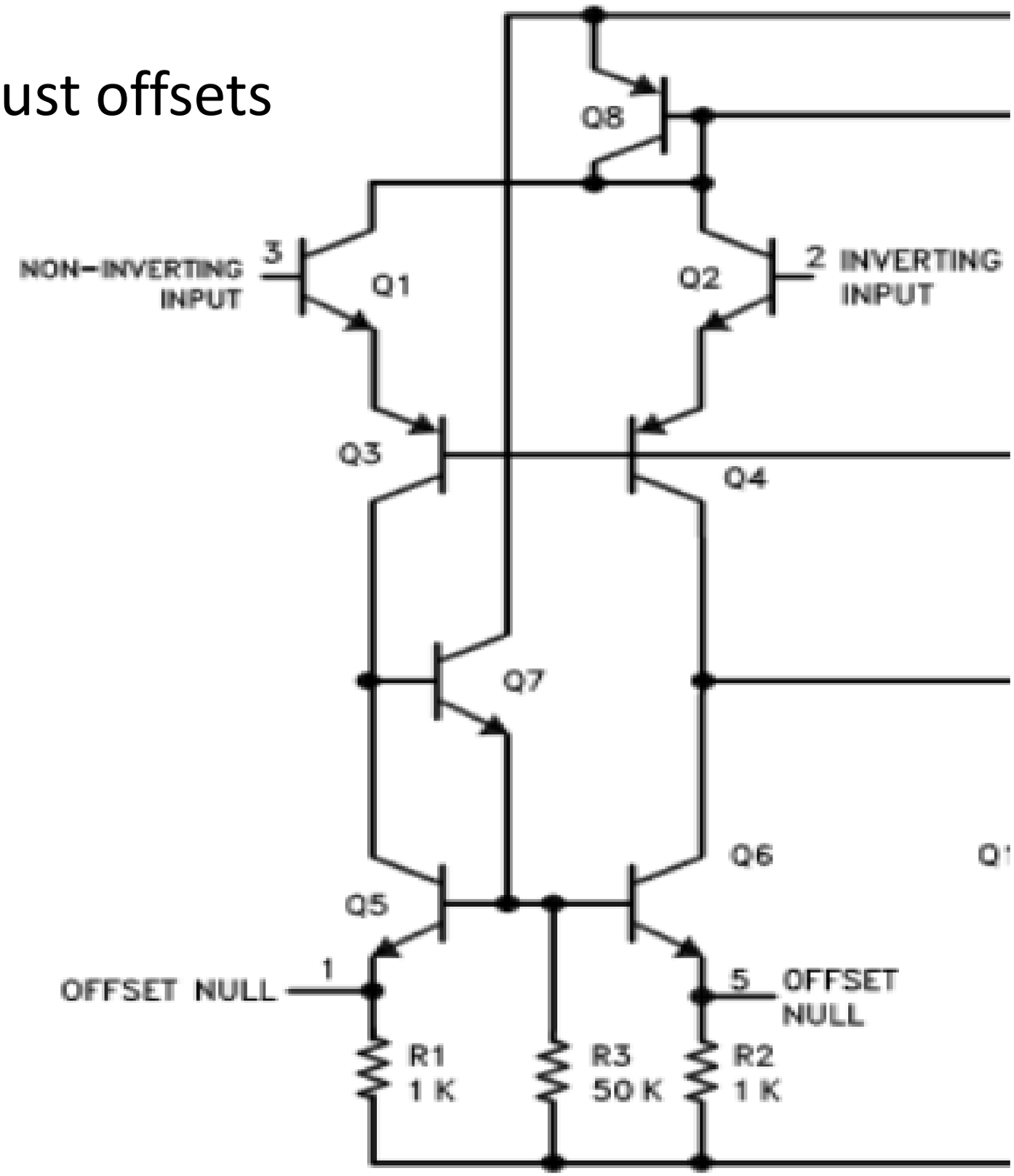




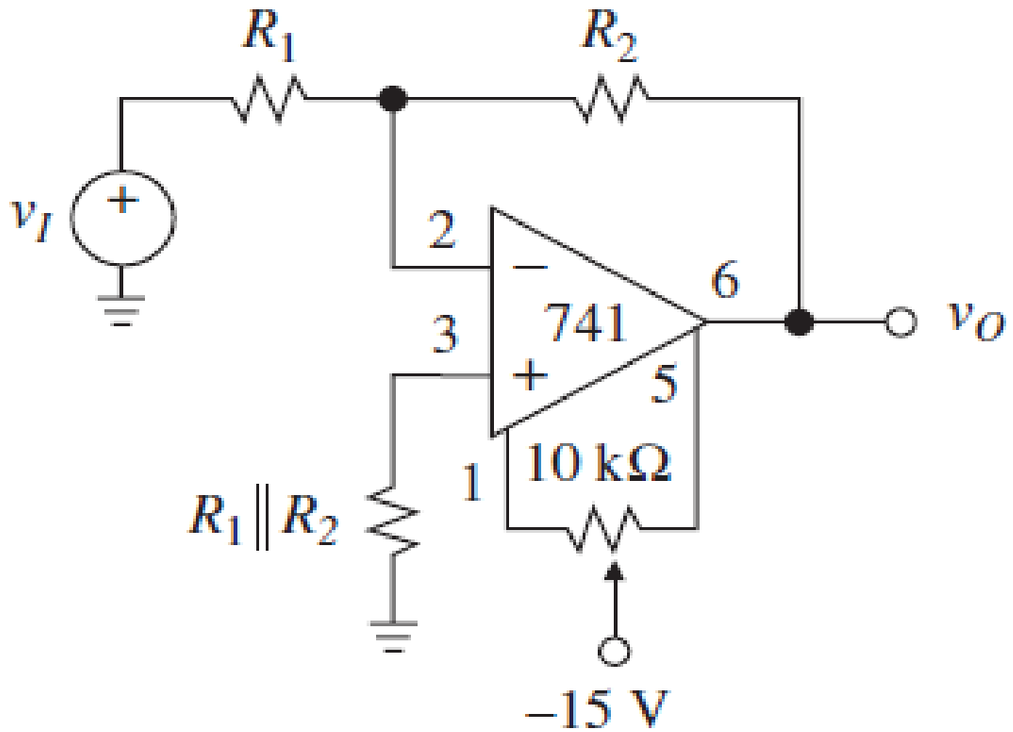
Internal Nulling

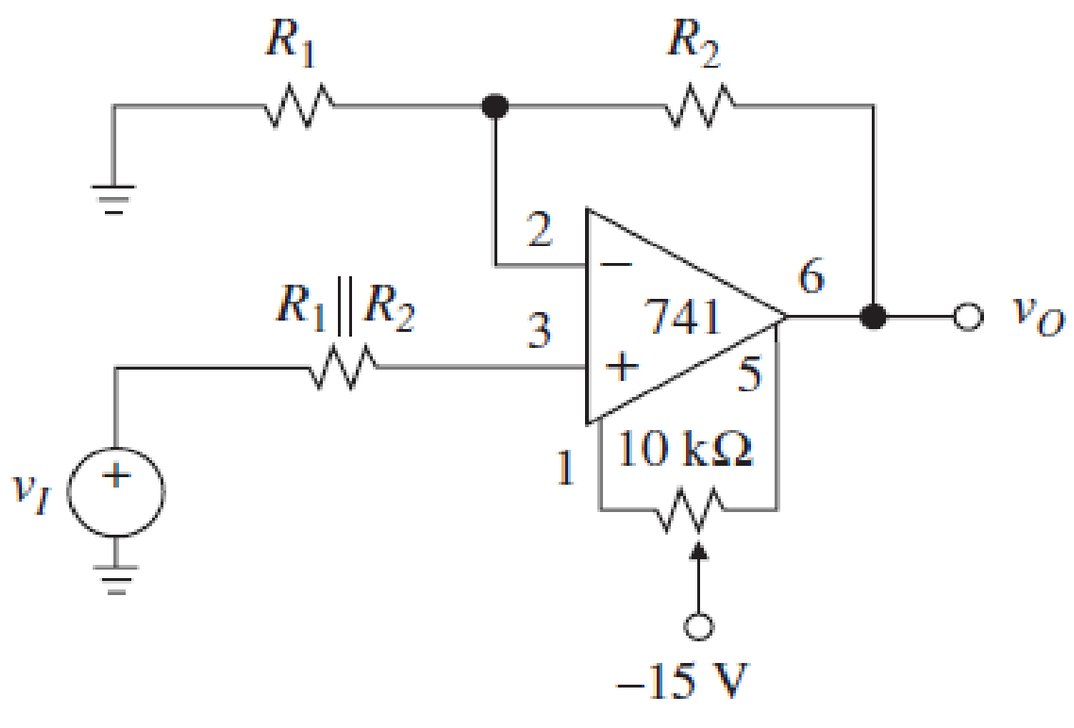
Extra input pins to adjust offsets inside the op amp:

- Located at the current mirror in the differential input stage of the op amp.
- Offset null pins to balance imperfections.



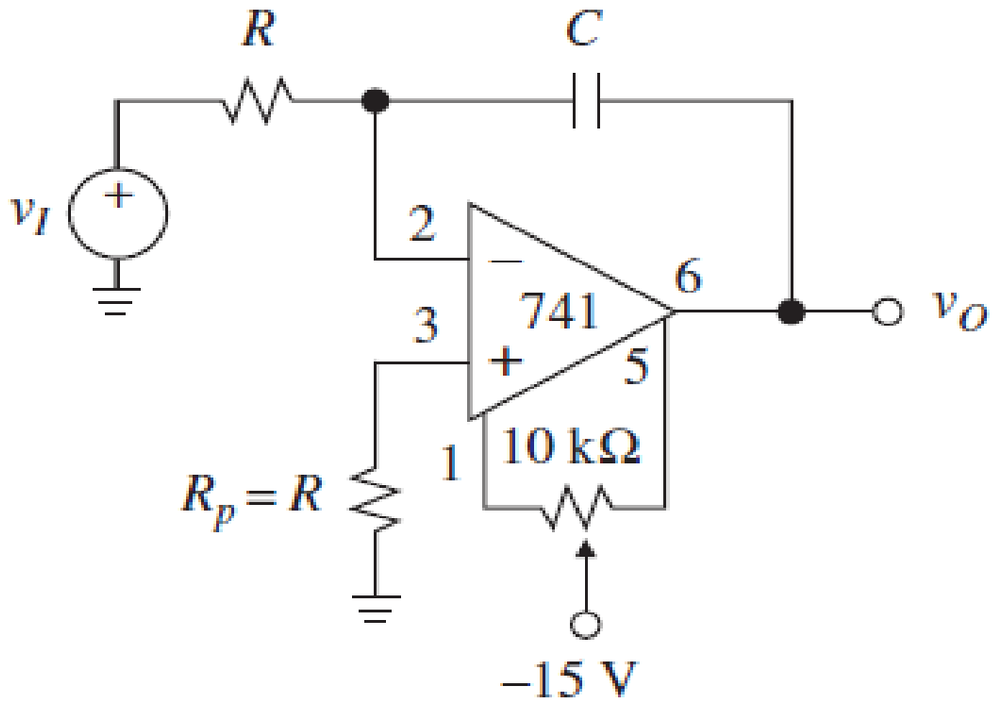
Internal Nulling





Internal nulling scheme:

- Inverting and non-inverting amplifiers with internal offset-error nulling (top).
- Integrator with internal offset-error nulling (bottom).

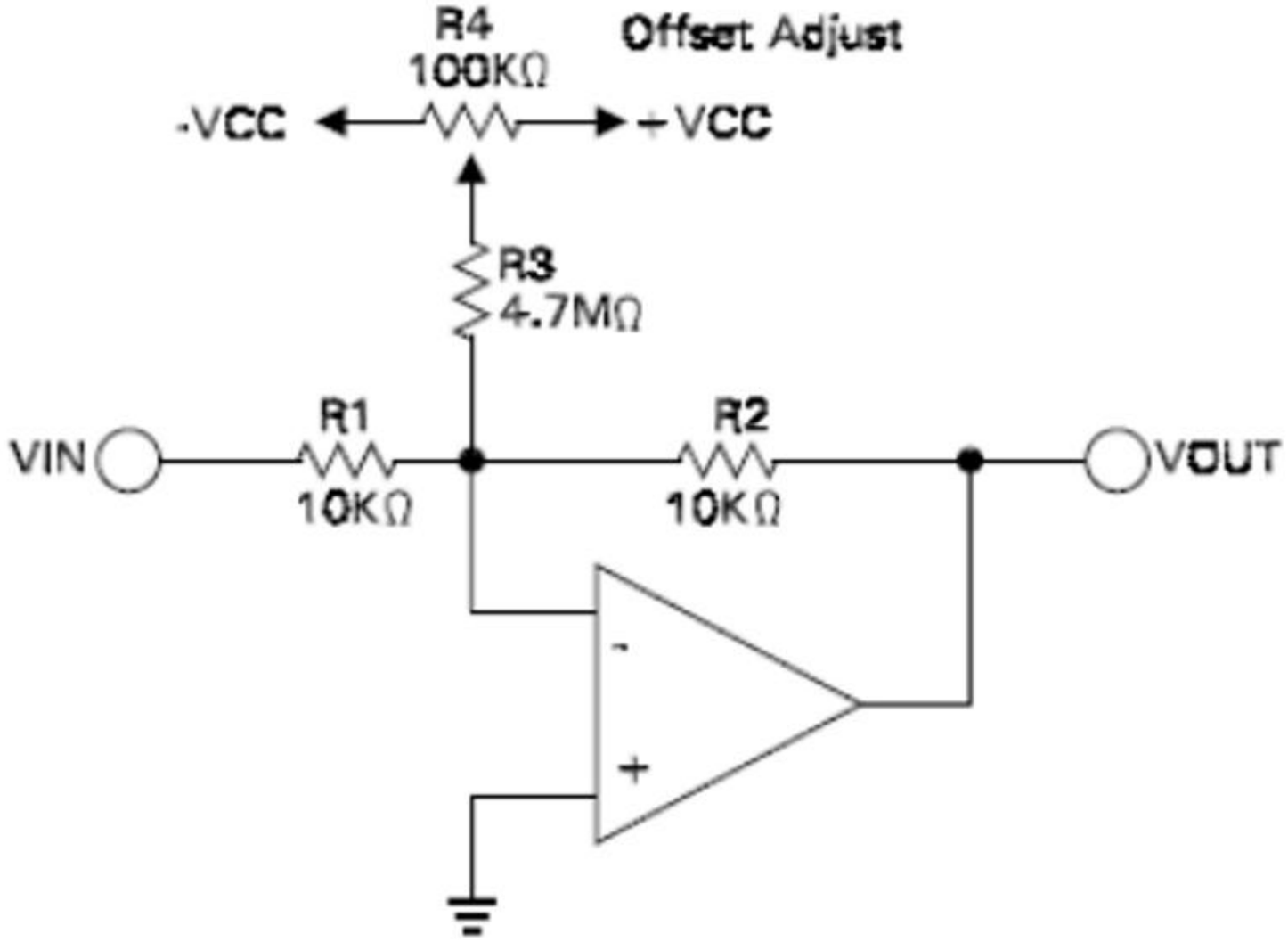


External Nulling

- External null circuits are for amplifiers with no internal nulling circuitry.
- Very similar to internal nulling i.e. use of the balance pins and a potentiometer to the supply rail.
- But external nulling is used for balancing and calibrating the functionality and operation of the circuit.
- Input offset may be nulled to optimize performance of the amplifiers.

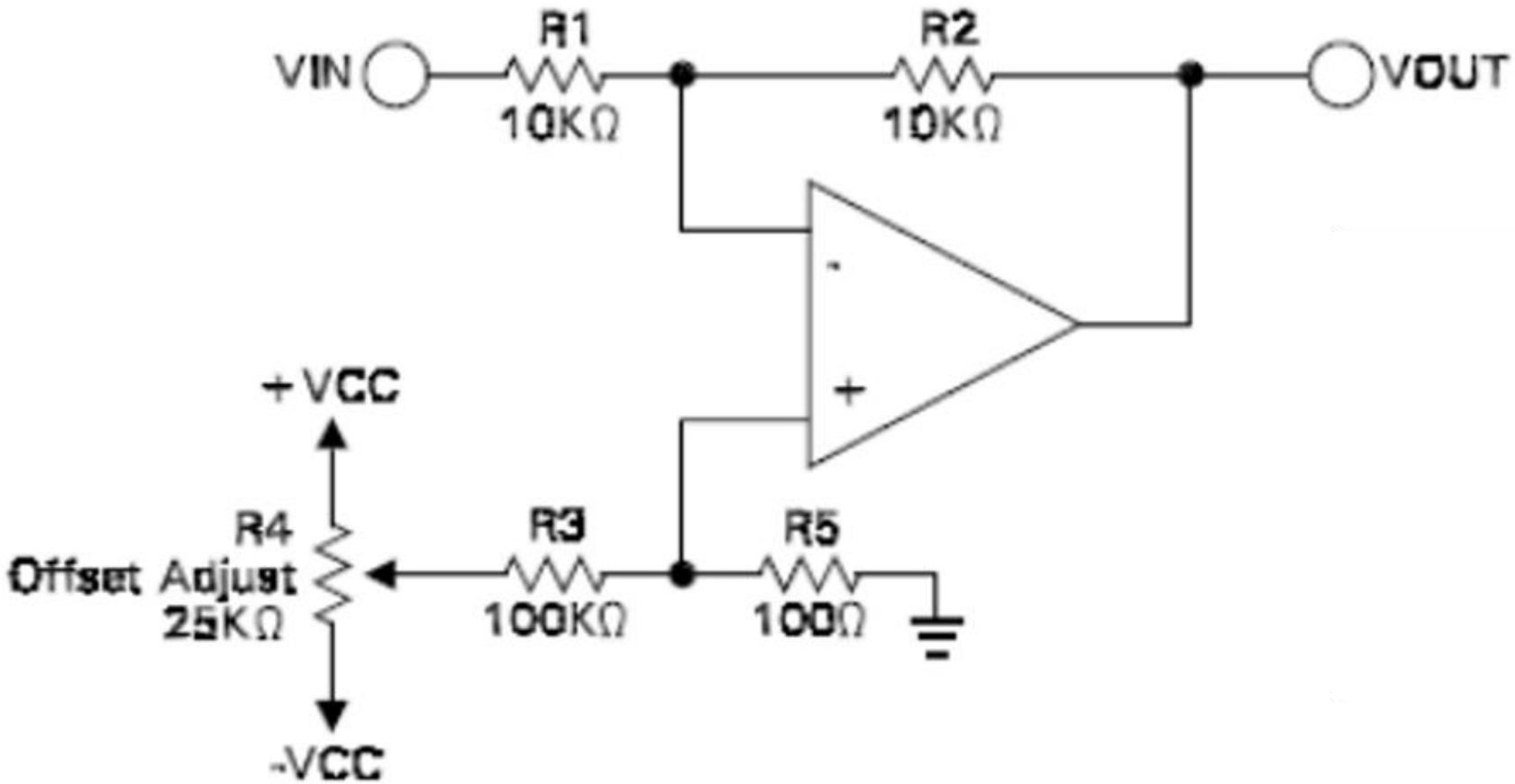
External Nulling

- External offset null adjust for an inverting amplifier.
- Offset voltage applied to the inverting input.
- Offset adjustment range = $\pm V_{CC}(R_1 \parallel R_2)/R_3$.



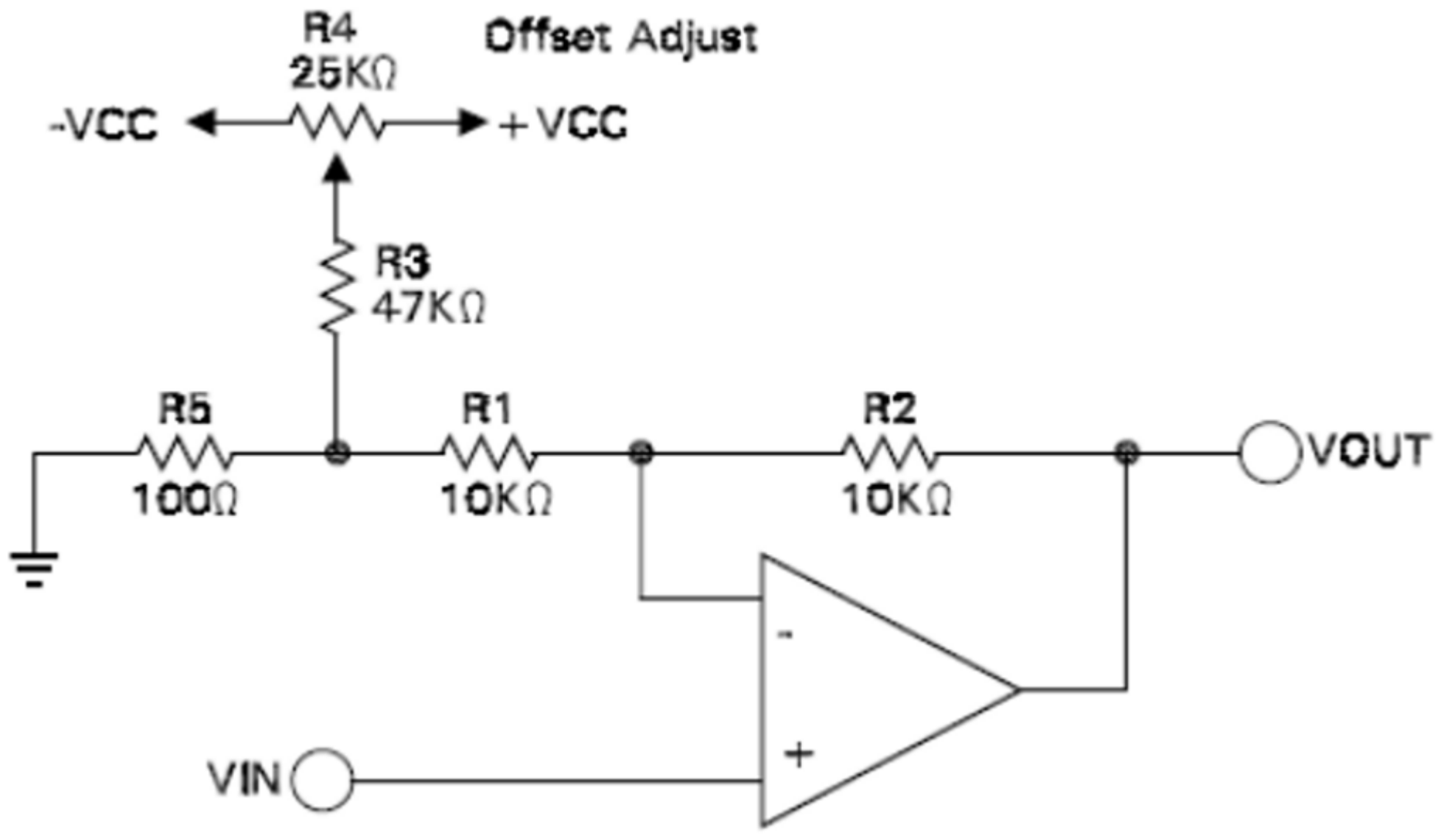
External Nulling

- External offset null adjust for a noninverting amplifier.
- Offset voltage applied to the noninverting input.
- Offset adjustment range = $\pm V_{CC}(R_5/R_3)$.



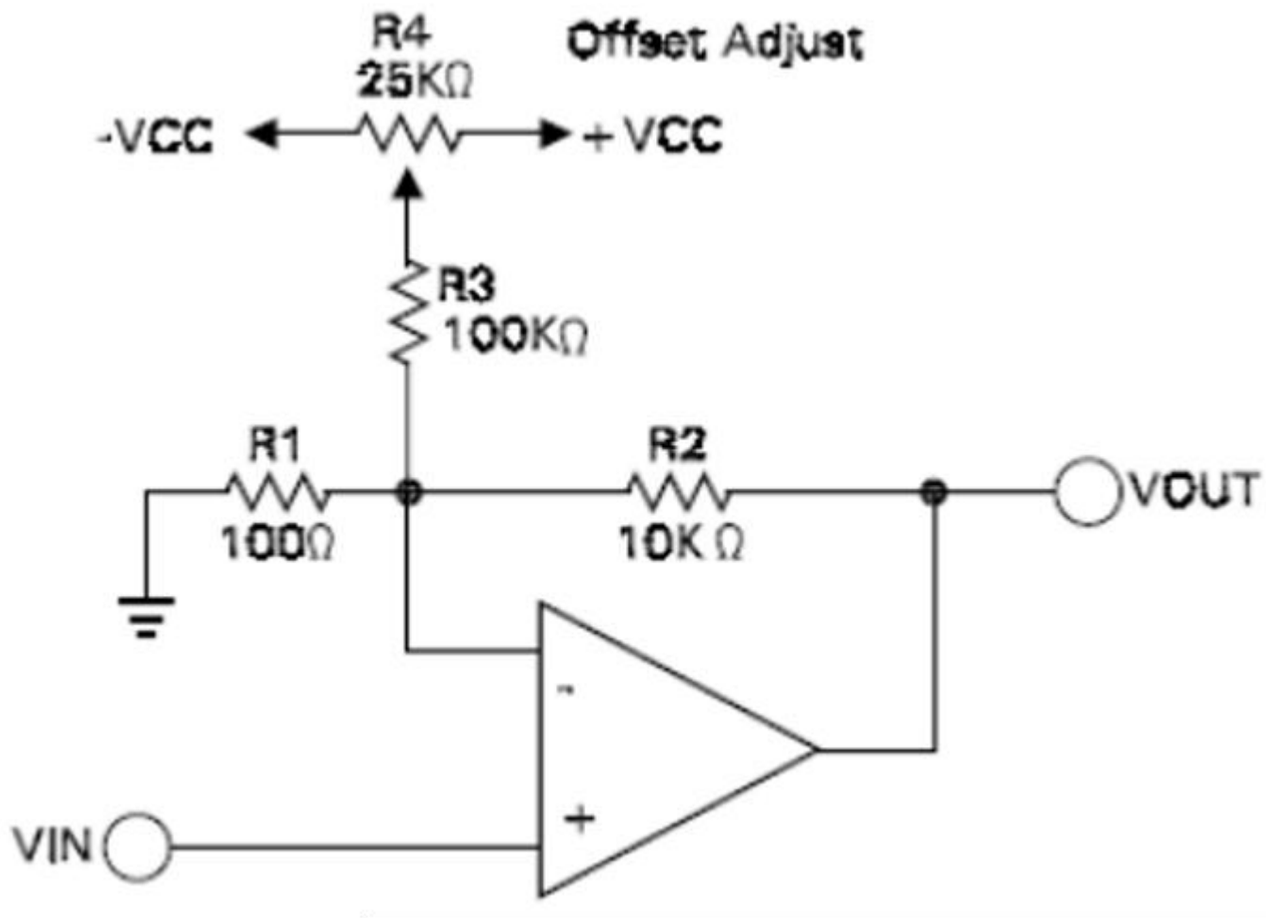
External Nulling

- External offset null adjust for a low-gain noninverting amplifier.
- Offset adjustment range = $\pm V_{CC}(R_5/R_3)\big(R_2/(R_1+R_2)\big)$.\
- Precision gain of stage modified by presence of R_5 in series with R_1: $A_V = (R_5 + R_1 + R_2)(R_5 + R_1)$.
- Disregarding $R_3 \parallel R_5$, since $R_3 \gg R_5$



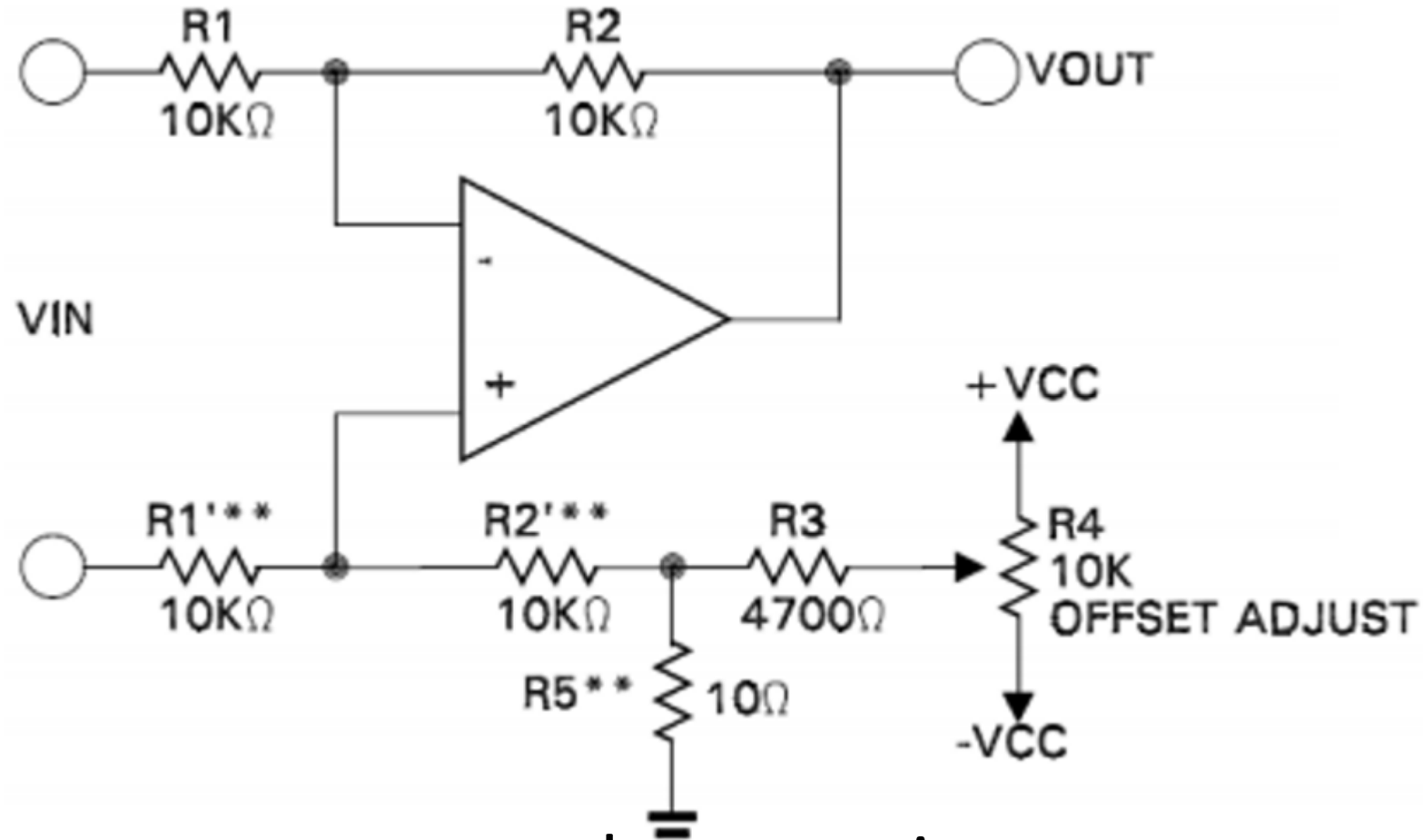
External Nulling

- External offset null adjust for a high-gain noninverting amplifier.
- Offset adjustment range = $\pm V_{CC}(R_1/R_3)$.



External Nulling

- External offset null adjust for a differential amplifier.
- Offset adjustment range = $\pm V_{CC}(R_5/R_3)\left(R'/(R_1' + R_2')\right)$.



- R_5 introduces a common-mode error, since:

$$R_2/R_1 = (R_2' + R_5)/R_1'$$

- If necessary, trim R_2' such that $R_2/R_1 = (R_2' + R_5)/R_1'$.

Block-Level Nulling

Multiple parameters nulling (block-level nulling):

- Use a single adjustable point to null entire block.
- Be careful with high-gain stages, integrators, etc.
- Competing goals and cancelling out effects.
- Simple tune-in procedure i.e. avoiding nulling objective conflict(s).
- Only a few op amp-based circuits could have block-level nulling (e.g. specific applications and multiple nulling objectives).

Block-Level Nulling

Instrumentation amplifier circuit:

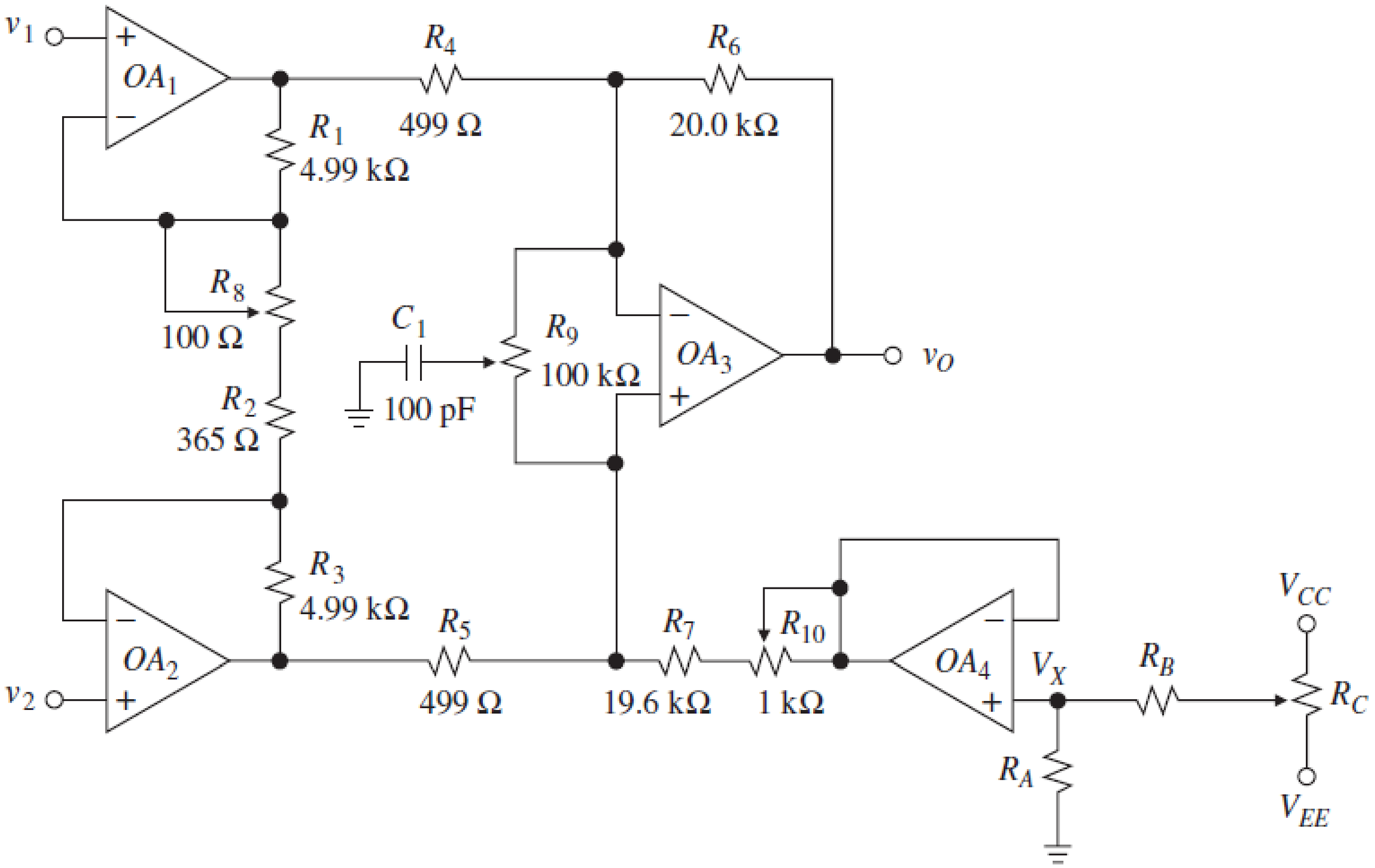
- Multiple op amp-based amplifiers to form an instrumentation amplifier.
- Voltage followers or buffer amplifiers at inputs.
- Differential amplifier.

Block-level nulling circuits:

- Gain adjustment of the amplifier circuit via R_g resistor.
- Input offset nulling circuit with external circuitry.

Block-Level Nulling

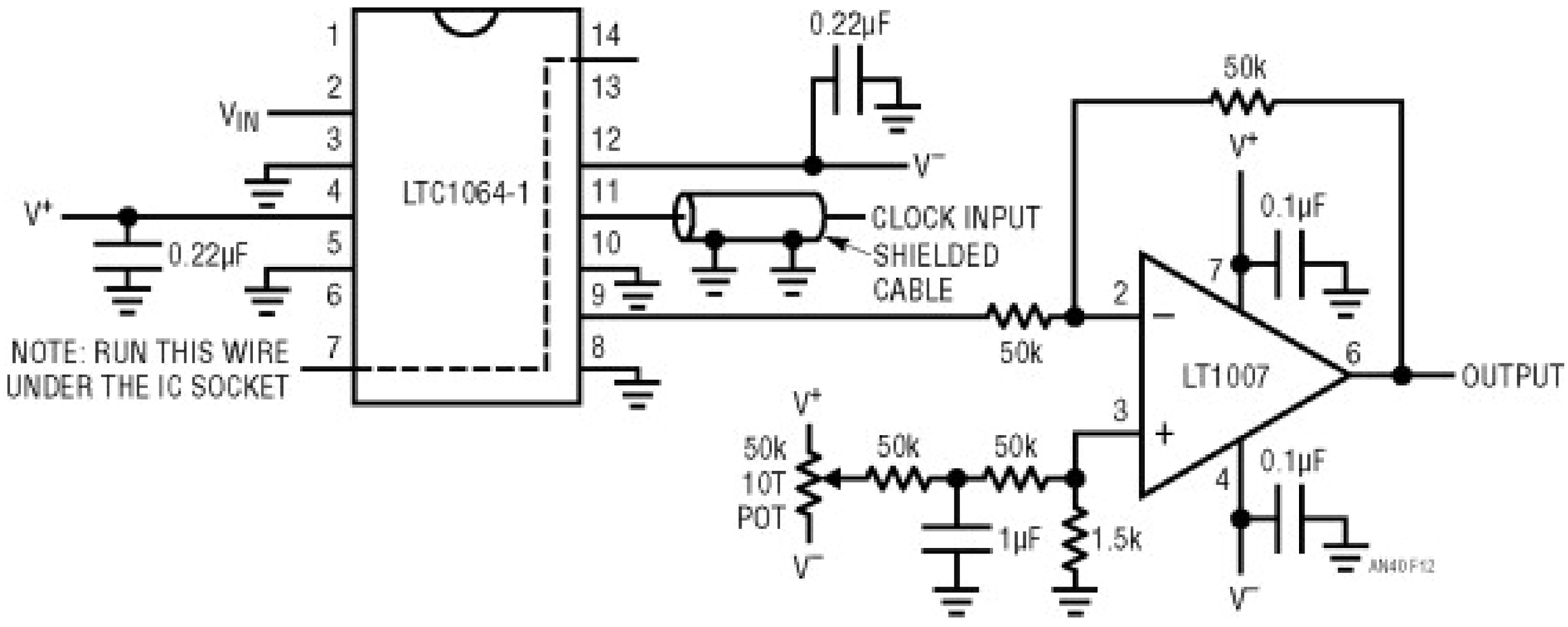
- Block level offset null and gain adjustment of an instrumentation amplifier:



Block-Level Nulling

Precision elliptic low-pass filter circuit:

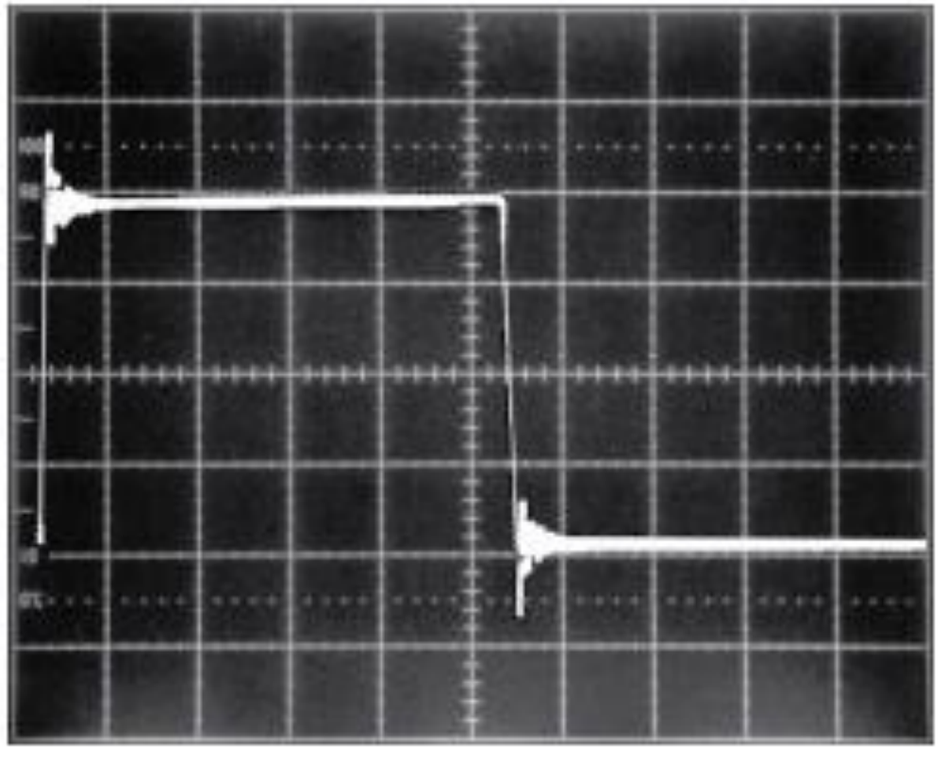
- Low noise 8th order, clock sweep able, low-pass elliptic antialiasing LTC1064-1.
- LT1007 low-noise, high-speed precision op amp.



Block-Level Nulling

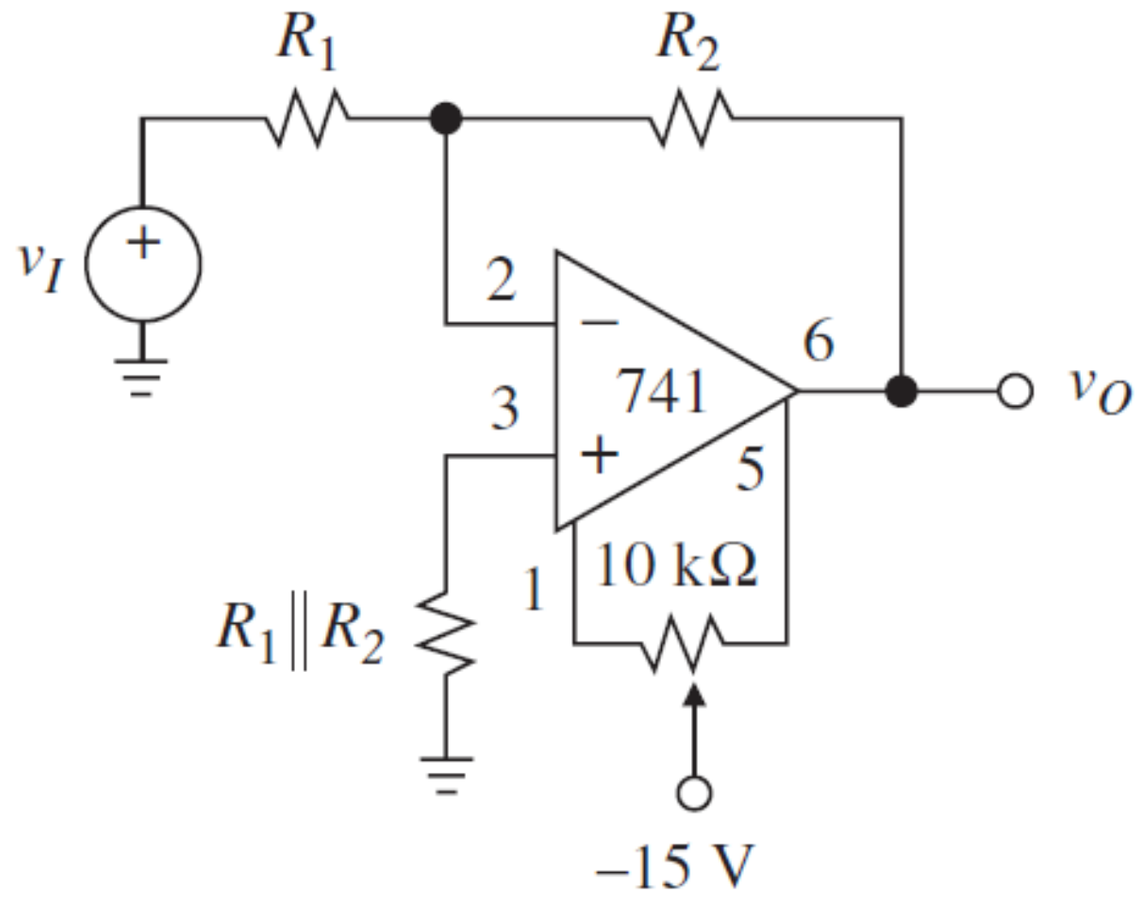
Block-level nulling circuit:

- Correct the offset at 25°C, but not the offset at other temperatures.
- Advantage is that it affect very little the filter's frequency response.
- The time domain response of the filter circuitry.
- The rising and falling edge overshoot is typical of high Q-factor filters i.e. switched capacitor or active RC.



Example 1 of Nulling

A 741C op amp is to be used in the circuit of the figure below to yield voltage gain, $A_v = -10$.



If $V_{os}(\max)$ = 6 mV and $I_{os}(\max)$ = 200 nA, specify suitable resistances that will maximise the input resistance R_i of the circuit. [10 marks]

Example 1 of Nulling

Solution

Since $R_i = R_1$, we need to maximise R_1.

As A_v = -10, impose $R_2 = 10R_1$ and say that $E_o \leq 15$ mV, if $V_{OS}(\max) + (R_1 \parallel R_2) I_{OS}(\max) \leq 15$ mV, we get:

$$R_1 \parallel R_2 \leq \frac{15\ \text{mV} - 6\ \text{mV}}{200\ \text{nA}} = 45\ \text{k}\Omega$$

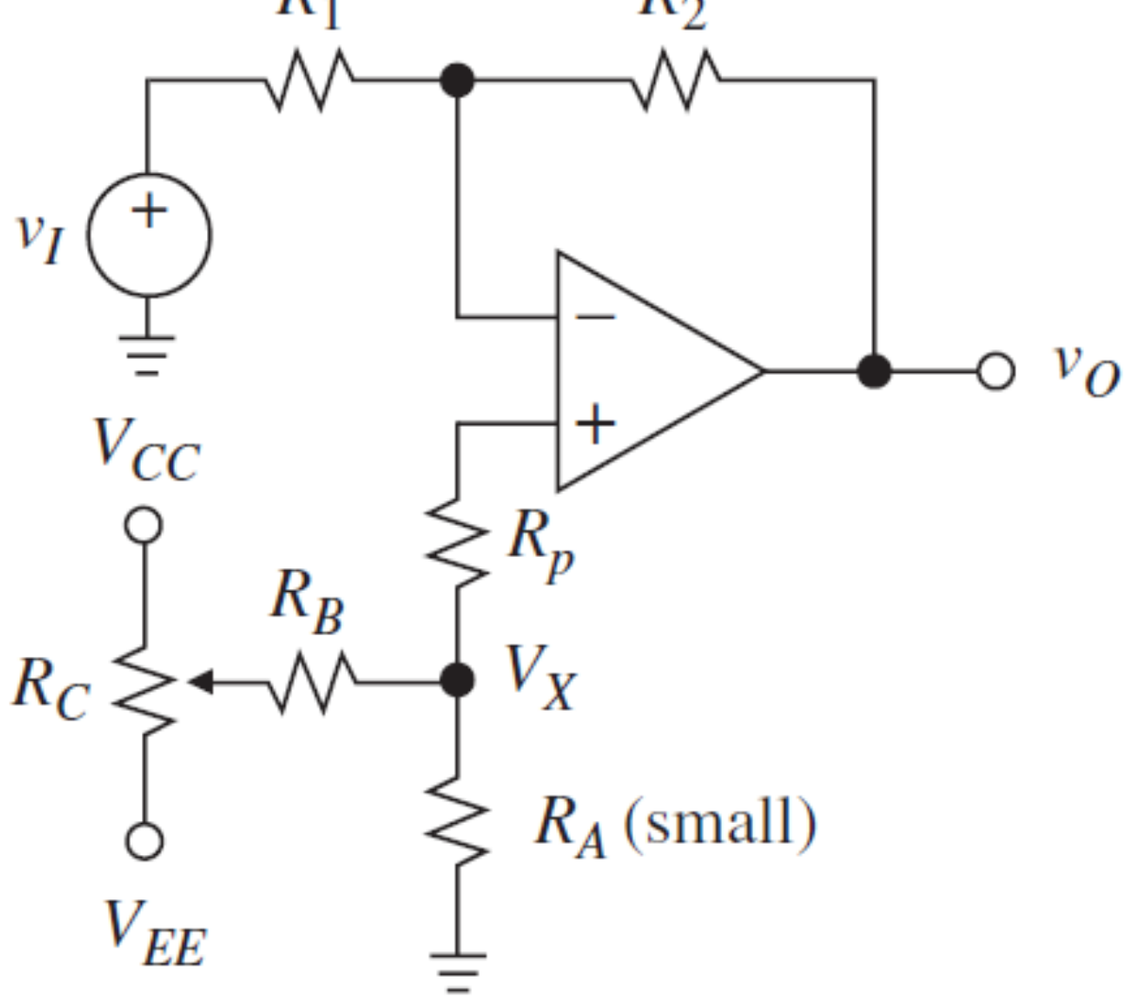
Or

$$\frac{1}{R_1} + \frac{1}{10R_1} \geq \frac{1}{45\ \text{k}\Omega}$$

Solving yields $R_1 \leq 49.5\ \text{k}\Omega$. Use the standard values R_1 = 47 kΩ, R_2 = 470 kΩ, and R_p = 43 kΩ.

Example 2 of Nulling

A 741C op amp is to be used in the circuit given in the figure below to yield A_v = −5 and R_i = 30 kΩ. Specify suitable resistances. Consider $V_{os}(\max)$ = 6 mV and $I_{os}(\max)$ = 200 nA [12 marks]

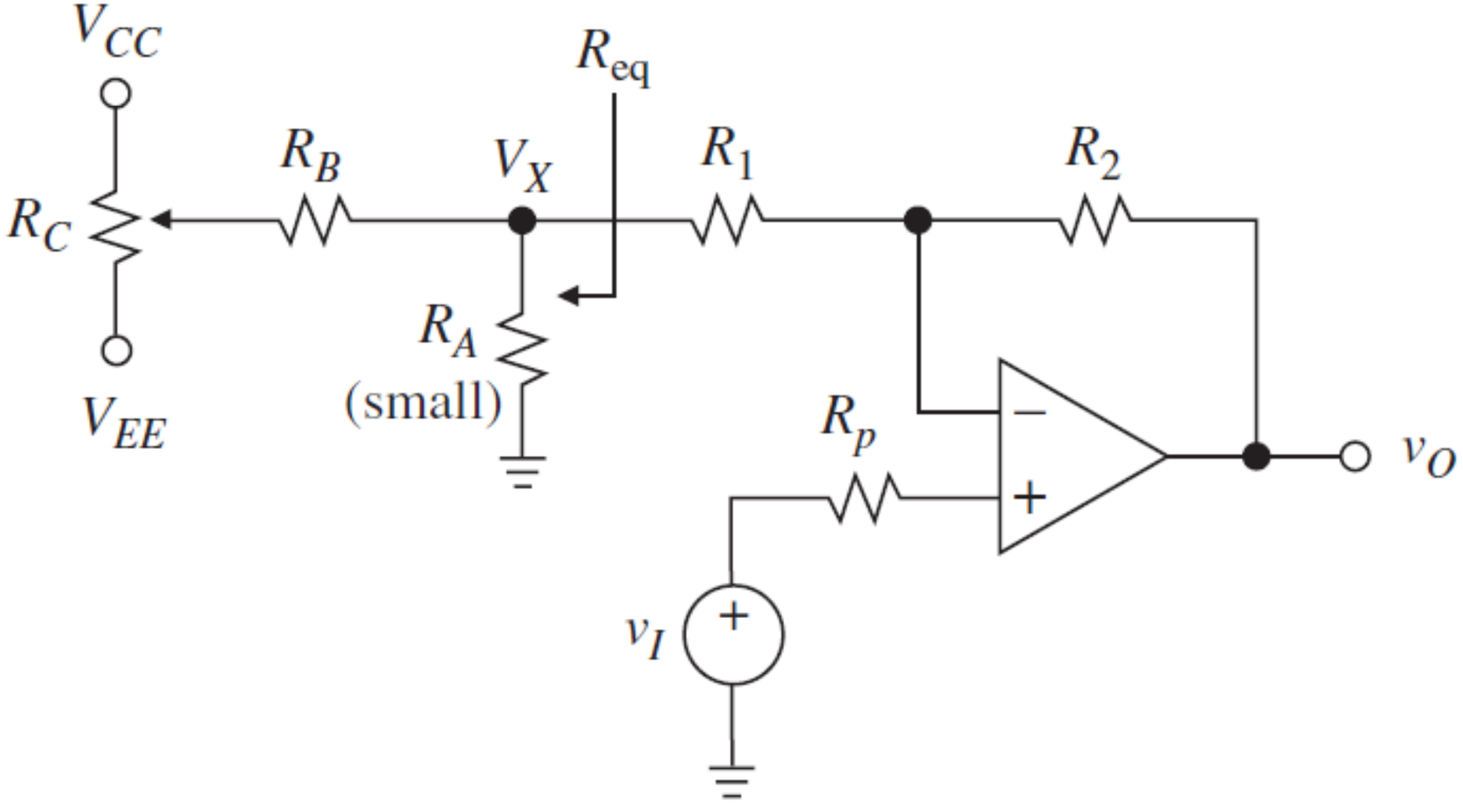


Example 3 of Nulling

Assuming a 741C op amp with $V_{os}(\max)$ = 6 mV and $I_{os}(\max)$ = 200 nA in the figure below, specify suitable resistances for:

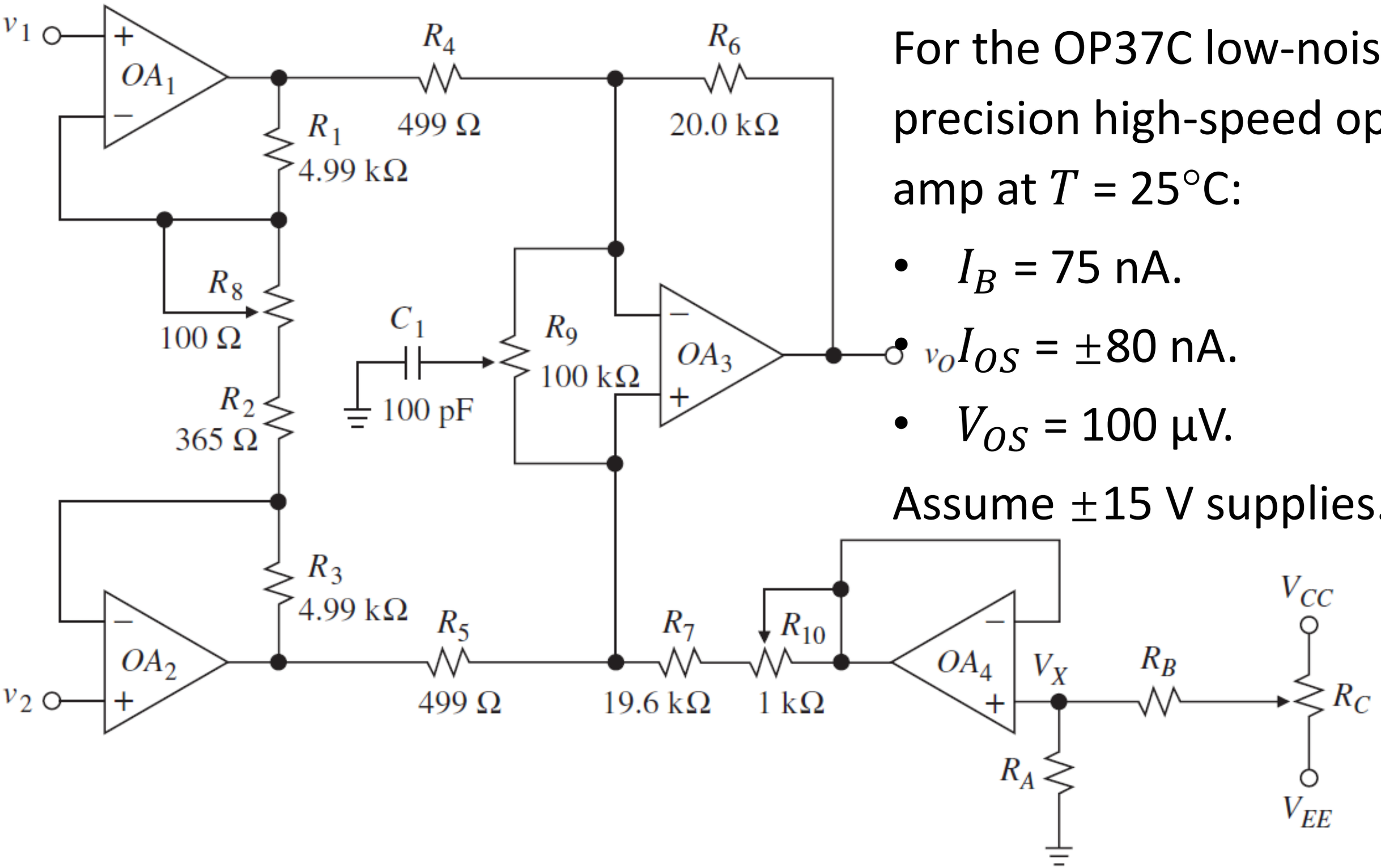
a. The gain A_v = 5. [16 marks]

b. The gain A_v = 100. [16 marks]



Example 4 of Nulling

Specify R_A, R_B, and R_C in the figure below. [10 marks]



For the OP37C low-noise precision high-speed op amp at T = 25°C:

- I_B = 75 nA.
- $v_O I_{OS}$ = ±80 nA.
- V_{OS} = 100 μV.

Assume ±15 V supplies.

Monte Carlo Analysis

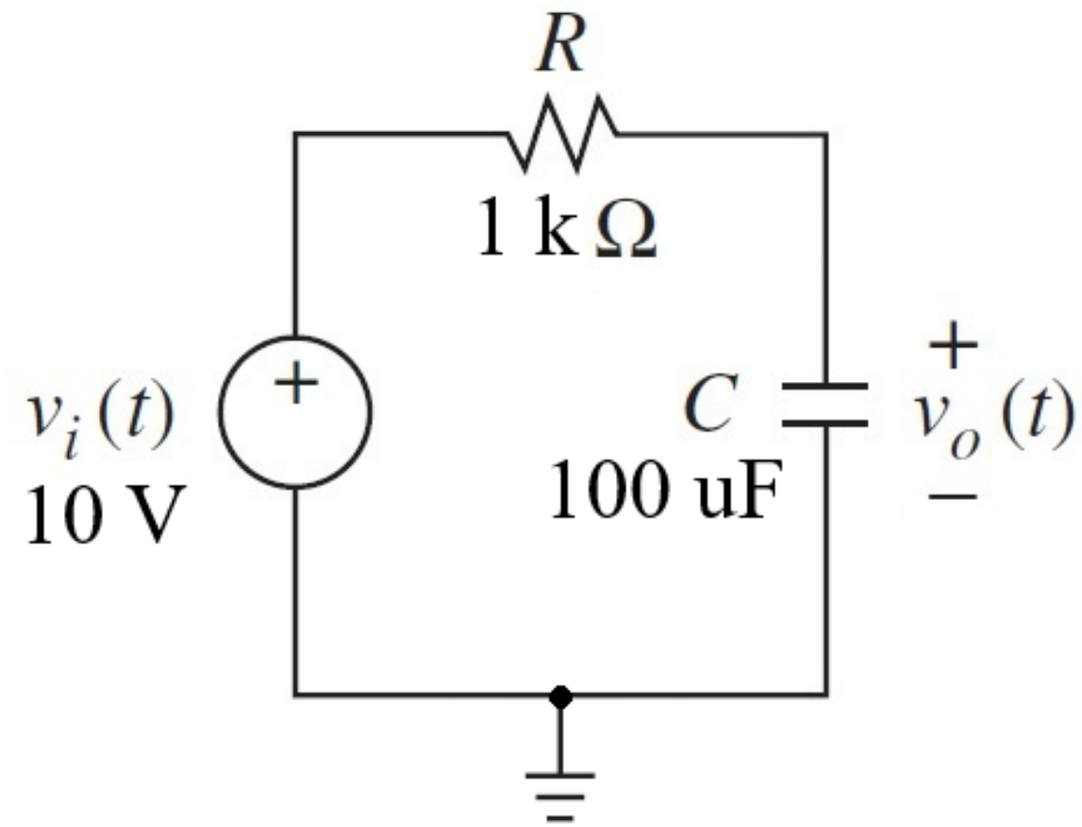
- It predicts the probability of a variety of outcomes when the potential for random variables is present.
- Most of the static limitation parameters of the electronic component and device are influenced by the type, value and tolerance of the components and devices used in the circuit.
- We use it to calculate variations around nominal electrical values (i.e. voltage, current, or power) using SPICE-based simulators.

Monte Carlo Analysis

Example 1 - Component tolerances of a RC circuit

The diagram in the figure below shows a typical series RC circuit with R = 1kΩ and C = 100 μF.

In this circuit, the capacitor charges in a time dependent on the time constant i.e. the voltage is about 63% of the power supply after RC seconds.



In this case, the voltage across the capacitor is 6.32 V after exactly $\tau = RC = (10^3)(10\times10^{-6}) = 0.01$ s.

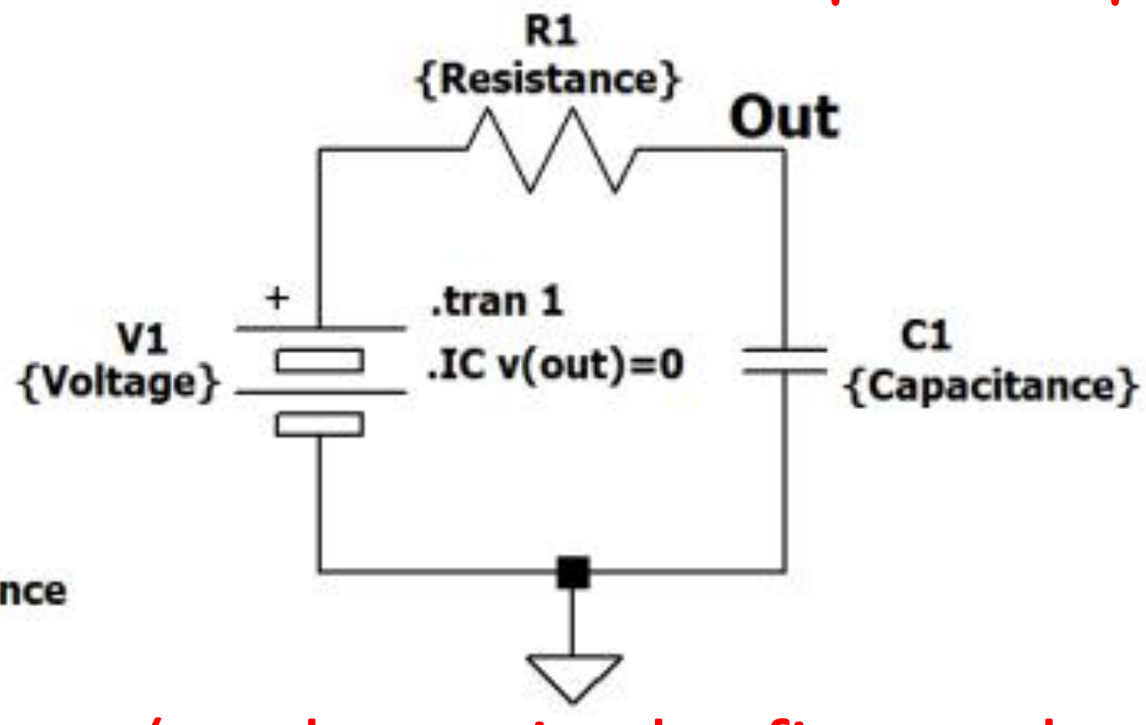
Perform Monte Carlo analysis for the circuit. [32 marks]

Monte Carlo Analysis

The values of the components are not to be ideal but real, with the following tolerances:

- Battery V_1: 10 V with 2% tolerance, i.e. 9.8 V-10.2 V.
- Resistor R_1: 1000 Ω with 10% tolerance, i.e. 900 Ω-1100 Ω.
- Capacitor C_1: 100 μF with 25% tolerance, i.e. 75 μF-125 μF.

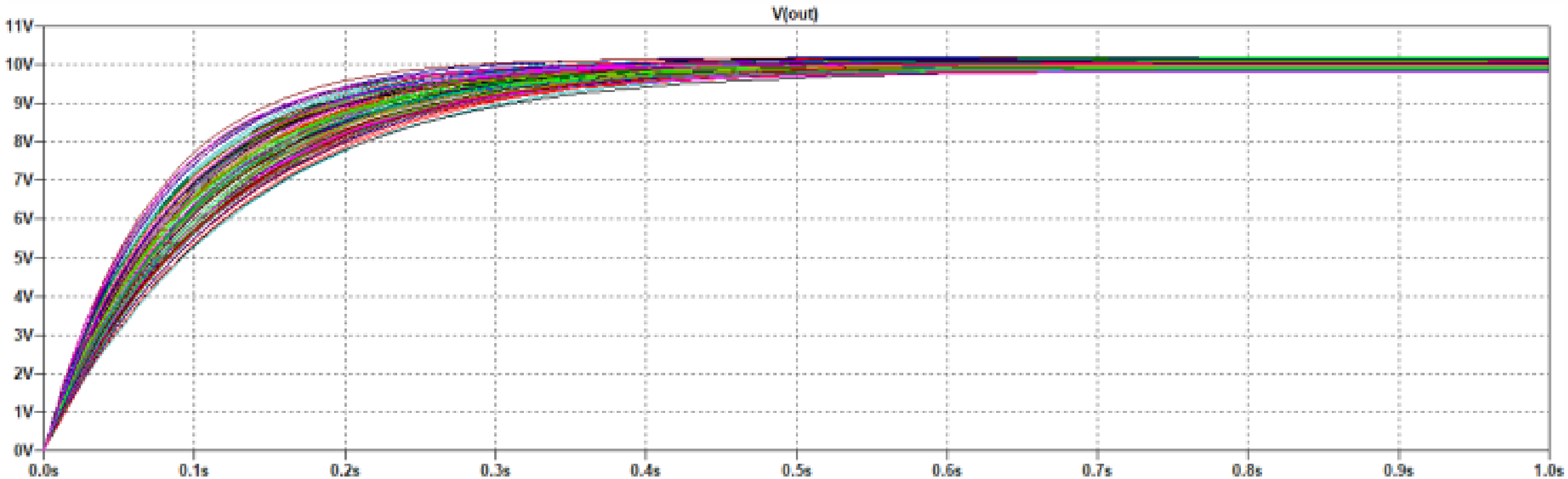
```
.param Voltage=mc(10,2/100)
.params Resistance=mc(1000,10/100)
.params Capacitance=mc(100u,25/100)

.step param Simulations 1 100 1

.meas TRAN V_Batt PARAM Voltage
.meas TRAN R_Res PARAM Resistance
.meas TRAN C_Cap PARAM Capacitance

.meas TRAN RC PARAM Resistance*Capacitance
```



- The simulation of the scheme (as shown in the figure above) is performed one hundred times.
- It generates a hundred different values for each component.

Monte Carlo Analysis

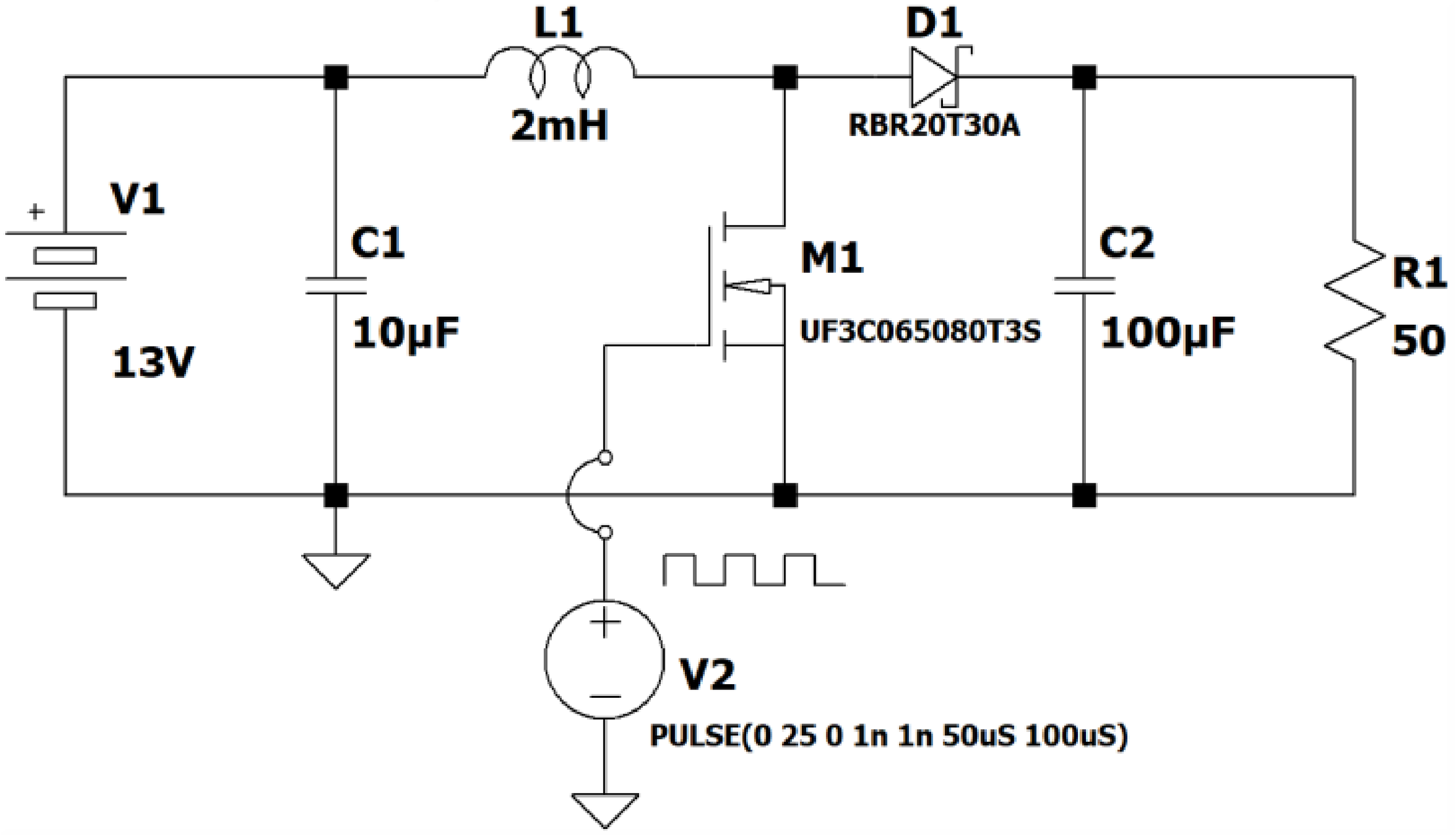
- The graph shows the voltage on the capacitor, precisely in the time interval between 0.069559 and 0.13325 s, with 100 Monte Carlo simulations performed.
- The variation of the components in different contexts makes us understand how they can influence and modify the behaviour of an electronic circuit and its timing.



Monte Carlo Analysis

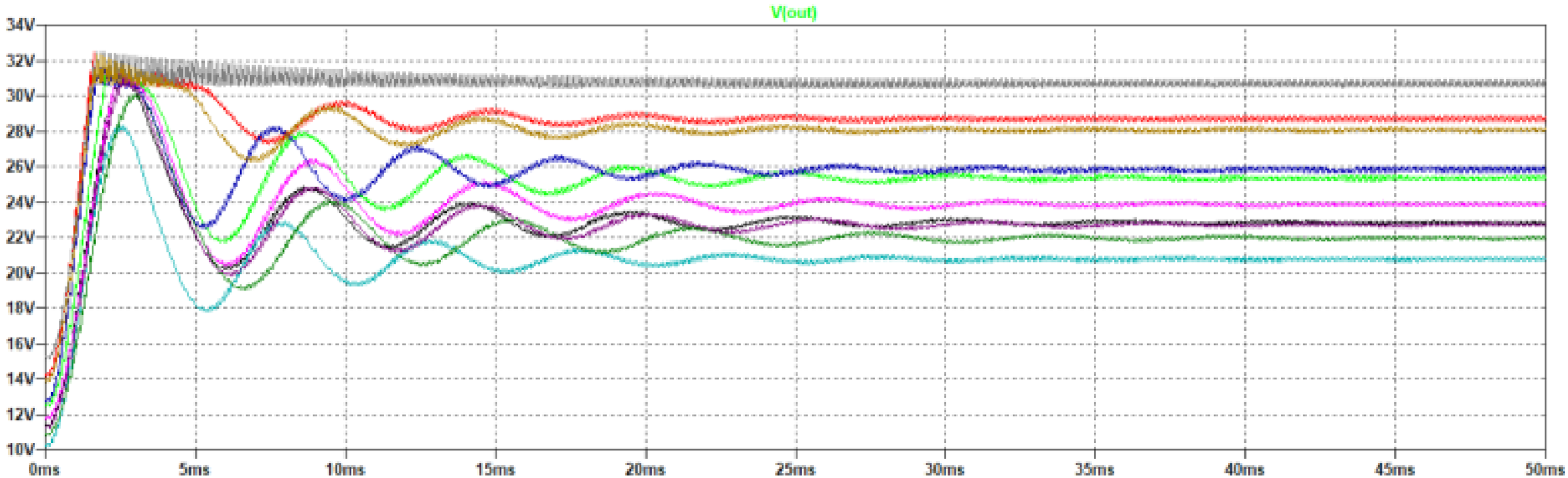
Example 2 - Component tolerances of a Boost converter circuit.

Perform Monte Carlo analysis for the circuit with component values are arbitrarily varied. [20 marks]



Monte Carlo Analysis

- The result of the Monte Carlo analysis for the circuit is shown in the figure below.



- The graph shows the voltage on the load depending on the different values of the electronic components.