XMUT303 Analogue Electronics

Note 4: Static Limitations

Topics:

- Static imperfections.
- Input offset voltage.
- Input biased and offset currents.
- Nulling.
- Monte Carlo analysis.

4.1. Static Imperfections

Static limitation is imperfection and limitation of op-amp due to input-referred errors, noticeable in high-dc-gain applications. Examples of static limitation are: input bias current, input offset current, input offset voltage, and these are also related other topics in op amp such as CMRR and gain non-linearity.

- Input bias current: a small current flows into both inputs to bias the input transistors of the op amp.
- Input offset current: difference between input bias current at inverting and non-inverting inputs of the op amp.
- Input offset voltage: voltage required between the inputs of the op-amp to make the output zero.
- Nulling: Effort to remove or null the voltage offset or current bias.

The following table shows input bias current, input offset current and input offset voltage of practical op amps from their manufacturer datasheets. As shown in the table that these are very small compared with the operating voltage and current of the op amp circuits.

But, for precision applications, these limitations will contribute significantly towards the errors and accuracy of the applications.

Op Amp	I_B	I_{OS}	V_{OS}
NE5534	800 nA	10 nA	0.5 mV
LF411	50 pA	25 pA	0.8 mV
LM318	150 nA	30 nA	4 mV
uA741	80 nA	20 nA	1 mV

Table 4.1: static limitations of several practical op amps

4.2. Input Offset Voltage (V_{OS})

Ideally, shorting the inverting pin of the op amp with the non-inverting pin $V_N = V_P$ should give V_O = 0. But, in real life application circuits, practical op amp will generally yield $V_O \neq 0$. This is due to inherent mismatches between the input stage of op amp as a result of inaccuracy and defects that will be expected from manufacturing the devices in the factories.

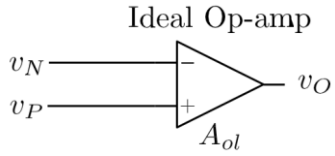


Figure 4.1: An ideal op amp circuit

Practically, imbalance between the inverting and non-inverting voltages V_N and V_P leads to some offset at the output voltage of the op amp (V_O).

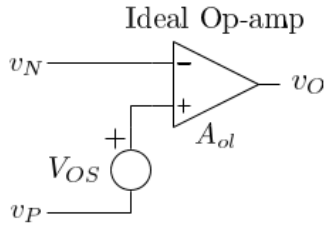


Figure 4.2: Offset voltage in an ideal op amp circuit

The output voltage of the op amp with the offset voltage included is calculated from the following equation:

$$V_O = A_{ol}(V_P - V_N + V_{OS}) \qquad (Eq. 1)$$

In the equation above, V_{OS} is the input offset voltage i.e. a tiny voltage source in series with one of op-amp inputs.

To force the output voltage of the op amp (V_O) to zero, a suitable correction voltage must be applied between the pins.

4.2.1. Errors Caused by V_{OS}

Error voltage added to output voltage as a result offset voltage is multiplied by the DC noise gain. In this case, the larger the noise gain, the larger the error.

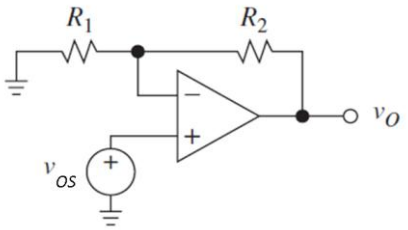


Figure 4.3: Offset voltage in a non-inverting amplifier

For the non-inverting amplifier as shown above, the equation of determining the offset voltage is:

$$E_O = \left(1 + \frac{R_2}{R_1}\right) V_{OS} \qquad (Eq.2)$$

Practically, for uA741 op amp with 1000 times gain, its offset voltage, V_{OS} = 2-6 mV.

4.2.2. Stability of V_{OS}

Offset voltage (V_{OS}) experiences drifts with temperature and time. The equation used to calculate the stability of offset voltage is shown as follows:

$$\text{Temperature coefficient} = \frac{\partial V_{OS}}{\partial T} \left(\frac{\mu\text{V}}{\text{K}}\right) \qquad (Eq.3)$$

Typical values for the the temperature coefficient are 5 µV/°C for general purpose op -amp like uA741 and 0.2 µV/°C for low-input voltage op-amp such as OP77.

Some (low offset) op amps specify drift characteristics in their data sheets. But these are not usually covered for general purpose op amps (i.e. time drift especially).

4.2.3. Common Mode Effects

Ideally, offset voltage (V_{OS}) is only determined by difference between V_P and V_N. The output voltage is calculated from the following equation.

$$V_O = A_{ol}(V_P - V_N) \quad \text{for} \quad A_{ol} \to \infty \qquad (Eq.4)$$

But practically, common mode voltage also affects the output voltage V_O. This is as shown in the equation given below.

$$V_O = A_{ol}(V_P - V_N) + A_{CM}\left(\frac{V_P + V_N}{2}\right) \qquad (Eq.5)$$

Notice that the Common Mode Rejection Ratio (CMRR) of the op amp amplifier circuit is calculated from:

$$\text{CMRR} = \left|\frac{A_{ol}}{A_{cm}}\right| \qquad (Eq.6)$$

This results in ideally CMRR = ∞. Practically CMRR is about 100 dB at DC. Referring to the frequency response of typical op amp amplifier circuit, the CMRR rolls off above frequency about 100 Hz.

The reason for this finite CMRR value is due to input stage imbalances and external component flaws due to device value tolerance.

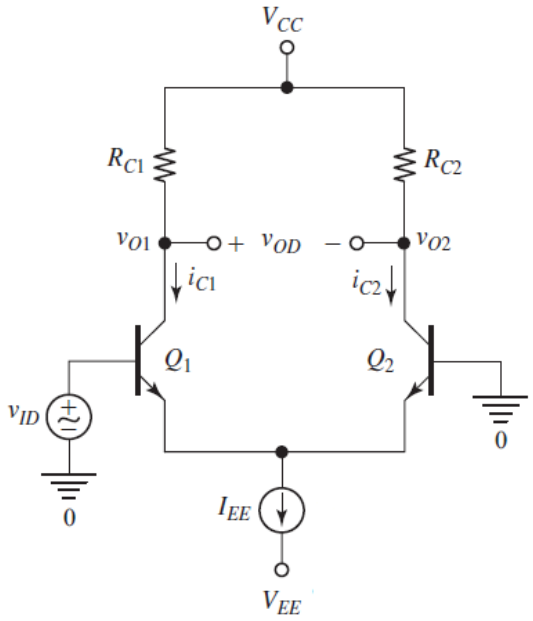


Figure 4.4: Single-ended differential amplifier circuit

As illustrated in the figure above, there are input stage imbalances between the inverting pin and non-inverting pin of the op amp. This is further exacerbated by single-ended topology in the output of the op amp as compared with more balanced dual-ended topology.

External component flaws such as component tolerance of the devices used in the circuit (e.g. resistor and capacitors typically have 5%, 1%, 0.1%, etc., component tolerance).

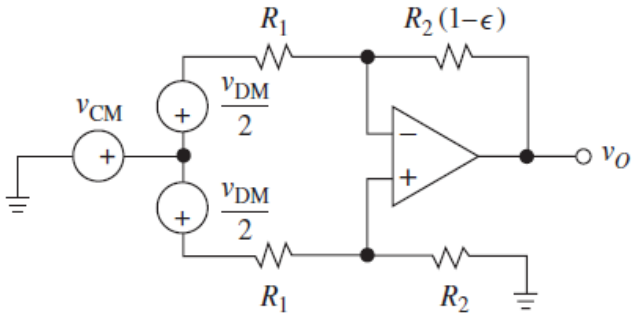


Figure 4.5: Difference amplifier circuit with component tolerance static limitations included

Knowing that the common mode voltage and the common mode rejection ratio are found from the following equations:

$$V_{cm} = \frac{(V_P + V_N)}{2} \qquad \text{with} \qquad \text{CMRR} = \frac{A_{ol}}{A_{cm}} \qquad (Eq.7)$$

Provided that common mode voltage (V_{CM}) is constant, it is included in the model as part of offset voltage (V_{OS}) following the equation below:

$$V_O = A_{ol}(V_P - V_N + V_{OS}) + \left(\frac{A_{ol}}{\text{CMRR}}\right)V_{cm}$$

$$= A_{ol}\left(V_P - V_N + V_{OS} + \frac{V_{cm}}{\text{CMRR}}\right) \qquad (Eq.8)$$

Simplifies calculations, as we already know how to deal with offset voltage V_{OS} as shown above.

4.2.4. Minimising V_{OS}

There are several approaches for minimising offset voltage of the op amp e.g. interleaved transistors, voltage trimming, chopper-stabilised op amps and auto-zero op amps.

4.2.4.1. Interleaved Transistors

Interleaved transistors are about arranging several transistors as alternating in between.

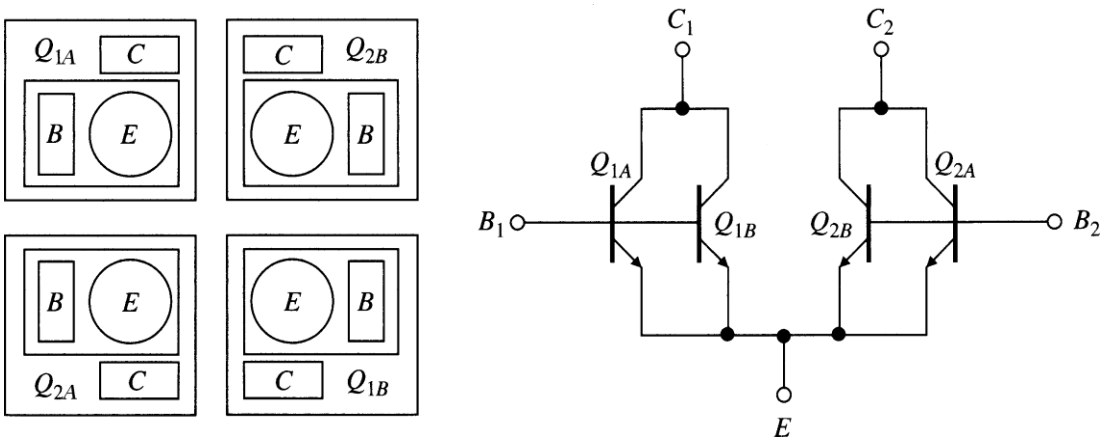


Figure 4.6: Top view and schematic circuit of interleaved transistors

Minimising the offset voltage could also be done by purposeful placement and geometric layout design of complementary components in the device. The figure above (left) shows how the blocks are designed in complementary arrangement.

This also can be done by grouping or pairing up self-compensated components. As illustrated in the figure (right) above, the transistors are arranged in complementary fashion. This will enable these transistors to cancel out their offset voltage imbalances.

4.2.4.2. Voltage Trimming

Another approach for minimizing offset voltage is through voltage trimming. It is about adjusting the voltage at the input of the op amp by a small amount. Perform precision calibration of the differential input.

Minimising the offset voltage (V_{OS}) can be performed by having an internal ladder of resistors network for eliminating the offset. The correct values of the internal resistors are chosen by closing the appropriate switch. The voltage differences due to these resistors are used to compensate the offset voltage of the op amp.

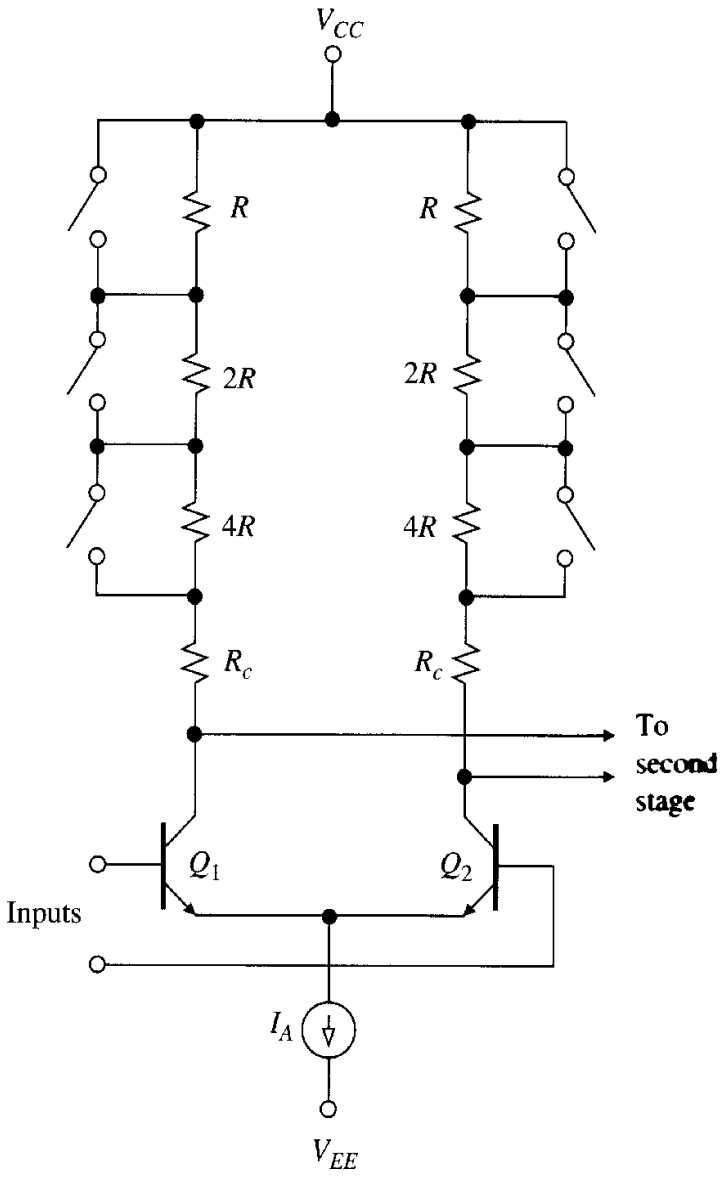


Figure 4.7: Internal ladder of resistors network for eliminating offsets

4.2.4.3. Chopper-stabilised Op-amps

Chopper-stabilised op-amps constantly correct low-frequency errors such as input offset voltage, input bias current, temperature drift, or pink ($1/f$) noise in the inputs of the amplifier.

The best op amps offer offset voltages of 25 µV and 0.1 µV/°C drift. Any offset voltage and drift less than these values require chopper stabilised circuit.

	Conventional (with trim-resistor correction)	Chopper Stabilised
Offset input error	100 μV - 2 mV	Up to 8 μV
Temperature accuracy (-40°C to 125°C)	0.02 μV/°C	1.5 μV/°C

Table 4.2: Performances of conventional vs. chopper stabilised op amps

As illustrated in the figure below, depending on the mode of operation based on the switches in the circuit, the capacitors C_2 and C_3 are charged to the amplifier input and output offset voltage. The voltages that appear across these capacitors are used to compensate for the op amp offset voltage. Notice the speed of the compensation operation of the chopper circuit depend on the frequency of operation of the chopper circuit.

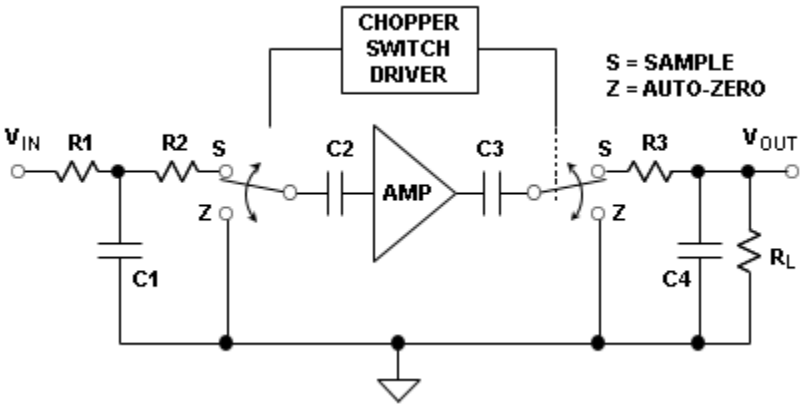


Figure 4.8: Chopper stabilised op amp circuit

By looking at the frequency spectra of the chopping circuit, we could see how offset voltage is removed. Before chopper circuit, we have input signal + offset and noise signals and then after chopper circuit, it is observed as only input signal.

As illustrated in the figure, both the signal and offset voltage and noise are modulated with square wave signal. This modulated signal is then amplified by the amplifier. After the amplifier stage, the signal is demodulated by the same square wave signal to remove the square wave signal.

Looking into the frequency spectra graph, the signal, offset voltage and noise are spread out into their harmonics and in the end, most of frequency components of the offset and noise signals are removed by

the low pass filter in the circuit. The output of the chopper stabilized op amp circuit contains only the input signal with substantially less offset and noise signals present.

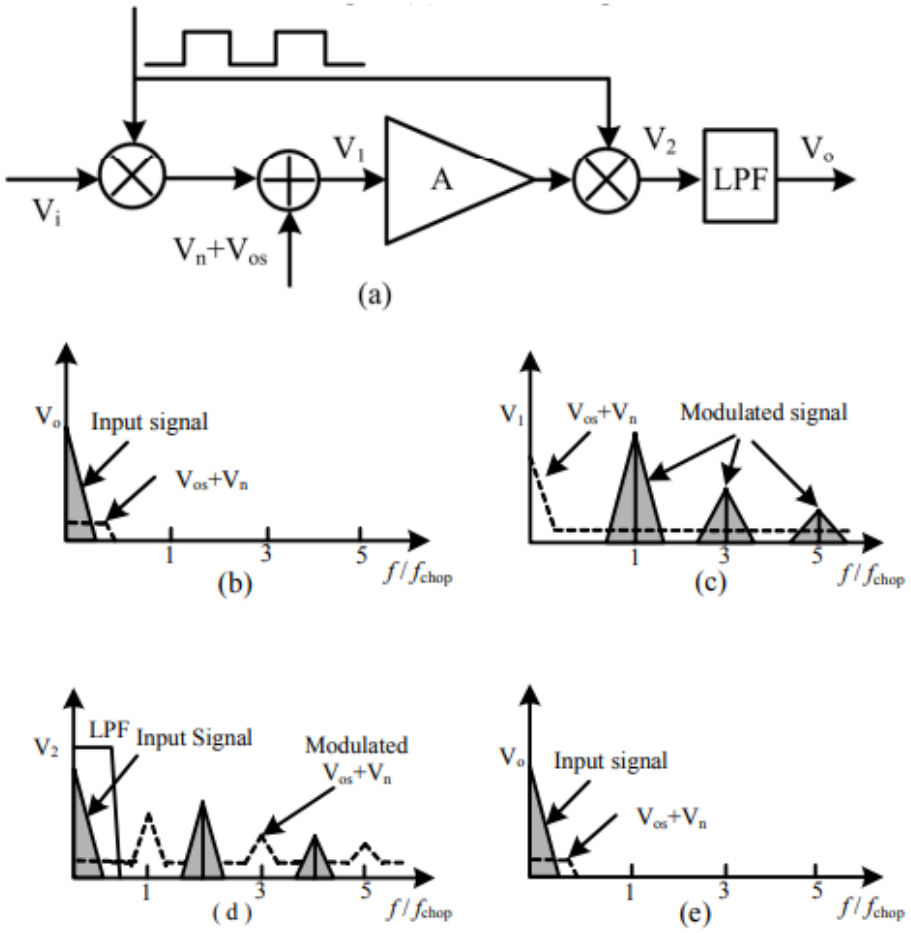


Figure 4.9: Frequency spectrum of chopper stabilised op amp circuit

4.2.4.4. Auto-zero Op-amps

Auto-zero op amps contains internal circuitry that automatically correct offset voltage. As shown in the figure given below, nulling amplifier, OA_2, monitors the input offset voltage of main amplifier O_{A1}. In this case O_{A2} amplifier drives O_{A1}'s output to zero by applying a suitable correcting voltage at its null pin.

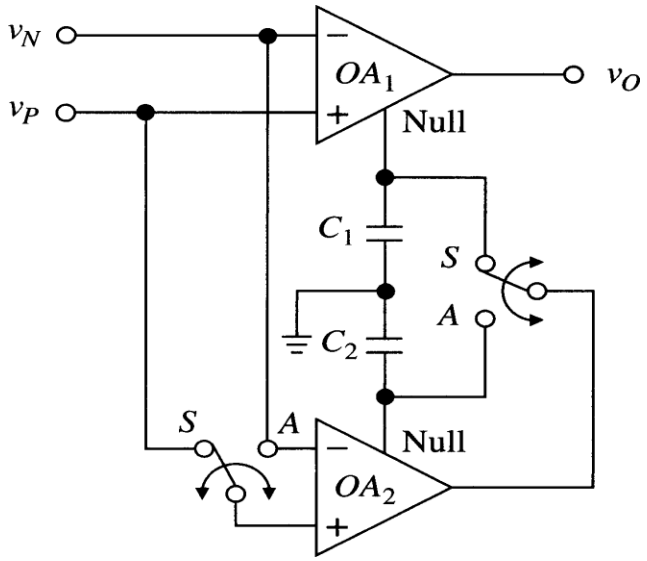


Figure 4.10: Op amp circuit with auto zero nulling amplifier

The operation of auto-zero amplifier is shown in the following figure. Depending on the mode of operation based on the position of the switches in the circuit, when the switch A is on and the switch B is off, the correction amplifier circuit measures the offset voltage of the correction amplifier itself and compensate its offset voltage nulling pin to 0 with the voltage generated by the charged capacitor.

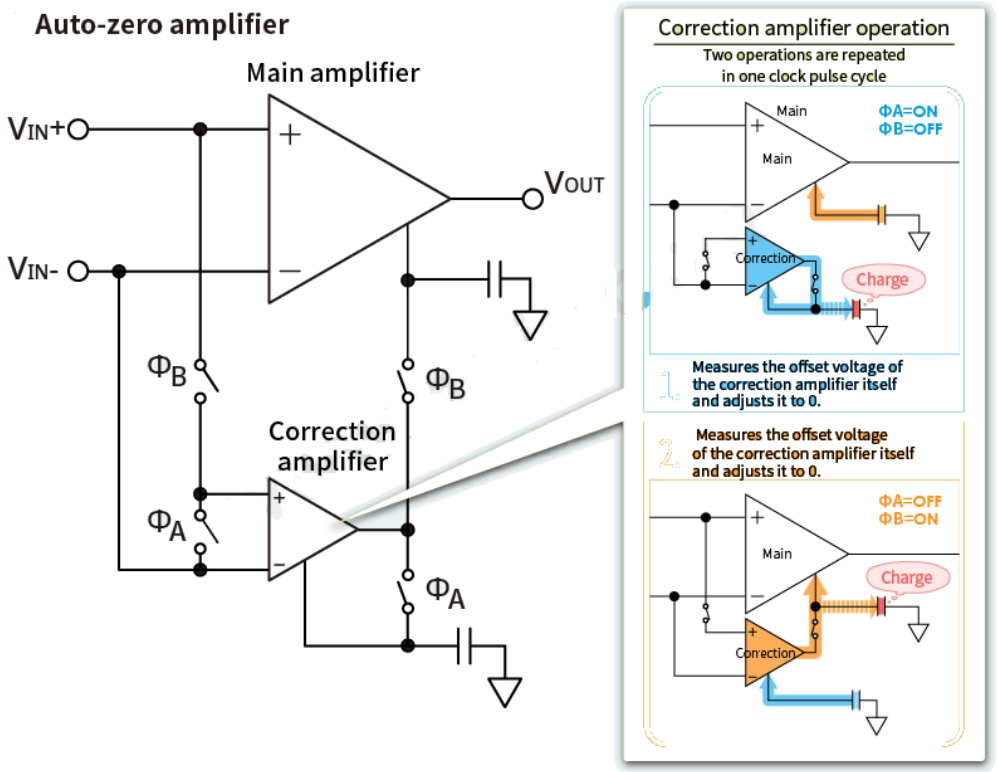
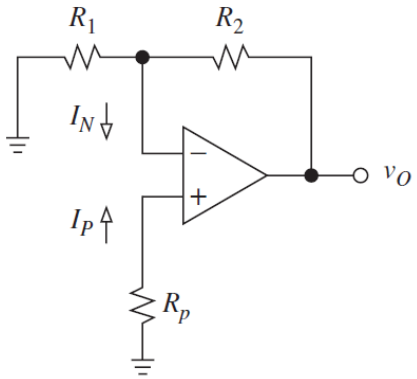


Figure 4.11: Operation of auto-zero amplifier circuit

When the switch A is off and the switch B is off, the main amplifier circuit measures the offset voltage of the correction amplifier and adjust its own offset voltage nulling pin to 0 by charging the capacitor.

Example for Tutorial 1 – Offset Voltage 1

In the circuit of the figure below, let R_1 = 22 kΩ and R_2 = 2.2 MΩ, and let the op amp ratings be I_B = 80 nA and I_{OS} = 20 nA.



a. Calculate error voltage at the output E_O for the case R_p = 0. [6 marks]

b. Repeat, but with $R_p = R_1 \parallel R_2$ in place. [2 marks]

c. Repeat part (b), but with all resistances simultaneously reduced by a factor of 10. [2 marks]

d. Repeat part (c), but with the op amp replaced by one with I_{OS} = 3 nA. [2 marks]

e. Comment on the results obtained in parts (b)-(d) for reducing the error. [2 marks]

Solution

a. The DC noise gain is calculated from:

$$A = 1 + \frac{R_2}{R_1} = 1 + \frac{2.2 \times 10^6}{22 \times 10^3} = 101 \text{ V/V}$$

Moreover, since the value of R_2 is 100 times of R_1, a parallel of R_1 and R_2 is approximately:

$$R_p = (R_1 \parallel R_2) \cong 22 \text{ k}\Omega$$

With R_p = 0, the error at the output of the op amp is dominated by the input bias current at the input, we have the error at the output voltage to be:

$$E_O = 101(R_1 \parallel R_2)I_N \cong 101(R_1 \parallel R_2)I_B \cong 101(22 \times 10^3)(80 \times 10^{-9}) \cong 175 \text{ mV}$$

b. With $R_p = R_1 \parallel R_2 \cong 22\ \text{k}\Omega$ in place, the error at the output of the op amp is dominated by the input offset current at the input, the error in the output voltage is:

$$E_O \cong 101(22 \times 10^3)(\pm 20 \times 10^{-9}) = \pm 44\ \text{mV}$$

where we write "±" to reflect the fact that I_{OS} may be of either polarity.

c. Like part (b), with all resistances reduced by a factor of 10 (e.g. R_1 = 2.2 kΩ, R_2 = 220 kΩ, and R_p = 2.2 kΩ), we get the error in the output voltage to be:

$$E_O = 101(2.2 \times 10^3)(\pm\ 20 \times 10^{-9}) \cong \pm\ 4.4\ \text{mV}$$

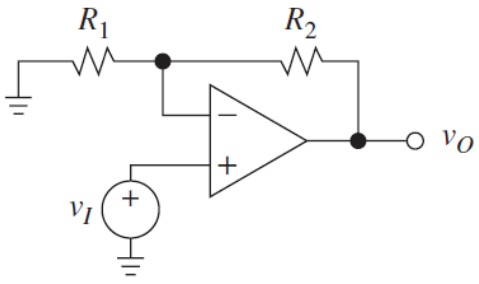
d. Like part (c), with the op amp replaced by a better op amp with I_{OS} = 3 nA, the error in the output voltage is:

$$E_O = 101(2.2 \times 10^3)(\pm\ 3 \times 10^{-9}) \cong \pm\ 0.7\ \text{mV}$$

e. Summarising, with R_p in place, error in the output voltage E_O is reduced by 4; scaling the resistances reduces E_O by an additional factor of 10; finally, using a better op amp reduces it by yet another factor of 7.

Example for Tutorial 2 – Offset Voltage 2

A noninverting amplifier with a closed-loop gain of 1000 is designed using an op amp having an input offset voltage of 3 mV and output saturation levels of ±13 V.



a. What is the maximum amplitude of the sine wave that can be applied at the input without the output clipping? [2 marks]

b. If the amplifier is capacitively coupled, what would the maximum possible amplitude be? [2 marks]

Solution

a. If the maximum output is 13 V, the maximum input is:

$$V_I(\max) = \frac{V_O}{A_v} = \frac{13\text{ V}}{1000} = 13\text{ mV}$$

At the non-inverting pin of the op amp, of that 3 mV is the offset, leaving a maximum signal amplitude of:

$$V_I'(\max) = V_I(\max) - V_{OS} = 13\text{ mV} - 3\text{ mV} = 10\text{ mV}$$

b. If the amplifier is capacitively coupled on the input, we can use superposition for the analysis, adding the DC offset voltage source and the AC input source.

Since for the DC source the gain path has an open circuit, there will be no current flowing in it, and the output voltage from the offset is equal to the offset voltage, 3 mV.

The result is that the AC source can supply up to:

$$V_O'(\max) = V_O(\max) - V_{OS} = 13\text{ V} - 3\text{ mV} = 12.997\text{ V}$$

This is effectively 13 V on the output, which corresponds to ≈ 13 mV on the input. This works when the input source is an AC signal only.

4.3. Input Bias Currents

If we consider op amp golden rule, there is no current flows into the inputs. But, in practice we have: i_{IN} ~ µA for BJTs, i_{IN} ~ 10 pA for FETs and i_{IN} ~ 1 pA for CMOS. This is due to DC currents needed in the amplifier's input pins for the op amp to operate (cf. parasitic capacitances in the device).

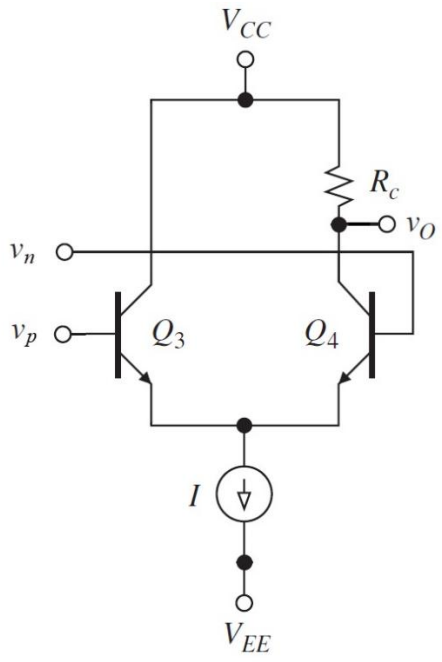


Figure 4.12: Single-ended differential amplifier

Generally current in the non-inverting input (I_N, N) is not equal to inverting input (I_N, P). This is further leading towards a further imperfection that is the offset bias current. The input bias current can be measured through experimental circuit as shown in the figure below.

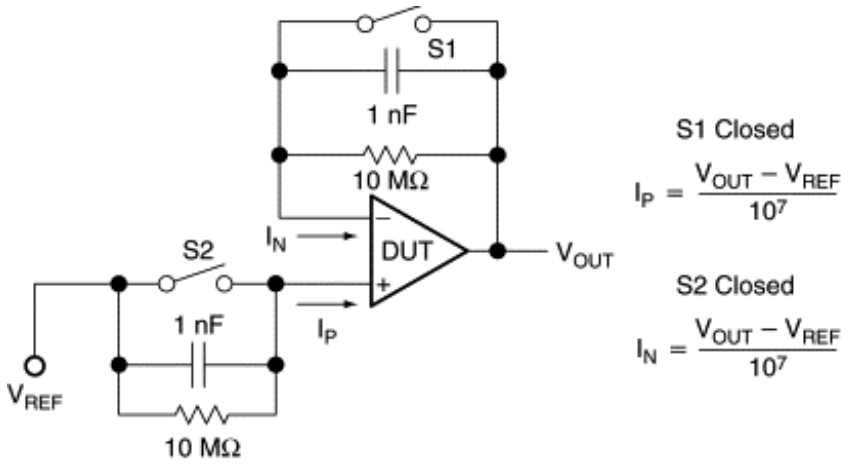


Figure 4.13: Experimental circuit for testing input bias currents of an op amp

From the circuit, the bias current can be calculated from the following equation:

$$I_B = \frac{i_N + i_P}{2} \qquad (Eq. 9)$$

Then, the offset current is found from the following equation:

$$I_{OS} = (i_N - i_P) \qquad (Eq. 10)$$

4.3.1. Errors Caused by I_B

For a given non-inverting amplifier (with bias current only), the output voltage of the amplifier circuit is calculated from the following equation:

$$V_O = \left(1 + \frac{R_2}{R_1}\right) V_P + R_2 I_N \qquad (Eq. 11)$$

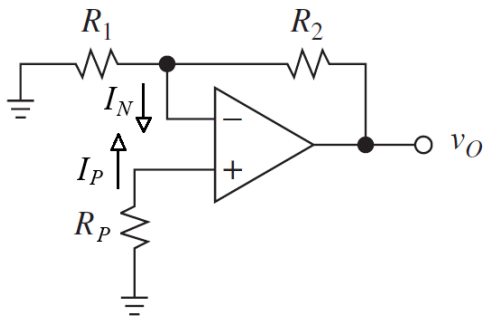


Figure 4.14: A simple-op amp based non-inverting amplifier

Applying both bias and offset currents, $V_p = I_p R_p$, we can calculate the output voltage of the non-inverting amplifier circuit as follows:

$$V_o = R_2 I_N - \left(1 + \frac{R_2}{R_1}\right) R_P I_P \qquad (Eq. 12)$$

Rearrange the equation given above to have a common $(1 + R_2/R_1)$ for both inverting and non-inverting parts in the equation.

$$V_o = \left(1 + \frac{R_2}{R_1}\right)\left[\left(\frac{R_2}{1 + R_2/R_1}\right) I_N - R_P I_P\right]$$

$$= \left(1 + \frac{R_2}{R_1}\right)[(R_1 \parallel R_2) I_N - R_P I_P] \qquad (Eq. 13)$$

4.3.2. Minimising I_B Errors

We can minimise error due to input bias current (I_B) by setting the resistor $R_p = R_1 \parallel R_2$.

$$V_o = \left(1 + \frac{R_2}{R_1}\right)(R_P I_N - R_P I_P) \qquad (Eq. 14)$$

The output voltage with offset bias current included in the equation is determined as follows:

$$V_o = \left(1 + \frac{R_2}{R_1}\right) R_P I_{OS} \qquad (Eq. 15)$$

This leaves the equation with offset current only. Similarly, reducing the value of resistors R_1, R_2 and R_p will reduce offset current error.

For a further example, the following figure shows an integrator circuit that consists of a first-order RC op amp-based filter circuit with appropriate capacitor and resistor.

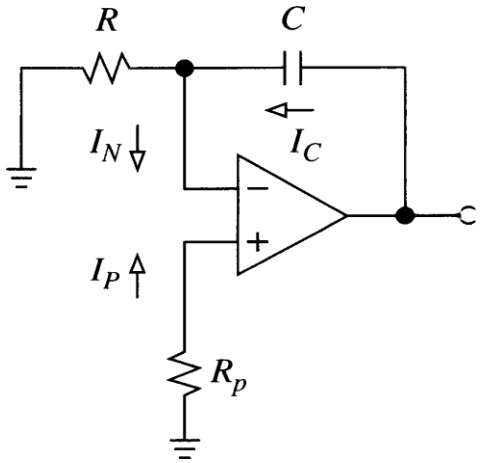


Figure 4.15: A simple op amp-based integrator circuit

Considering the response of the first order RC circuit, the output voltage of the integrator circuit is derived from the following equation:

$$V_o = \frac{1}{RC}\int_o^t V_{in}dt \qquad (Eq.16)$$

Assuming constant input bias current I_B and offset bias current I_{OS}, the output voltage of the integrator circuit is shown in the equation given below.

$$V_o = \left[\frac{(R - R_P)I_B - (R + R_P)\frac{I_{os}}{2}}{RC}\right]t \qquad (Eq.17)$$

We could minimise bias current error with assigning the resistors $R_p = R$ as shown in the equation below. We have only offset current error and choosing large value of C will reduce this error.

$$V_o = -\left(\frac{RI_{os}}{RC}\right)t = -\left(\frac{I_{os}}{C}\right)t \qquad (Eq.18)$$

4.3.3. Avoiding I_B Problems

There are several methods for avoiding the input bias current such as: super beta BJTs, input bias cancellation, and field effect transistor technologies as in the JFET and MOSFET.

4.3.3.1. Super Beta BJTs

A super-beta transistor is a single BJT made with a very narrow base region e.g. LM108 op amp. It has very high β ($\sim 10^4$) and provides high input impedance and ultralow input bias currents for high-speed applications. This transistor minimises the input bias current (I_B) as it has very narrow base structure, so require less biasing current.

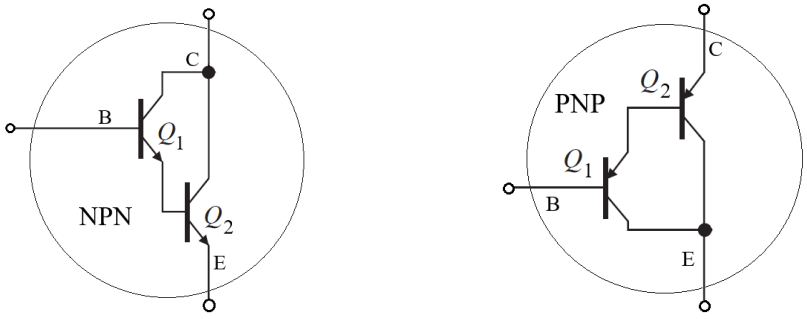


Figure 4.16: A schematic layout of Darlington transistor

As far its fabrication is concerned, it is very similar to arrangement of Darlington pair transistor (e.g. two separate transistors).

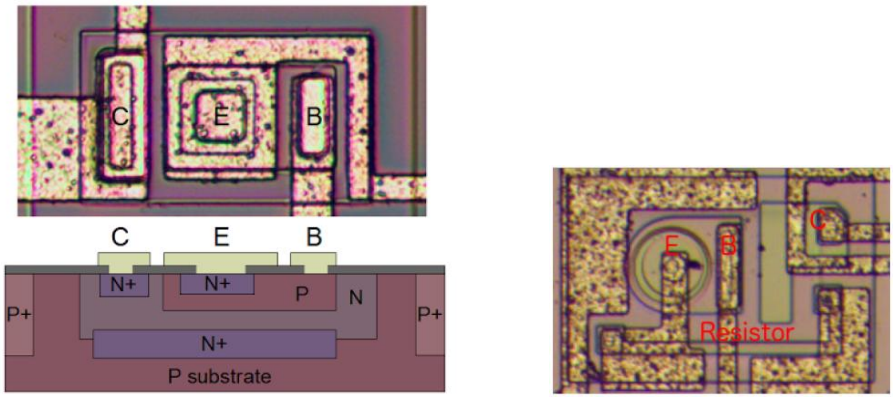


Figure 4.17: Super Beta BJT transistor of LM108 (right) compared with uA741

4.3.3.2. Input Bias Cancellation

For input bias cancellation approach, we determine first the "estimate" required bias currents and supply internally – then, this reduces i_{IN}.This arrangement minimise input bias current I_B by providing internal biasing current compensation network. For example, see the input stage section of OP77 as shown in the figure given below.

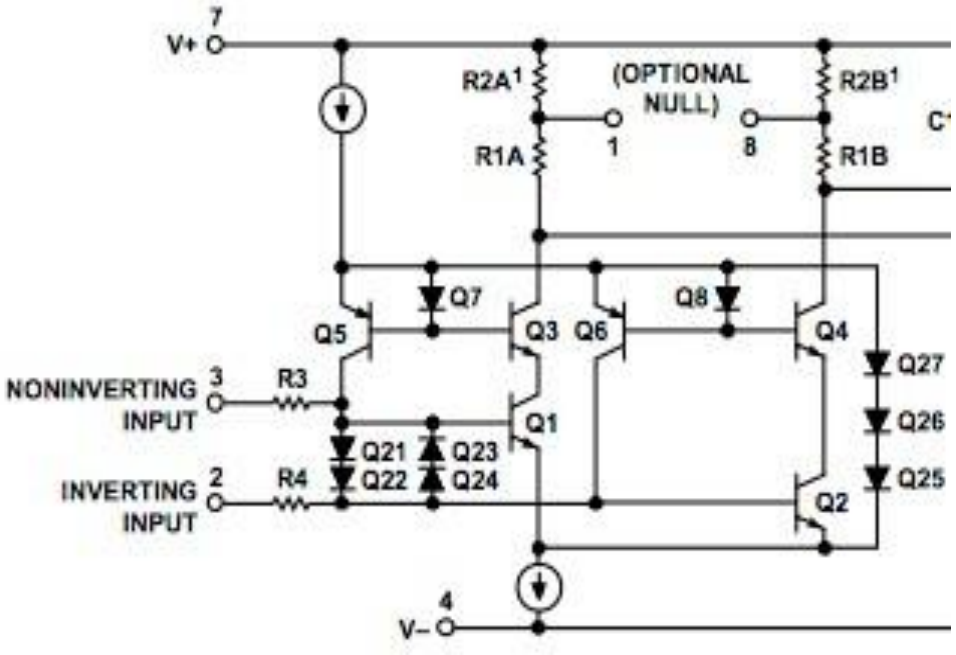


Figure 4.18: Input stage circuit of OP77 op amp

Input stage section of OP77 op amp has a network of diodes which are implemented in the device for providing the required internal biasing current.

4.3.3.3. JFET-Input Op Amps

With the JFET technology, input current (i_{IN}) is reverse current through a PN junction, (cf. i_{BASE} for BJT). This will reduce the input bias current of the transistor.

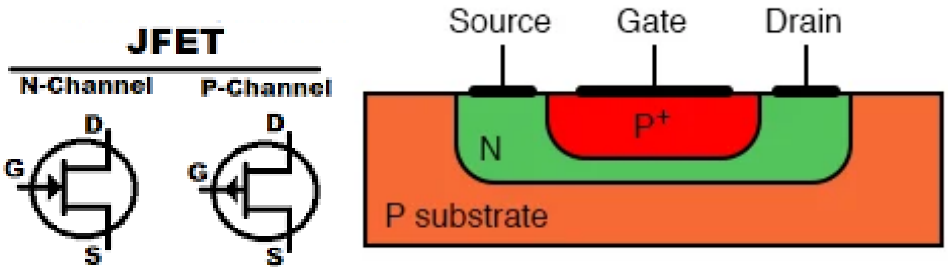


Figure 4.19: JFET notation and its 2-D structure

But biasing current is still needed for controlling the width of the N or P channel. This technology exists in the JFET based input op amps such as e.g. OPA827.

4.3.3.4. MOSFET Op Amps

MOSFET has even lower i_{IN} than JFET. This is due to relatively higher impedance due to insulator layer -> smaller bias current. This higher impedance is further enhanced in the Bi(C)MOS with dual depletion channels. In the end, this results in a small bias offset.

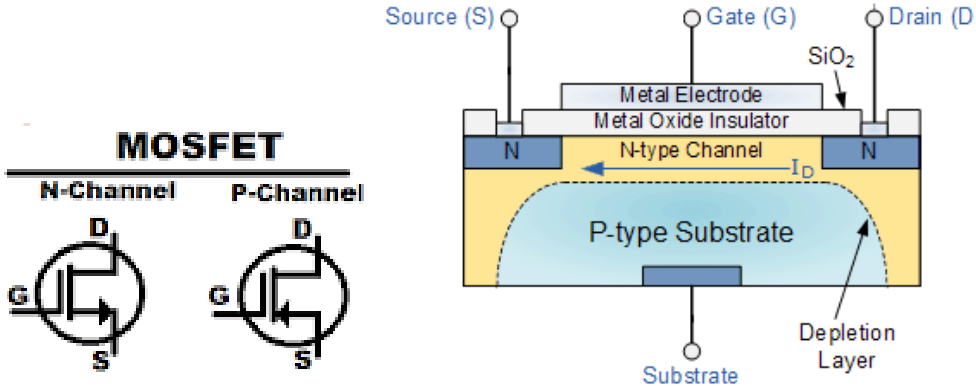


Figure 4.20: MOSFET notation and its 2-D structure

4.3.4. I_B Temperature Dependence

Input bias current (I_B) is very temperature dependent in FETs. It is calculated from the following equation.

$$I_B(T) \approx I_B(T_0)2^{(T-T_0)10} \qquad (Eq.19)$$

As shown in the equation, the input bias current (I_B) is approximately doubles for temperature +10°C. So, we need to keep FETs cool for reduced input bias current.

The following diagram shows the relative merits of the approaches used for minimising the input base current. Compared with the performance of general-purpose op amp, super beta BJTs, cancelation and FET technologies have lower input bias current.

As shown in the given figure, in terms of stability of the operating temperature, op amp with super beta BJTs is comparable in terms of the input bias stability performance with the general-purpose op amp.

Furthermore, the op amp with the cancelation approach is less stable at higher temperature compared with the general-purpose op amp.

The stated op amps with FET and CMOS technologies tend to have their biasing currents to increase proportionally as the operating temperature is increased. Their magnitudes are relatively smaller compared with the biasing currents of the general purpose and super beta op amps. On the other hand, at high temperature, the input biases of these op amps could potentially exceed those of the general purpose and super beta op amps.

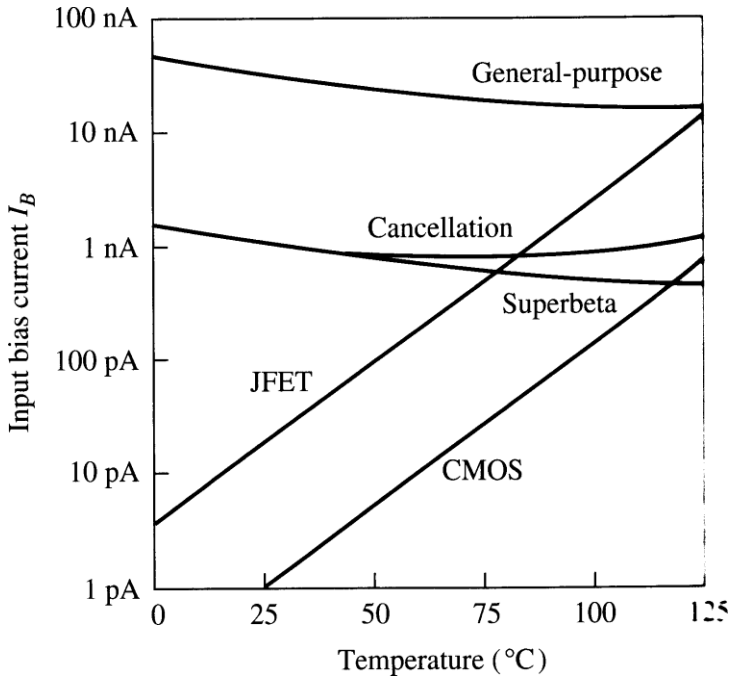
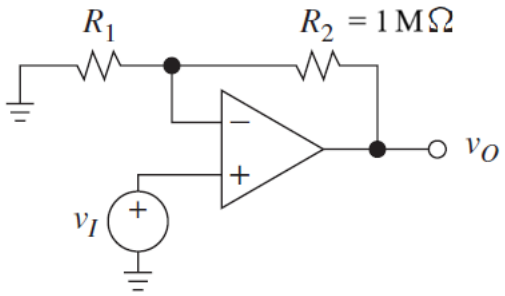


Figure 4.21: Graph of input bias current vs. temperature of several input bias current eliminations

Example for Tutorial 3 – Bias and Offset Currents

An op amp is connected in a closed loop with gain of +100 utilizing a feedback resistor of 1 MΩ.



a. If the input bias current is 100 nA, what output voltage results with the input grounded? [4 marks]

b. If the input offset voltage is ±1 mV and the input bias current as in (a), what is the largest possible output that can be observed with the input grounded? [2 marks]

c. If the bias-current compensation is used, what is the value of the required resistor? If the offset current is no more than one-tenth the bias current, what is the resulting output offset voltage (due to offset current alone)? [4 marks]

d. With the bias-current compensation as in (c) in place what is the largest DC voltage at the output due to the combined effect of the offset voltage and offset current? [2 marks]

Solution

a. This is a non-inverting amplifier circuit.

$$A_v = \frac{R_1 + R_2}{R_1} = 100 \qquad \text{thus} \qquad R_2 = 99R_1$$

Since the feedback resistor is R_2 = 1 MΩ, the resistor to ground must be:

$$R_1 = \frac{R_2}{99} = \frac{10^6}{99} = 10.1\ \mathrm{k}\Omega$$

If the input source is grounded then the inverting input is also at ground and thus all the bias current flows through the feedback resistor, resulting in output voltage:

$$v_o = I_B R_2 = (100 \times 10^{-9})(1)(10^6) = 0.1\ \mathrm{V}$$

b. With an input offset voltage, E_o of ±1 mV, we expect an output:

$$v_o' = A_v E_o = 100 \times (\pm\ 1\ \mathrm{mV}) = \pm\ 0.1\ \mathrm{V}$$

Thus, the maximum output is:

$$v_0 + v_o' = 0.1 + 0.1 = 0.2\ \mathrm{V}$$

c. The bias compensating resistor, R_B, should be equal to the ground resistor, R_1, thus R_B = 10.1 kΩ. This gives rise to a voltage drop which causes exactly the bias current to flow through R_1, no current through R_2, and zero output voltage.

   If the offset current is one tenth of the bias current, then the resulting output voltage is one tenth of the output voltage when considering only bias current without compensation, except that it can be either positive or negative, v_o = ± 0.01 V

d. The value of the output due to offset voltage is 0.1 V with either sign. The value of output due to offset current is 0.01 V with either sign. The largest value of the combined output is 0.11 V, either positive or negative.

4.4. Nulling

Nulling is number of ways to remove DC (static) errors affecting op amps. There are several methods for performing nulling: we can use op amp's built-in offset null circuitry, we can add an external nulling circuit (e.g. external and block nulling circuits), or we can use a better op amp.

Static errors are not static as they also drift with time and temperature. This would later complicate the effort to nullify these errors in the op amp circuit.

No	Measurement	S_1	S_2	S_3	S_4	S_5	S_6
1	Voltage offset	1	1	0	A	a	0
2	Offset and bias current	0/1	0/1	0	A	a	0
3	DC gain	1	1	0	A	a	0/1
4	AC gain	1	1	0	A	A	0
5	DC CMRR	1	1	0	A/B	a/b	0
6	DC PSRR	1	1	0	A/B	a/b	0
7	AC CMRR	1	1	1	C	c	0
8	AC PSRR	1	1	1	D	d	0

Table 4.3: Nulling circuit and op amp testing set up

The following diagram shows a setup of an experimental circuit for nulling process. With this circuit, we can measure op amp parameters such as offset voltage, bias current, gain, CMRR, PSRR, etc. The mode of operation of the testing circuit depends on the set up of the switches provided in the circuit (switches S_1 - S_6).

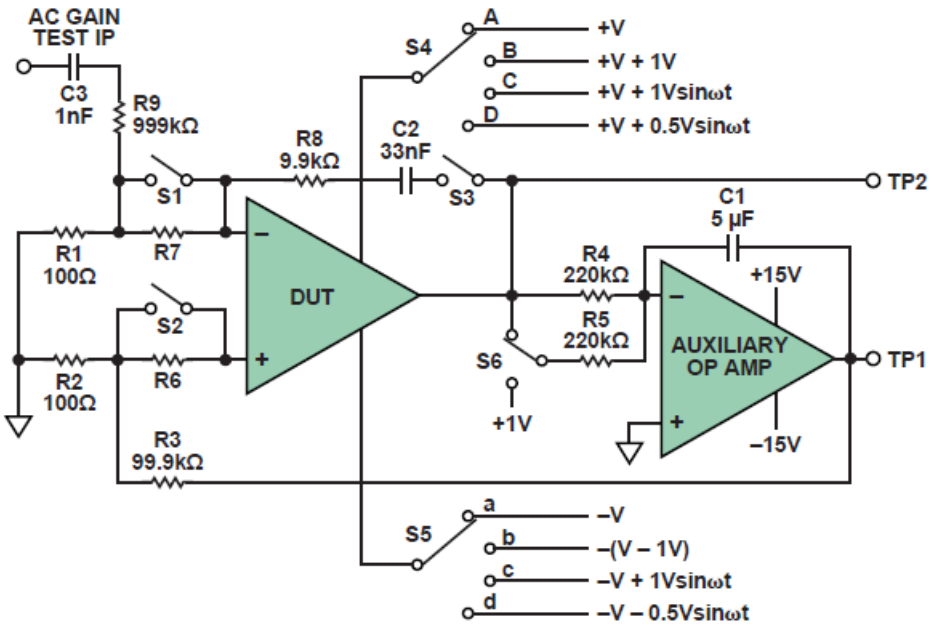


Figure 4.22: Experimental circuit for op amp nulling

4.4.1. Internal Nulling

Many op amps have extra input pins to adjust offsets. These pins deliberately unbalance the input stage to counteract manufacturing imperfections. No standard for external circuit required to interface with internal null circuitry. This feature is not available for bi- & quad- packages.

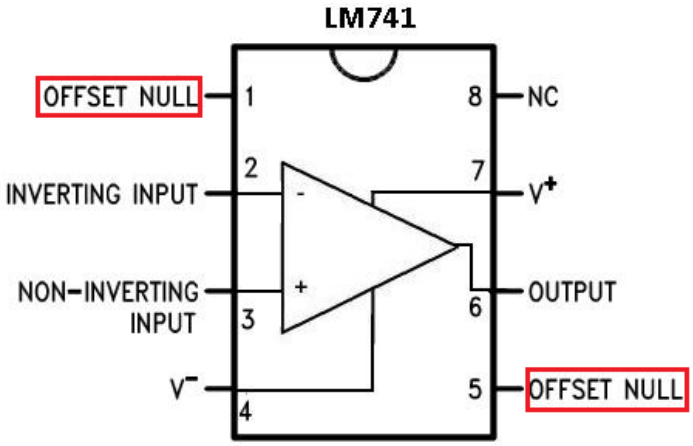


Figure 4.23: Extra input pins in op amp for adjusting offset

The following figure shows the circuit arrangement for nulling processes. Notice that a variable resistor (e.g. 20 kΩ) is used to balance out the voltage between the offset pins with the supply voltage (V_{CC}).

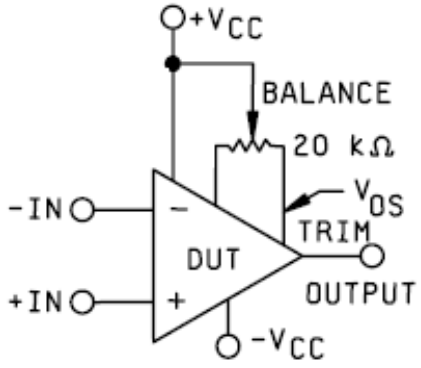


Figure 4.24: External circuit in op amp for nulling purposes

As illustrated in the figure given below, when we see these extra input pins to adjust offsets inside the op amp, these pins are typically located at the current mirror in the differential input stage of the op amp and these offset null pins to balance imperfections in the differential input stage of the op amp.

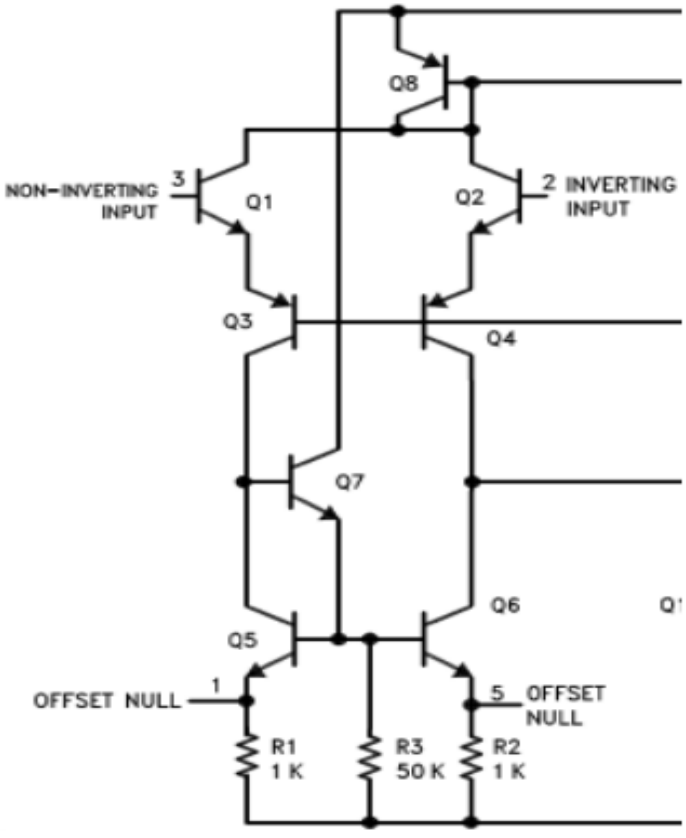


Figure 4.25: Offset nulling circuit in the input stage of an op amp

The following diagram shows internal nulling scheme for inverting and non-inverting amplifiers (left) with internal offset-error nulling (right). Notice the variable resistor and supply voltage set up.

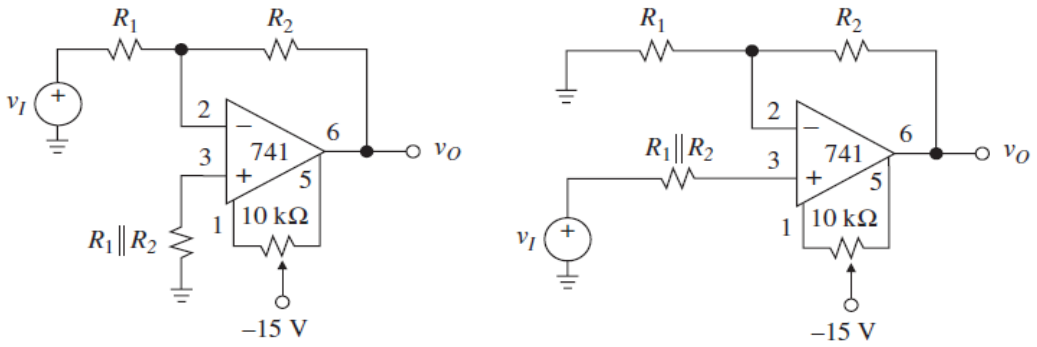


Figure 4.26: Inverting and non-inverting amplifiers with internal offset-error nulling

The following diagram illustrated the integrator with internal offset-error nulling. Notice similar set up of variable resistor for balancing voltage in the nulling pins in the op amp.

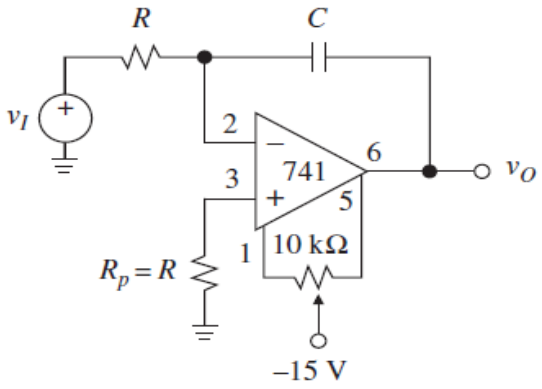


Figure 4.27: Integrator with internal offset-error nulling

4.4.2. External Nulling

External null circuits are required for amplifiers with no internal nulling circuitry. Very similar to internal nulling i.e. it uses offset pins, potential divider resistors and a potentiometer with the supply rail, but the circuit is used for balancing and calibrating the functionality and operation of the circuit. In this arrangement, the input offset is nullified to optimize the performance of the amplifiers.

The following diagram shows an external offset null adjust circuit for the inverting amplifier. Depending on the requirement for nulling, notice that the variable voltage is used to compensate for the offset voltage at the inverting input of the op amp. In the circuit, the offset voltage applied to the inverting input.

$$\text{Offset adjustment range} = \pm V_{CC} \frac{(R_1 \parallel R_2)}{R_3} \qquad (Eq. 20)$$

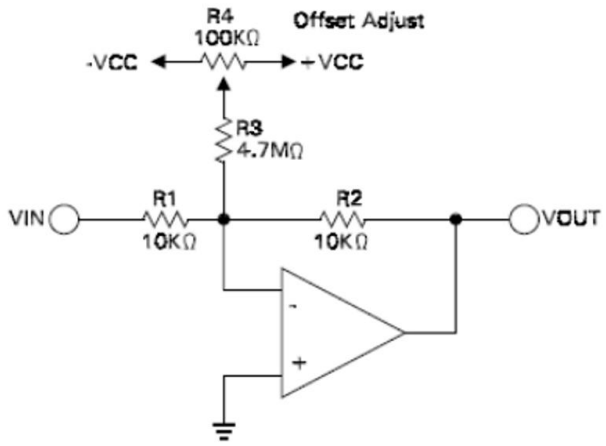


Figure 4.28: External offset null adjusts for inverting input of an inverting amplifier

The following diagram shows the nulling circuit for the voltage at the non-inverting input of the op amp. In the nulling circuit, the offset voltage applied to the noninverting input.

$$\text{Offset adjustment range} = \pm V_{CC}\left(\frac{R_5}{R_3}\right) \qquad (Eq.21)$$

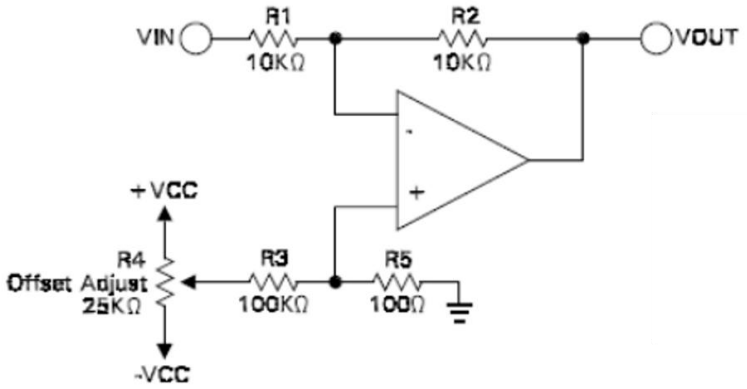


Figure 4.29: External offset null adjusts for noninverting input of an inverting amplifier

The following figure illustrates external offset null adjust circuit for non-inverting amplifier. The circuit shows the same use of the offset pins, potential divider resistors and a potentiometer with the supply rail adjusted for balancing the functionality and operation of the circuit as well.

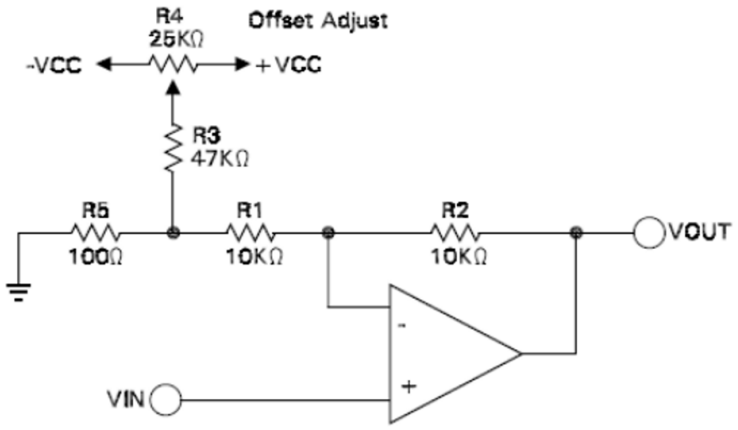


Figure 4.30: External offset null adjusts of a low-gain non-inverting amplifier

In a circuit for low-gain non-inverting amplifier as shown in the figure above, the nulling can typically be performed at a specific node in the circuit as indicated in the figure.

Low gain amplifier tends to have less sensitive calibration process and produce a coarse offset compensation, so it requires additional components (e.g. a drop off resistor) to mitigate these limitations.

Furthermore, this arrangement is usually done to obtain also precise gain adjustment of the amplifier with addition of compensating resistor R_5 implemented in the circuit (in this case $R_3 \gg R_5$).

$$\text{Offset adjustment range } = \pm V_{CC}\left(\frac{R_5}{R_3}\right)\left(\frac{R_2}{(R_1+R_2)}\right) \qquad (Eq.22)$$

Precision gain of stage modified by presence of R_5 in series with R_1:

$$A_V = (R_5 + R_1 + R_2)(R_5 + R_1) \qquad (Eq.23)$$

Disregarding $R_3 \parallel R_5$, since $R_3 \gg R_5$.

In a circuit for high-gain non-inverting amplifier as shown in the figure below, the offset adjustment can be performed straight away like the inverting amplifier.

$$\text{Offset adjustment range } = \pm V_{CC}\left(\frac{R_1}{R_3}\right) \qquad (Eq.24)$$

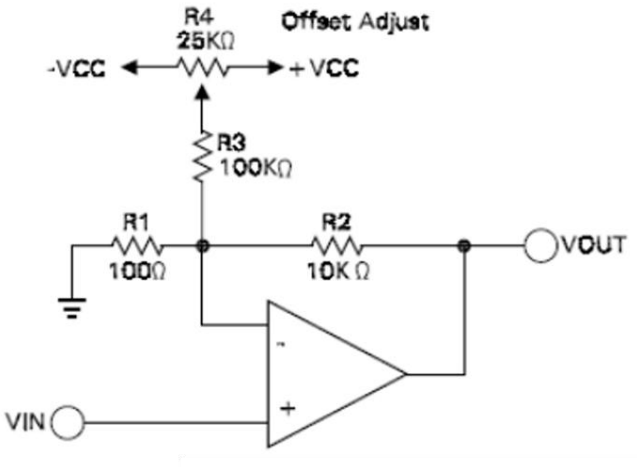


Figure 4.31: External offset null adjusts of a high-gain non-inverting amplifier

The following diagram shows an external offset null adjust for a differential amplifier.

$$\text{Offset adjustment range} = \pm V_{CC}\left(\frac{R_5}{R_3}\right)\left(\frac{R'}{(R_1' + R_2')}\right) \qquad (Eq.25)$$

In this arrangement, voltage offset is compensated at the non-inverting pin of the differential amplifier circuit.

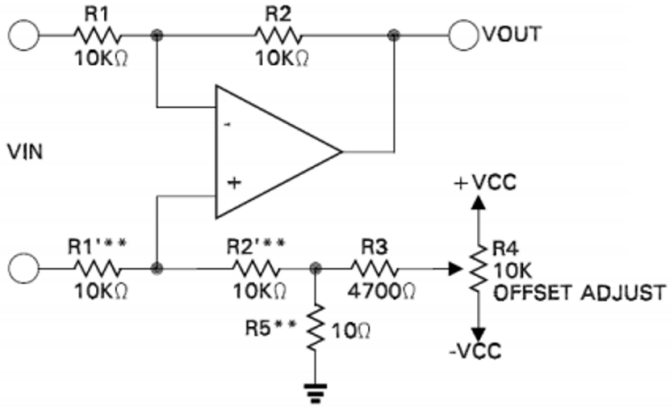


Figure 4.32: External offset null adjusts of a differential amplifier circuit

Furthermore, R_5 also introduces a common mode error, since $R_2/R_1 = (R_2^{'} + R_5)/R_1^{'}$. If necessary, trim $R_2^{'}$ such that $R_2/R_1 = \left(R_2^{'} + R_5\right)R_1^{'}$.

4.4.3. Block-Level Nulling

We can perform multiple parameters nulling with the block-level nulling. We can use a single adjustable point to null entire block. But, be careful with high-gain stages, integrators, etc. as in these types of circuit, we have competing goals and potential cancelling out effects.

With block-level nulling, we typically perform simple tune-in procedure. This is done for avoiding nulling objective conflict(s) as stated above. Only a few op amp-based circuits could have block-level nulling (e.g. specific applications and multiple nulling objectives).

The following figure outlines instrumentation amplifier circuit. The circuit consists of multiple op amp-based amplifiers to form an instrumentation amplifier. It has voltage follower/buffer amplifiers at the inputs and differential amplifier.

The block-level nulling circuit is realized as a gain adjustment of the amplifier circuit via R_g resistor and an input offset nulling circuit with external circuitry. The figure shows the block level offset null and gain adjustment of an instrumentation amplifier:

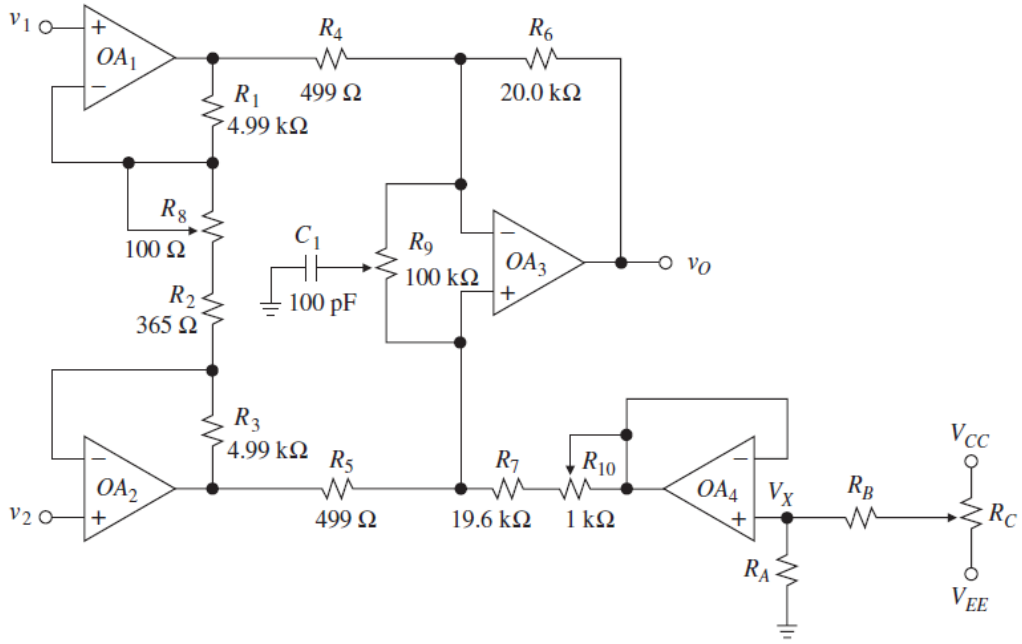


Figure 4.33: Block level nulling implemented in an instrumentation amplifier circuit

The following figure shows a precision elliptic low-pass filter circuit. The filter circuit is made up from a low noise 8th order, clock sweep able, low-pass elliptic antialiasing LTC1064-1 and a LT1007 low-noise, high-speed precision op amp.

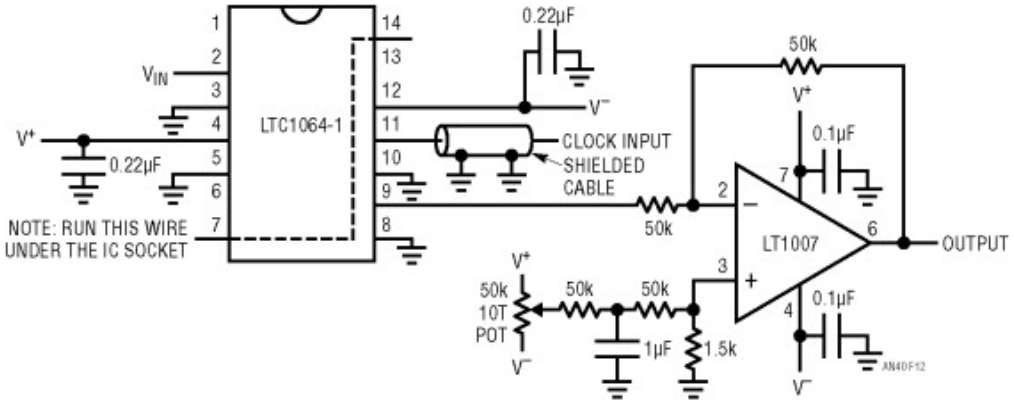


Figure 4.34: Precision elliptic low-pass filter circuit

Temperature stability of the offset voltage is often becoming an important design requirement for precision application of the op amp. It is also for convenient reason that the compensation setting is implemented at one location, instead of multiple locations, hence the chosen block level nulling.

As in the figure shown above, for block-level nulling circuit, we try to correct the offset specifically at 25°C. The offset calibration is performed at the non-inverting pin of the amplifier circuit part. Moreover, the advantage of this approach is that it affects very little the filter's frequency response. Since the circuit is intended to be a filter, any effects due to adjustment should be avoided.

The figure shown below shows the time domain response of the filter circuit. The graph illustrates the rising and falling edge overshoots of a typical of high Q filter i.e. switched capacitor or active RC filter.

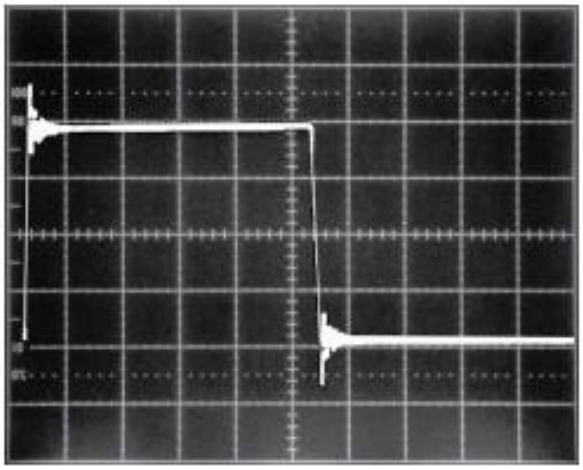
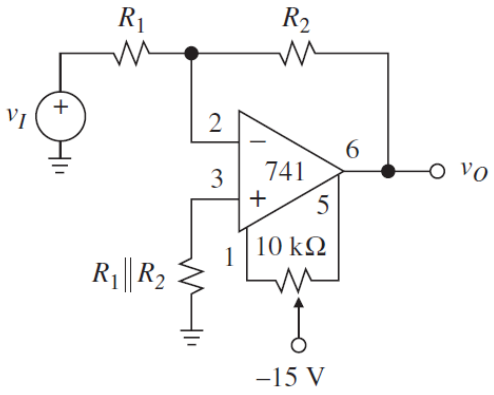


Figure 4.35: Time domain response of the elliptic filter circuit

Example for Tutorial 4 – Nulling Circuits 1

A 741C op amp is to be used in the circuit of the figure below to yield $A_s = -10$ V/V.



If $V_{os}(\max)$ = 6 mV and $I_{os}(\max)$ = 200 nA, specify suitable resistances that will maximize the input resistance R_i of the circuit. [10 marks]

Solution

Since $R_i = R_1$, we need to maximize R_1.

Imposing $R_2 = 10R_1$, and $V_{OS}(\max) + (R_1 \parallel R_2)I_{OS}(\max) \leq 15$ mV, we get:

$$R_1 \parallel R_2 \leq \frac{15\text{ mV} - 6\text{ mV}}{200\text{ nA}} = 45\text{ k}\Omega$$

Or

$$\frac{1}{R_1} + \frac{1}{10R_1} \geq \frac{1}{45\text{ k}\Omega}$$

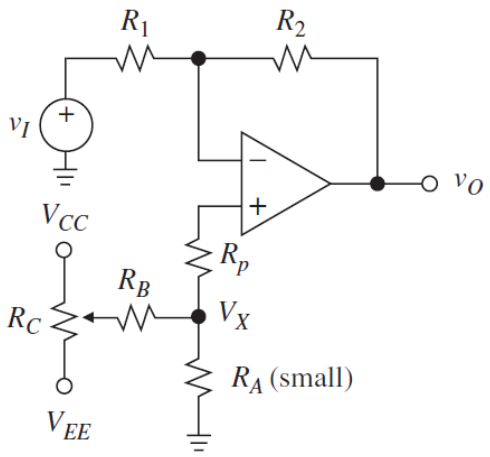
Solving yields $R_1 \leq 49.5$ kΩ.

Use the standard values R_1 = 47 kΩ, R_2 = 470 kΩ, and R_p = 43 kΩ.

Example for Tutorial 5 – Nulling Circuits 2

A 741C op amp is to be used in the circuit given in the figure below to yield A_s = −5 V/V and R_i = 30 kΩ. Specify suitable resistances. Consider $V_{os}(\max)$ = 6 mV and $I_{os}(\max)$ = 200 nA

[12 marks]



Solution

As $R_i = 30\ \text{k}\Omega$, then assign resistor R_1 = 30 kΩ.

For a gain of $A_s = 5$ for the inverting amplifier circuit, then $R_2 = 5R_1$ = 150 kΩ.

As we know that $R_p = R_1 \parallel R_2$, thus the value of R_p is:

$$R_p = R_1 \parallel R_2 = \frac{(30 \times 10^3)(150 \times 10^3)}{(30 \times 10^3) + (150 \times 10^3)} = 25\ \text{k}\Omega$$

Use the standard value R_p = 24 kΩ, and impose R_A = 1 kΩ to make up for the difference.

We have:

$$E_I(\text{max}) = V_{OS}(\text{max}) + (R_1 \parallel R_2)I_{OS}(\text{max})$$
$$= 6\ \text{mV} + (25\ \text{k}\Omega)(200\ \text{nA}) = 11\ \text{mV}$$

To be on the safe side, impose −15 mV ≤ V_X ≤ 15 mV.

Thus, with the wiper all the way up, we want:

$$\frac{R_A}{R_A + R_B} = \frac{15\ \text{mV}}{15\ \text{V}}$$

Or $R_B \cong 10^3 R_A$ = 1 MΩ.

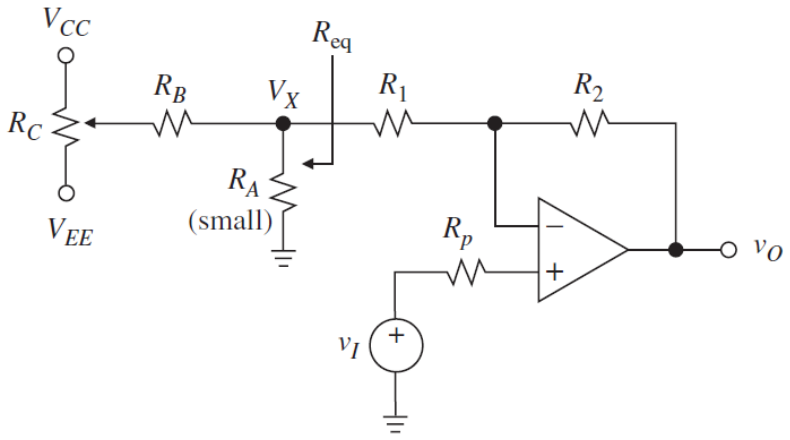
Finally, choose R_C = 100 kΩ as a variable to tune the accuracy.

Example for Tutorial 6 – Nulling Circuits 3

Assuming a 741C op amp in the figure below with $V_{os}(\text{max})$ = 6 mV and $I_{os}(\text{max})$ = 200 nA, specify suitable resistances for:

a. A_s = 5 V/V, and [16 marks]

b. A_s = 100 V/V. [16 marks]



Solution

a. As we want the gain of the amplifier circuit to be:

$$A_s = 1 + \frac{R_2}{R_1} = 5$$

So, the values of the resistors are calculated from:

$$R_2 = 4R_1$$

Pick R_1 = 25.5 kΩ, 1%, and R_2 = 102 kΩ, 1%.

Then, the value of resistor R_p is:

$$R_p = R_1 \parallel R_2 = 25.5\ \text{k}\Omega \parallel 102\ \text{k}\Omega$$

As a result, the value of resistor $R_p \cong 20\ \text{k}\Omega$.

Moreover, the error voltage at the output is:

$$\begin{aligned} E_O(\max) &= \left(\frac{1}{\beta}\right) E_I(\max) \\ &= 5[6\ \text{mV} + (20\ \text{k}\Omega)(200\ \text{nA})] \\ &= 50\ \text{mV} \end{aligned}$$

To balance this out, we need:

$$V_X = \frac{E_O(\max)}{-\left(\frac{R_2}{R_1}\right)} = \frac{50}{-(4)} = -12.5\ \text{mV}$$

Pick a range of ± 15 mV, just to make sure.

To avoid upsetting A_s, choose $R_A \ll R_1$, say, R_A = 100 Ω.

Then, imposing

$$\frac{R_A}{R_A + R_B} = \frac{15\text{ mV}}{15\text{ V}}$$

This yields $R_B \cong 10^3 R_A$ = 100 kΩ.

Finally, let R_C = 100 kΩ as variable resistor for adjusting the accuracy.

b. Now, for the specified gain of 100 V/V.

$$A_s = 1 + \frac{R_2}{R_1} = 100$$

The values of resistors R_1 and R_2 are determined from:

$$R_2 = 99R_1$$

Let R_2 = 100 kΩ, so R_1 = 1010 Ω.

If we were to use R_A = 100 Ω as before, R_A would no longer be negligible compared to R_1.

So let R_1 = 909 Ω, 1%, and R_A = 1010 − 909 = 101 Ω (use 102 Ω, 1%), so that the series ($R_1 + R_A$) still ensures A_s = 100 V/V.

Moreover, let $R_p \cong$ 1 kΩ. Then, the error in the output voltage is:

$$E_O(\text{max}) = 100[6\text{ mV} + (1\text{ k}\Omega)(200\text{ nA})]$$
$$= 620\text{ mV}$$

And

$$V_X = \frac{E_O(\text{max})}{-\left(\frac{R_2}{R_1}\right)} = \frac{620}{-\left(\frac{105}{909}\right)} = -5.6\text{ mV}$$

Pick a range of ± 7.5 mV to make sure. Imposing

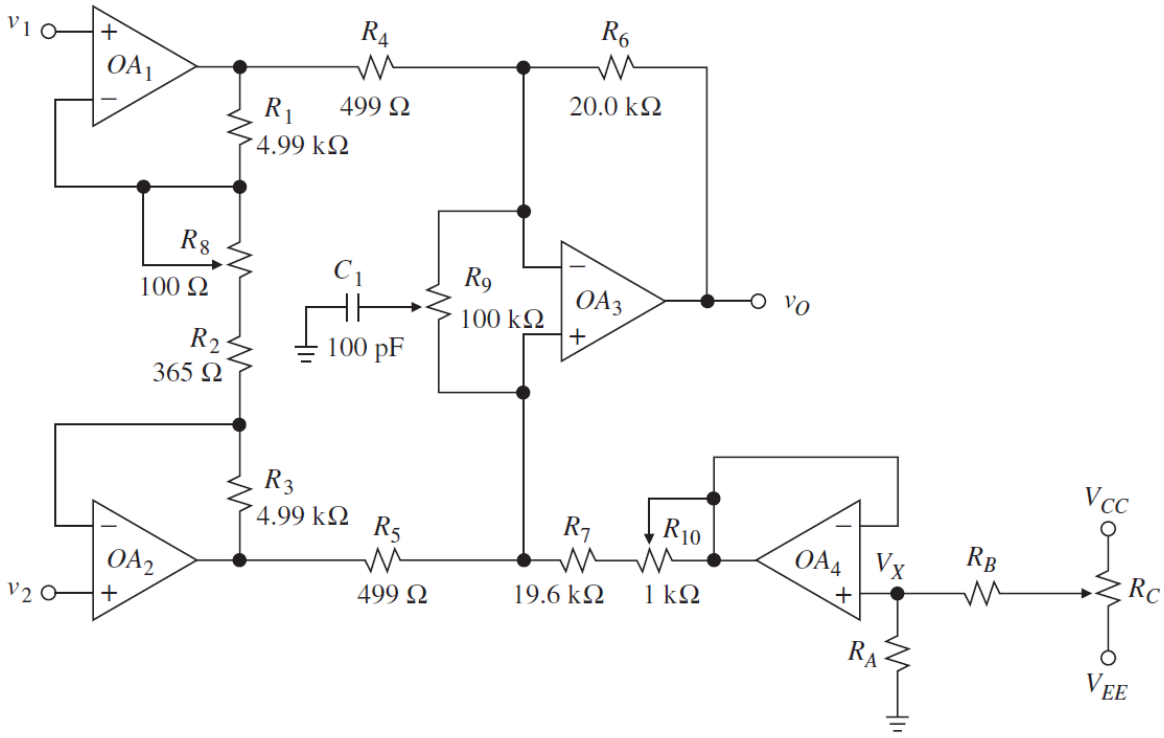
$$\frac{R_A}{R_A + R_B} = \frac{7.5\text{ mV}}{15\text{ V}}$$

This gives $R_B \cong 2000R_A \cong$ 200 kΩ.

Finally, let R_C = 100 kΩ as variable resistor for adjusting the accuracy.

Example for Tutorial 7 – Nulling Circuits 4

Specify R_A, R_B, and R_C in the figure below, given the following maximum ratings for the OP37C low-noise precision high-speed op amp at T = 25°C: I_B = 75 nA, I_{OS} = ±80 nA, and V_{OS} = 100 μV. Assume ±15 V supplies. [10 marks]



Solution

The error at the circuit due to first and second op amps is calculated from:

$$E_{I1} = E_{I2} = V_{OS} + \left[R_1 \parallel \left(R_2 + \frac{R_8}{2}\right)\right] I_B$$

$$= 10^{-4} + (5000 \parallel 208)(75 \times 10^{-9}) \cong 115\ \mu\text{V}$$

The error at the circuit due to the third op amp is calculated from:

$$E_{I3} = 10^{-4} + (500 \parallel 20{,}000)(80 \times 10^{-9}) \cong 139\ \mu\text{V}$$

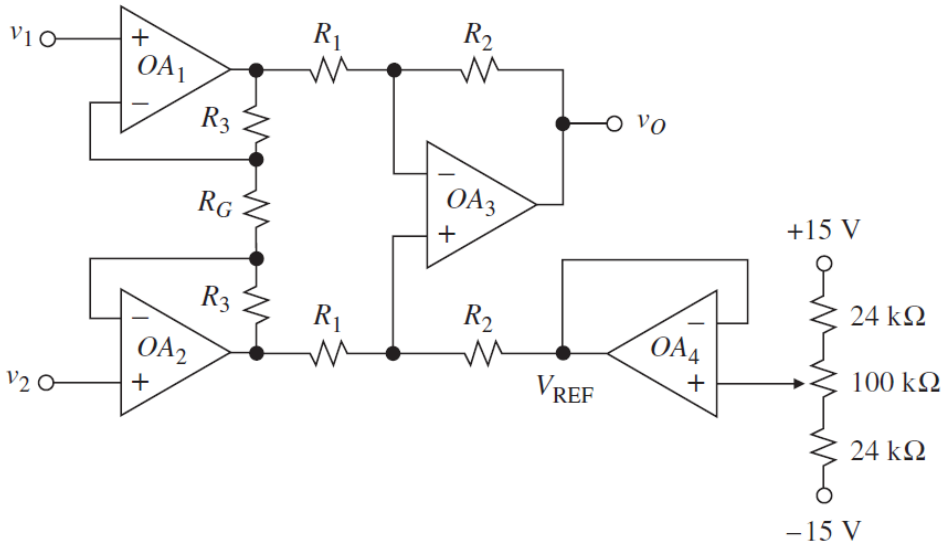
Using the superposition, the error in the output voltage is summed as contribution from as calculated above.

$$E_O = A(E_{I1} + E_{I2}) + \left(\frac{1}{\beta_3}\right) E_{I3}$$

$$= 10^3(2)(115) + \left(1 + \frac{20}{0.5}\right) 139$$

$$\cong 230\ \text{mV} + 5.7\ \text{mV} = 236\ \text{mV}$$

For a given instrumentation amplifier circuit with output offset control as shown below, the reference node is driven by voltage V_{REF}. This voltage, in turn, is obtained from the wiper of a pot and is buffered by OA4, whose low output resistance prevents disturbance of the bridge balance.



Applying the superposition principle, we obtain:

$$v_O = A(v_2 - v_1) + V_{REF}$$

Following the equation given above, for E_o = 236 mV as calculated above, we need −236 mV ≤ V_X ≤ +236 mV. In this example, use 300 mV to make sure.

Finally, choose the values for the resistors R_A = 2 kΩ, R_B = 100 kΩ, and R_C = 100 kΩ.

4.5.1. Monte Carlo Analysis and Test

A Monte Carlo analysis method is typically used to predict the probability of a variety of outcomes when the potential for random variables is present. It helps to explain the impact of risk and uncertainty in prediction and forecasting models in many areas of application from business, medicine, engineering and so forth. A Monte Carlo simulation requires assigning multiple values to an uncertain variable to achieve multiple results and then averaging the results to obtain an estimate.

4.5.1.1. Introduction to Monte Carlo Analysis in Electronics

In electronics, Monte Carlo is commonly employed for helping electronic engineers to perform analysis and design of devices and circuits. Typical applications of this method in electronics are estimating the operational limits of specific design or solution, simulating safe-operating-area of electronic systems and circuits, determining the tolerances of components and devices, and so on.

We have discussed to some extend in the previous sections in this chapter that most of static limitation parameters of the electronic component and device are influenced by the type, value and tolerance of the components and devices used in the circuit.

All components have tolerances, and some of these are very precise (resistors for instance), but other components can have very wide tolerances on their nominal values (e.g., wire wound inductors or

ferrites). In the event the tolerances on these components become too large, how can you predict how these tolerances will affect your circuits?

While you could calculate variations around nominal electrical values (voltage, current, or power) by hand, running these calculations by hand is very time consuming, especially in large circuits. However, these processes could be automated to some extends with the use of general purpose or specific ECAD software such as for example SPICE based simulators.

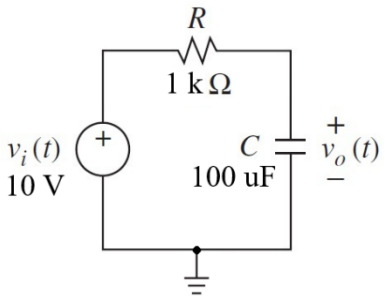
When a Monte Carlo simulation is used in SPICE, the simulation generates the component values in your circuit randomly using tolerances that you define. It then uses these randomly generated component values to run a standard SPICE simulation. This process is repeated multiple times (sometimes 100's of times) to give you a set of data describing how your circuit behaviour changes due to component tolerances.

4.5.1.2. Examples of Monte Carlo Analysis for Designing Circuit Component Values

We will investigate two examples of Monte Carlo analysis method for designing component values in the circuits. The first example uses a simple first-order RC circuit and use the method to determine the values of the component. The second example is about Monte Carlo simulation of a DC-DC step up Boost converter circuit.

Example for Tutorial 8 – Monte Carlo Analysis for RC Circuit

The diagram in the figure below shows a typical series RC circuit with R_1 = 1kΩ and C_1 = 100 µF.



In this circuit, the capacitor charges in a time dependent on the time constant i.e. the voltage is about 63% of the power supply after RC seconds. In this case, the voltage across the capacitor is 6.32 V after exactly $\tau = RC = (10^3)(10 \times 10^{-6}) = 0.01$ s. Perform Monte Carlo analysis for the circuit.

[32 marks]

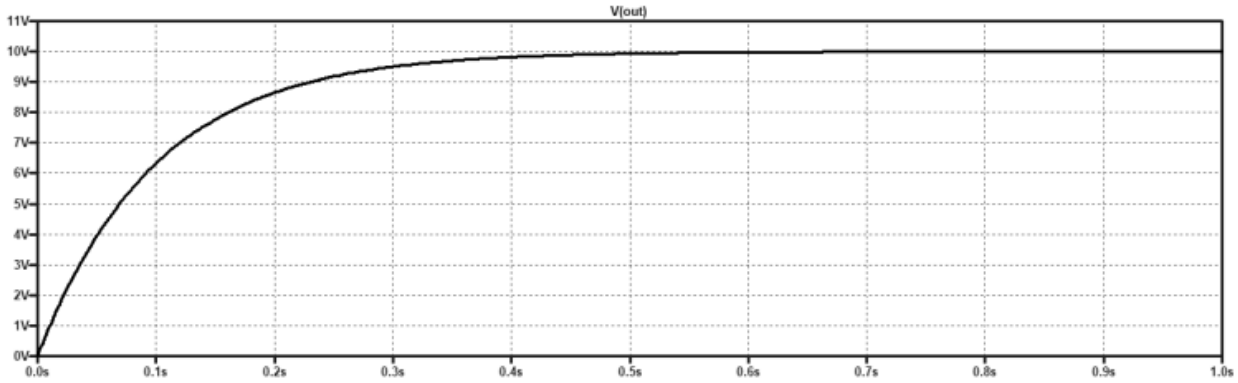
Solution

In this example, we assume that the values of all components are ideal, namely:

- Power supply voltage V_1 is 10 V.

- Resistor R_1 is 1000 Ω.
- Capacitor C_1 has a capacitance of 100 μF.

Since all the components have ideal values, even the graph produced is ideal and does not consider possible anomalies or variations. The market offers resistors with tolerances of 1%, 5%, 10% and others. Even capacitors might have characteristics that deviate from the plate data, with tolerances in the order of 20% or more. The battery may experience a decrease or increase in voltages for various reasons.



For all these reasons, the designer needs to obtain a "more realistic" graph that considers the real variations in the value of the components used, bringing the simulation behaviour closer to that of a real system.

That is why we really want the value of the components not to be ideal but real, with the following tolerances:

- Battery V_1: 10 V with 2% tolerance.
- Resistor R_1: 1000 Ω with 10% tolerance.
- Capacitor C_1: 100 μF with 25% tolerance.

This means that the electronic components used could assume the following ranges of values:

- Battery V_1: voltage between 9.8 V and 10.2.
- Resistor R_1: resistance value between 900 Ω and 1100 Ω.
- Capacitor C_1: capacitance between 75 μF and 125 μF.

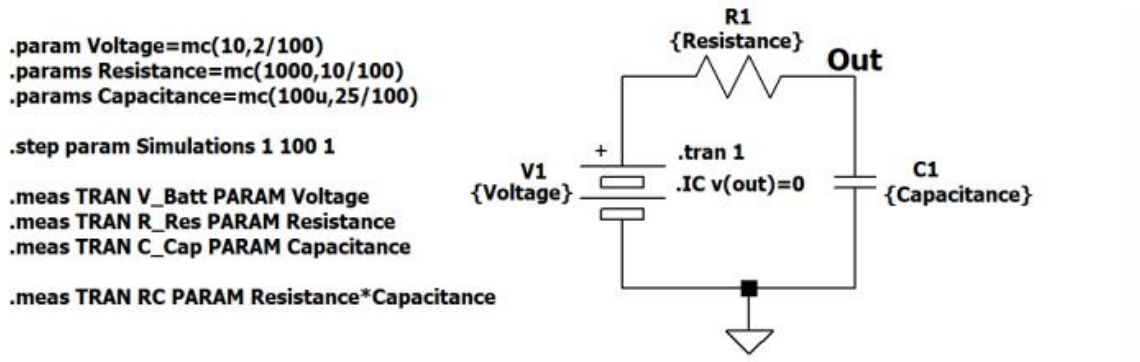
The variations obviously occur simultaneously. The possible values of combinations are in theory infinite, but designers need to observe a graph of the capacitor charge with as many variations as possible, in the natural range provided by the tolerances.

```
mc(value,tolerance)
```

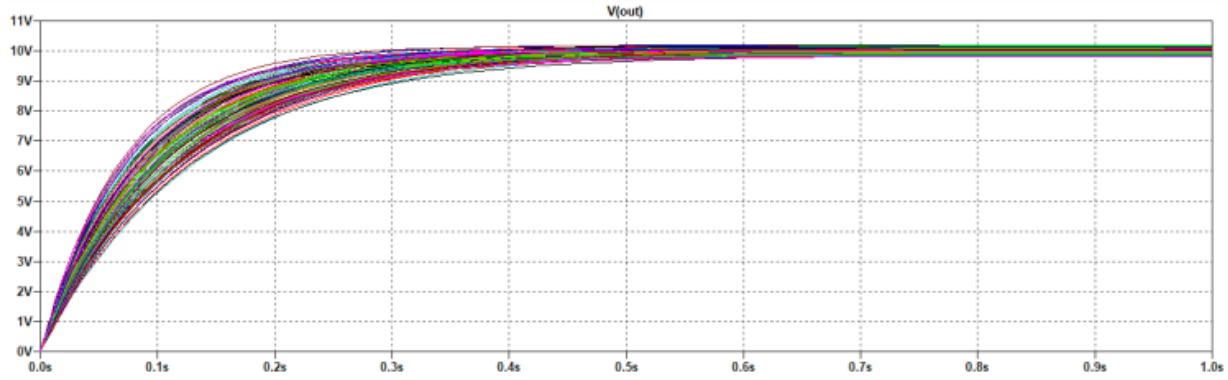
The function above randomly generates a random value between `x*(1+y)` and `x*(1-y)`, as specified within the tolerance range, with a uniform distribution. The Spice directives to be included in the LTspice schematic diagram are as follows:

```
.param Voltage = mc(10,2/100)
.param Resistance = mc(1000,10/100)
.param Capacitance = mc(100u,25/100)
.step param Simulations 1 100 1
.meas TRAN V_Batt PARAM Voltage
.meas TRAN R_Res PARAM Resistance
.meas TRAN C_Cap PARAM Capacitance
.meas TRAN RC PARAM Resistance*Capacitance
```

The simulation of the scheme (as shown in the below) is performed one hundred times. It generates a hundred different values for each component. It is advisable to carefully observe the diagram, the values of the components and the directives to have an in depth understanding of the procedure and be able to continue reading the article.



As you can see, this time the graph includes several curves, corresponding to the increasing voltage on the capacitor, with one hundred different component values. The more simulations are carried out, the more realistic the final curve will be, remember that the simulation time increases proportionally to the number of steps performed. Sometimes, if the circuit is extremely complex and made up of many components, the simulator takes a long time to perform the mathematical calculations.



In the table below, you will find some values of the hundred voltages, resistances and capacities generated by the program. Obviously, these are random values generated by the software, so for further simulations, they will always be different.

Simulation	Battery (V)	Resistance (Ohm)	Capacitance (uF)	RC Constant (S)
1	9.87732	1012.72	75.0626	0.0760171
2	9.99195	1017	115.437	0.1174
3	10.1291	1079.19	92.5146	0.099841
4	10.1436	934.822	112.33	0.105009
5	9.9216	1002.71	110.525	0.110824
6	9.94578	918.281	75.7492	0.069559
7	10.1954	933.18	82.3656	0.0768619
8	9.80187	923.817	97.2846	0.0898731
9	10.0127	975.576	75.4456	0.0736029
10	10.0429	1020.35	103.559	0.105667
.....	.....	.....	.....	.....

The following results show the minimum and maximum values of the randomly generated quantities, with reference to the hundred simulations:

Battery V_1:

- Minimum Monte Carlo voltage generated: 9.80065 V.
- Maximum Monte Carlo voltage generated: 10.1999 V.

Resistor R_1:

- Minimum Monte Carlo resistance value: 901.75 Ω.
- Maximum Monte Carlo resistance value: 1099.36 Ω.

Capacitor C_1:

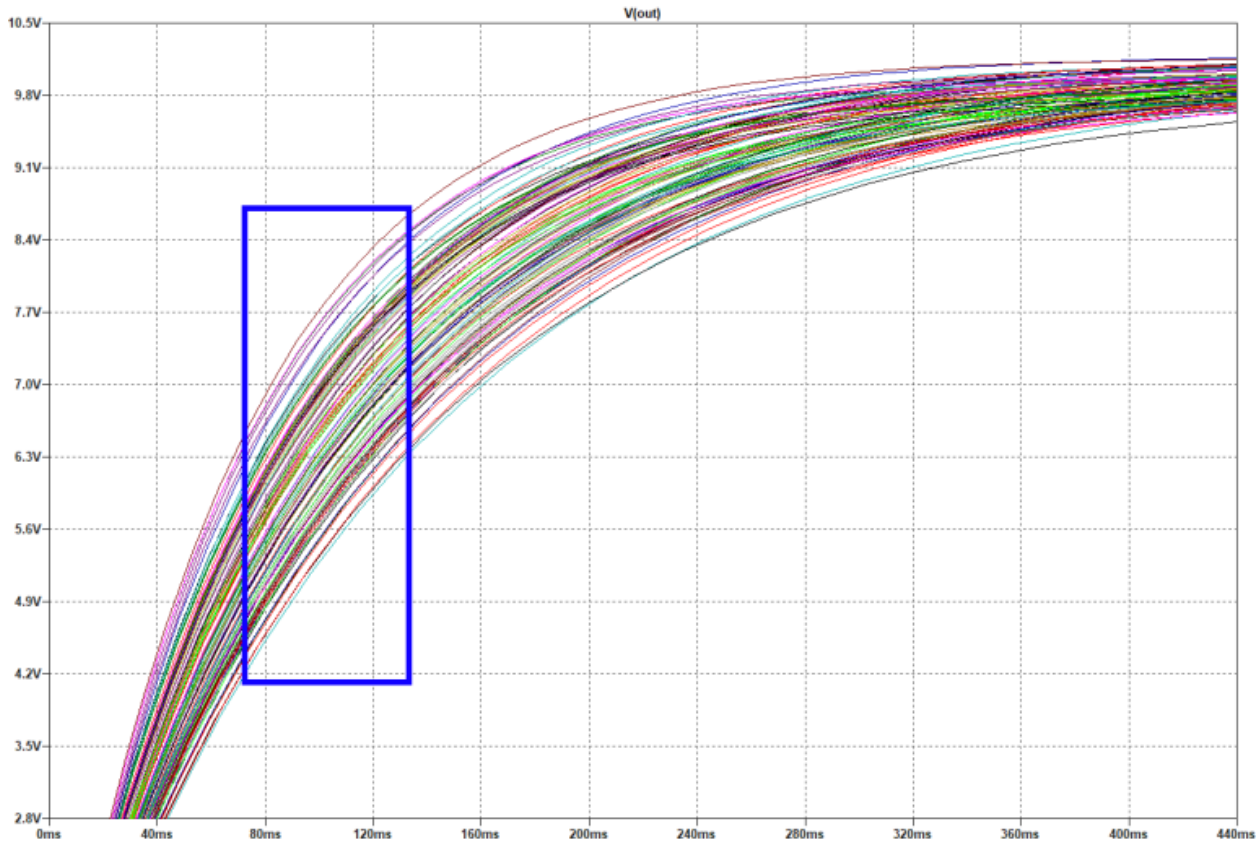
- Minimum Monte Carlo capacity: 75.0626 uF.
- Maximum Monte Carlo capacity: 124,759 uF.

Circuit time constant, RC:

- Minimum “t”: 0.069559 second.
- Maximum “t”: 0.13325 second.

In the figure below, we can see what happens in the graph of the voltage on the capacitor, precisely in the time interval between 0.069559 and 0.13325 second, with 100 Monte Carlo simulations performed.

The variation of the components in different contexts makes us understand how they can influence and modify the behaviour of an electronic circuit and its timing.



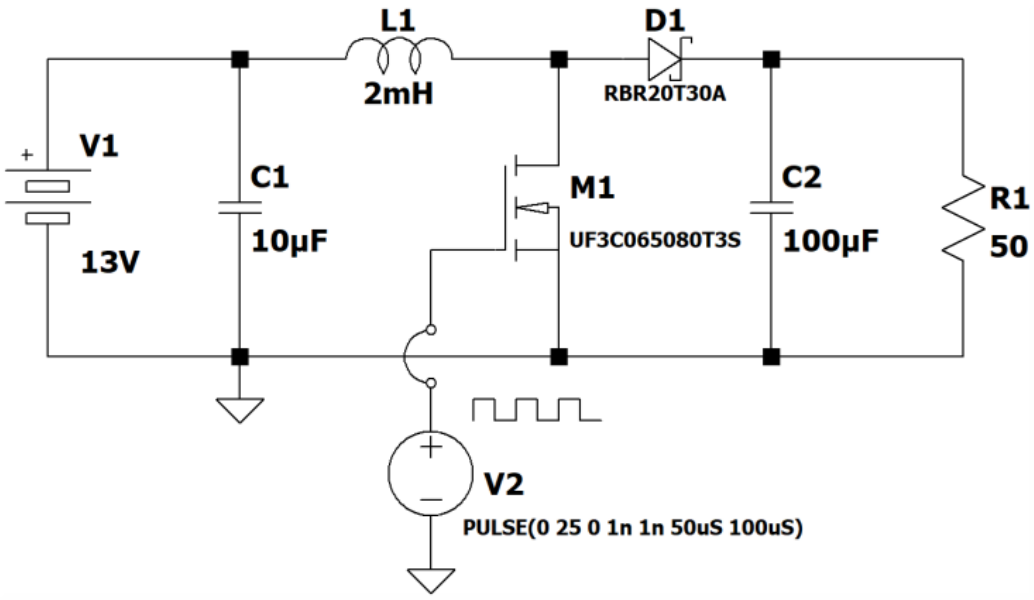
Example for Tutorial 9 – Monte Carlo Analysis for DC-DC Converter Circuit

In DC-DC converters, the most important power loss is due to the ON and OFF switching transition. The losses are proportional to the switching frequency and the parasitic capacitance values. The circuit for this example is a step-up Boost converter.

The MOSFET transistor used for switching are of primary importance for analysis and design of the circuit, especially the $R_{ds}(\text{on})$ parameter and the switching speed. The Boost converter shown in figure below consists of the following components:

- 13 V generator V_1 which can be a battery or a voltage source.
- 2 mH inductor.
- UF3C065080T3S SiC MOSFET.
- Power Schottky diode (i.e. RBR20T30A).
- 50 Ω load.
- 10 µF and 100 µF capacitor.

Also, this Boost converter operates with a switching frequency f = 10 kHz with the pulse generator as specified i.e. `PULSE (V1 V2 Tdelay Trise Tfall Ton Tperiod Ncycles).`



The components are not real therefore we can easily admit the following tolerances: V_1: ± 20%, C_1: ± 25%, L_1: ± 15%, C_2: ± 25%, R_1: ± 5%, and temperature: ± 30%. Perform Monte Carlo analysis of the DC-DC converter. [20 marks]

Solution

The SPICE directives and commands in the LTspice to be included in the diagram are the following:

```
.param Voltage = mc(13,20/100)
.param Cap1 = mc(10u,25/100)
.param Induct = mc(2m,15/100)
.param Cap2 = mc(100u,25/100)
.param Load = mc(50,5/100)
.param T = mc(27,30/100)
.temp {T}
.step param Simulations 1 10 1
.meas TRAN V_Batt PARAM Voltage
.meas TRAN Capacitor1 PARAM Cap1
.meas TRAN Inductor PARAM Induct
.meas TRAN Capacitor2 PARAM Cap2
.meas TRAN Resistor PARAM Load
```

```
.meas TRAN Temperature PARAM T
```

For a short but comprehensive simulation, we have provided only ten random generations of values within the respective tolerances. Remember that the higher the number of simulations, the better the result.

In the table and figure below, we can see the simulation of ten different operating conditions (i.e. it lasted for about 15 minutes and generated a temporary file on the computer's hard disk of 1.3 GB). The following table shows the values of the components generated by the Monte Carlo method, in any case within the declared tolerance.

Sim	V_batt (V)	Capacitor1 (uF)	Inductor (mH)	Capacitor2 (uF)	Resistor (Ohm)	Temperature (°C)
1	12.8953	10.425	2.18524	84.6652	50.3179	18.9203
2	11.6237	9.8104	1.7854	101.968	52.1286	34.3856
3	14.575	9.62577	1.83506	82.5777	49.3067	28.173
4	10.5825	11.6734	1.92069	81.151	49.8765	30.595
5	12.1488	8.9304	2.26464	90.7033	51.2156	20.6808
6	15.5897	9.78721	2.29711	83.9175	49.1797	21.9771
7	11.1754	11.5226	2.11467	106.019	50.5602	30.9001
8	13.1278	11.4248	1.73944	81.3616	52.22	23.7609
9	14.265	8.15813	1.92455	83.829	50.6542	34.3826
10	11.5729	10.2403	1.88137	103.668	49.639	19.9719

The figure below shows a Monte Carlo simulation of the Boost converter behaviour, which shows the voltage on the load depending on the different values of the electronic components.

