XMUT303 Analogue Electronics

Final Exam Revision Questions (Solution)

A. Operational Amplifier

1. Given in the figures shown below (a) a non-inverting amplifier and (b) a circuit model for its analysis.

   a. Derive an expression for the output voltage (V_O) of the amplifier with a finite op amp open-loop gain (a). [10 marks]

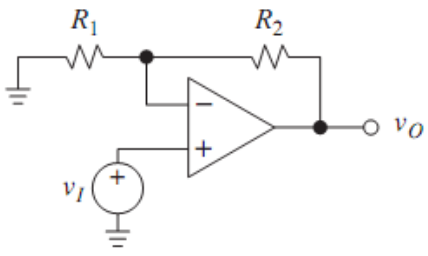
   b. Let V_I = 1 V, R_1 = 2 kΩ, and R_2 = 18 kΩ. Find V_O if:

      i. Gain a = 10^2 V/V. [2 marks]

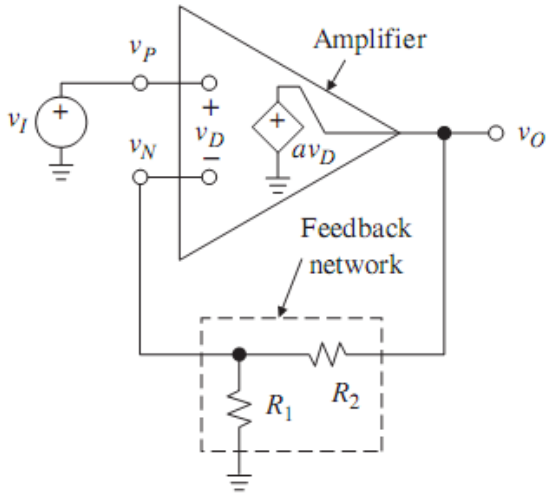
      ii. Gain a = 10^4 V/V. [2 marks]

      iii. Gain a = 10^6 V/V. [2 marks]

   c. Comment on your findings in part (b). [2 marks]



(a)



(b)

Solution

a. For non-inverting amplifier as given in the circuit above, by inspection we know:

$$V_P = V_I \qquad (Eq.\,1)$$

Using voltage divider formulae, this yields:

$$V_N = \left(\frac{R_1}{R_1 + R_2}\right) V_O \qquad \text{or} \qquad V_N = \left(\frac{1}{1 + R_2/R_1}\right) V_O \qquad (Eq.2)$$

Letting a as the open-loop gain of the op amp, the output voltage of the amplifier is:

$$V_O = a(V_P - V_N) \qquad (Eq.3)$$

We get as follows when you substitute V_P and V_N in equation (3) with equations (1) and (2).

$$V_O = a\left(V_I - \frac{1}{1 + R_2/R_1} V_O\right)$$

Collecting terms and solving for the ratio of V_I/V_O which is designated as A_v and rearrangement of the equation, the transfer function of the amplifier becomes:

$$A_v = \frac{V_O}{V_I} = \left(1 + \frac{R_2}{R_1}\right) \frac{1}{1 + (1 + R_2/R_1)/a}$$

b. By using the equation given in (a) and let V_I = 1 V, R_1 = 2 kΩ, and R_2 = 18 kΩ, this gives:

$$\frac{V_O}{1} = \left(1 + \frac{18}{2}\right) \times \left(\frac{1}{(1 + 18/2)/a}\right) \qquad \text{or} \qquad V_O = \frac{10}{(1 + 10/a)}$$

So

i. For a = 10^2 V/V:

$$V_O = \frac{10}{(1 + 10/10^2)} = 9.091$$

ii. For a = 10^4 V/V:

$$V_O = \frac{10}{(1 + 10/10^4)} = 9.990$$

iii. For a = 10^6 V/V:

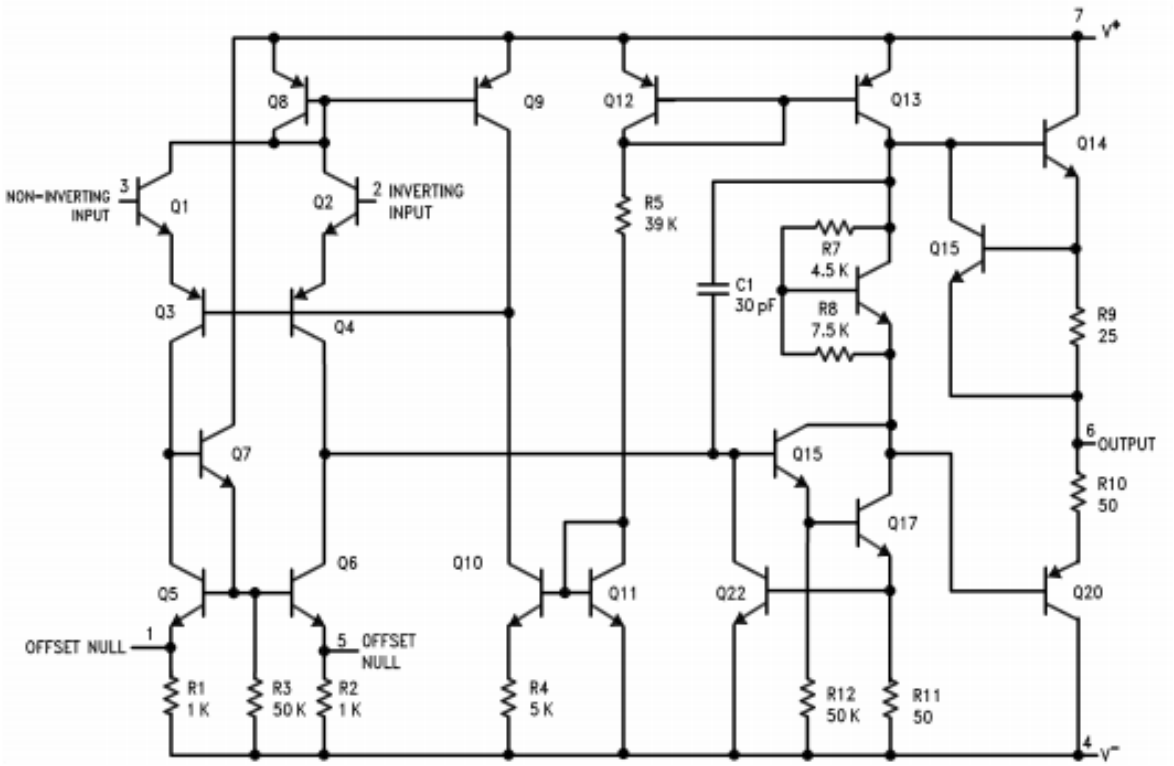
$$V_O = \frac{10}{(1 + 10/10^6)} = 9.9999$$

c. The higher the op amp open loop gain (a), the closer the output voltage (V_O) is to 10.0 V.

2. Given in the figure below is an internal schematic of LM741 op amp.

a. Describe the main features of inside the op amp internal circuit. [4 marks]

b. What is the role of capacitor C_1 in the circuit? [2 marks]



Solution

a. There are a number of features/functionalities inside the internal circuitry of LM741 for realising a working operational amplifier:

- Reference current bias – Reliable reference current at working condition and set up.
- Input stage bias – Current mirror for precise biasing.
- Input stage – Differential inputs.
- First output stage – Cascaded amplifier.
- Second output stage – Class AB amplifier.
- Short circuit protection – Prevent short circuit at the output.

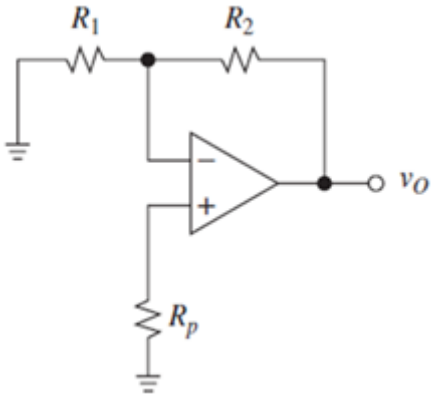
b. The capacitor C_1 inside second gain stage in the internal circuitry of the op amp is used for providing compensation.

Due to parasitic capacitance of the op amp, the frequency response of the op amp tends to roll off at low frequency which could result in small gain at the working frequency range.

This capacitor creates a desired dominant-pole behaviour in the open loop transfer function of the op amp that would extend the availability of the useable bandwidth for the op amp.

B. Op Amp Analysis

3. For a given practical non-inverting amplifier given in the figure below:



a. What is input offset voltage in the op amp? [2 marks]

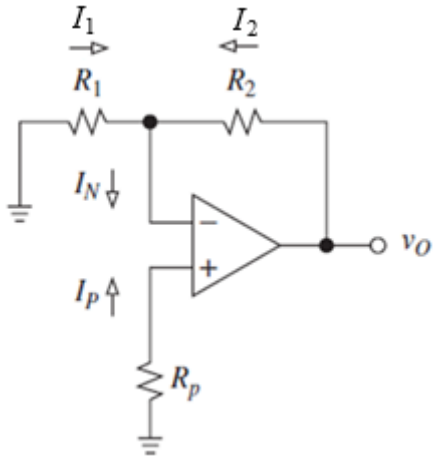
b. Derive the equation for determining the output voltage of the amplifier circuit. Take into account the typical offset voltage and bias current that exist in the op amp circuit. [16 marks]

c. Describe how bias current causes errors in the amplifier circuit. [4 marks]

Solution

a. The input offset voltage is defined as the voltage that must be applied between the two input terminals of the op amp to obtain zero volts at the output. Ideally the output of the op amp should be at zero volts when the inputs are grounded.

b. The current flowing through R_p generates a voltage across this resistor (V_p).



The convention of current flow we have adopted means that V_P must be less than zero.

$$V_p = -R_P I_P \qquad (1)$$

For ideal op amp, voltage at the inverting pin is equal to non-inverting pin:

$$V_N = V_p \qquad (2)$$

Because of the virtual short between the terminals of the op-amp, $V_N = R_p I_p$ also, now.

$$I_1 = -\frac{V_N}{R_1} = -\left(\frac{R_P}{R_1}\right) I_P \qquad (3)$$

Then $I_N = I_2 + I_1$ as a result:

$$I_2 = I_N - I_1 \qquad (4)$$

Assigning equation (3) into equation (4) will yield:

$$I_2 = I_N - I_1 = I_N + \left(\frac{R_p}{R_1}\right) I_p \qquad (5)$$

At the inverting input node (V_N), we know that $V_o - V_N = R_2 I_2$. Rearrange the equation:

$$V_O = V_N + R_2 I_2 \qquad (6)$$

For the given non-inverting amplifier, by considering equation (2), then put equation (5) into equation (6):

$$\begin{aligned} V_o &= V_p + R_2 \left(I_N + \frac{R_p}{R_1} I_p\right) \\ &= I_p R_p + R_2 I_N + I_p R_p \left(\frac{R_2}{R_1}\right) \\ &= \left(1 + \frac{R_2}{R_1}\right) I_p R_p + R_2 I_N \\ &= \left(1 + \frac{R_2}{R_1}\right) V_p + R_2 I_N \end{aligned}$$

c. The following rationales are explanations on how bias current causes error in the amplifier circuit:

- First, in spite of the absence of any input signal, the circuit yields some output voltage E_o. We regard this unwanted output as an error or, more properly, as output dc noise.
- Second, the circuit produces E_o by taking an input error, or input dc noise, and amplifying it by $(1 + R_2/R_1)$, which is aptly called the dc noise gain (recall that this gain is the reciprocal of the feedback factor β, hence the reason for calling $1/\beta$ the noise gain).
- Third, the input error consists of two terms, namely, the voltage drop $-R_p I_p$ due to I_p flowing out of R_p, and the term $(R_1 \parallel R_2) I_N$ arising as if I_N flew out of the parallel

combination $R_1 \parallel R_2$ (e.g. R_1 and R_2 are not in parallel per se, but they only appear as such as they conspire with I_N to create the corresponding error term).

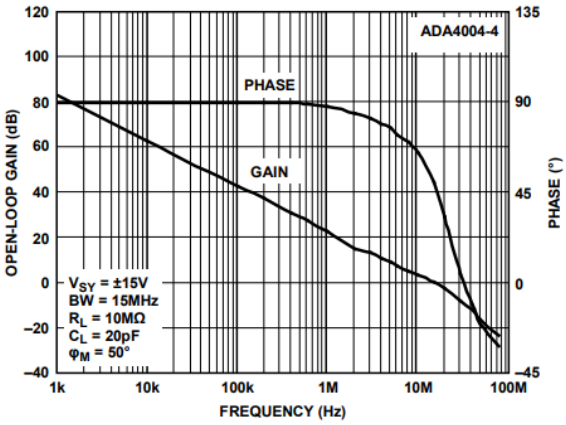
- Fourth, the two terms in the third part tend to compensate for each other since they have opposite polarities.

4. In case of ADA4004 op amp with its GBP is 12 MHz, the frequency response of the given op amp is shown below (note that measurement is taken when supply voltage V_{supply} is $\pm$15 V).

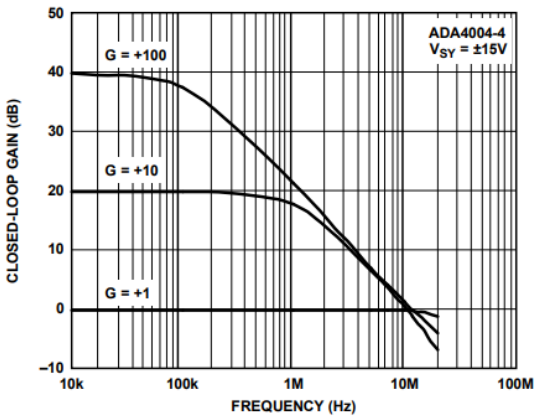
   a. Determine the bandwidth of the op amp at a gain of 1. [2 marks]

   b. Calculate the bandwidth of the op amp if the open loop gain is 500,000 maximum. [2 marks]

   c. Define the full-power bandwidth of the op amp. Determine full power bandwidth of the ADA4004 op amp if its slew rate is 2.7 V/µs and a closed loop gain of 100. [2 marks]



Open-Loop Gain and Phase vs. Frequency



Closed-Loop Gain vs. Frequency

Solution

For the given ADA4004 op amp:

a. At a gain of 1 (e.g. a gain in dB = 0 dB), the bandwidth of the op amp is 12 MHz.

b. Its open loop gain (maximum) of 500,000, the bandwidth of the given op amp is (e.g. op amp open loop cut off frequency):

$$\text{Bandwidth} = \frac{GBP}{Acl} = \frac{12\ \text{MHz}}{5 \times 10^5} = 24\ \text{Hz}$$

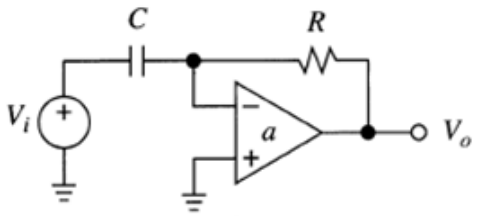
c. The full power bandwidth of the op amp is the frequency range where op amp can swing through its maximum output range without suffering slew rate limitations. It is a range of

frequencies where the op amp has the most gain.

The full-power bandwidth (ω_{FPB}) of the given op amp is:

$$\omega_{FPB} = \frac{SR}{A_{max}} = \frac{2.7 \times 10^6}{100} = 27 \text{ KHz}$$

5. For a given differentiator circuit as shown below, its rate of convergence (ROC) by design is found to be 40 dB/decade.



a. What is rate of convergence (ROC)? [2 marks]

b. Design a pole compensation that will stabilize the given differentiator circuit. [4 marks]

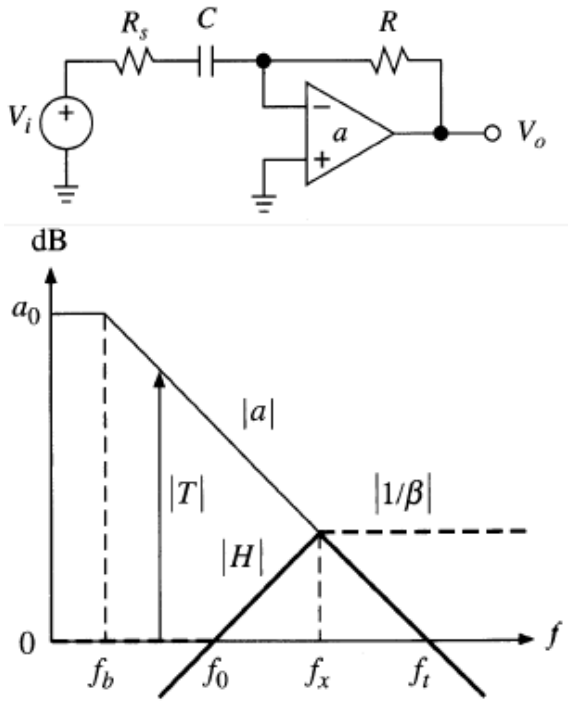
c. Determine the value of compensating resistor as in part (a) if R = 10 kΩ, the frequency of pole compensation is 100 kHz, and the open loop bandwidth of the op amp is 2 MHz. [4 marks]

Solution

a. Rate of convergence (ROC) is an analysis method for determining the stability of op-amp based circuit. It uses the result of measurement of the open loop and feedback loop gains of the op amp circuit. The ROC of a given op amp circuit is determined from (e.g. a is open loop gain of op amp and β is the feedback loop gain of op amp circuit):

$$\text{ROC} = |da - d(1/\beta)|$$

b. Since a differentiator has ROC 40 dB/decade, to stabilize this we add a zero to β (or a pole to $1/\beta$). We place this pole at the frequency where the $1/\beta$ curve crosses the a curve. This will result in a ROC of 30 dB/decade and hence a more stable system.



c. Since $f_x = \sqrt{f_0 f_t}$, we find the appropriate R_s by setting $R_s C = 2\pi f_x$.

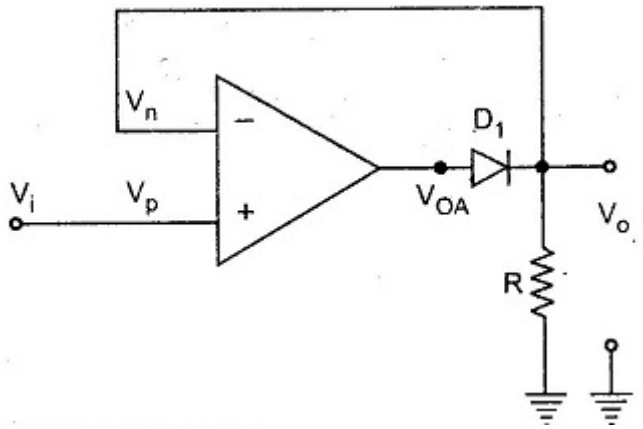
It can be shown that this results in:

$$R_s \approx \frac{R}{\sqrt{\frac{f_t}{f_0}}} = \frac{10 \times 10^3}{\sqrt{\frac{2 \times 10^6}{100 \times 10^3}}} = 2.2\text{k}\Omega$$

If extra phase margin is desired, then the pole can be shifted further to the left.

C. Op Amp based Circuits

6. In the figure below is a precision half-wave rectifier circuit. It consists of non-inverting amplifier with diode D_1 in the feedback loop of an op-amp.



a. Describe why the op-amp based rectifier circuit provides a more precise rectification compared with diode-based rectifier circuit. [4 marks]

b. Describe the operation of the given circuit. The analysis of this circuit can be done considering two distinct cases of $V_i > 0$ V and $V_i < 0$ V. [4 marks]

c. Draw the waveform of the input and output of the circuit and also the output voltage-input voltage transfer function graph of its operation. [2 marks]

Solution

a. In a typical diode-based rectifier circuit, we use diodes to rectify AC to DC. But, this rectification method can only be used if the input voltage to the circuit is greater than the forward voltage of the diode which is typically 0.7 V.

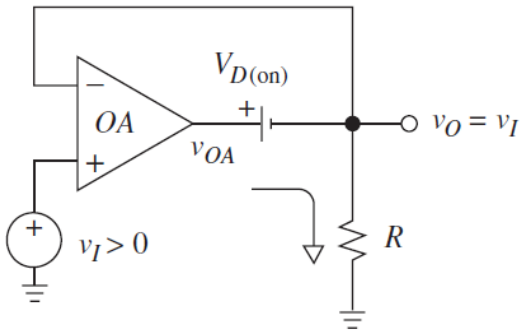
To overcome this issue, the precision rectifier circuit was introduced e.g. it is another rectifier that converts AC to DC, but in a precision rectifier we use an op-amp to compensate for the voltage drop across the diode. That is why we are not losing the 0.6 V or 0.7 V voltage drop across the diode, also the circuit can be constructed to have some gain at the output of the amplifier as well.

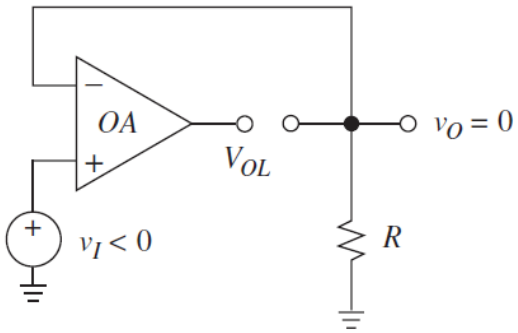
b. Description of operation of precision half-wave rectifier circuit.

Case 1: $V_i > 0$ V

For closed loop feedback op-amp $V_p = V_n$, due to virtual ground, when $V_i > 0$ V, op-amp tries to keep $V_o = V_n = V_p = V_i$ and it does this because forward biasing diode provides closed loop feedback path.

The voltage drop across forward bias diode $V_d(on)$ is 0.7 V. To accommodate the voltage drop across the diode, the op-amp swings about 0.7 V higher than V_o.



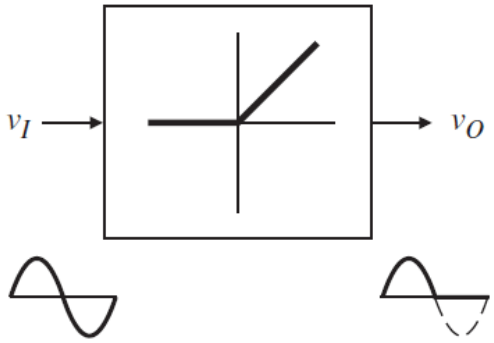


Case 2: $V_i < 0$ V

When $V_i < 0$ V, diode D_1 is reverse biased and the op-amp is working in the open loop. Therefore, op-amp is no longer capable of keeping $V_n = V_p$.

With no current through resistance R we have $V_o = 0$. The op-amp output V_{oA} is saturated at V_{sat} .

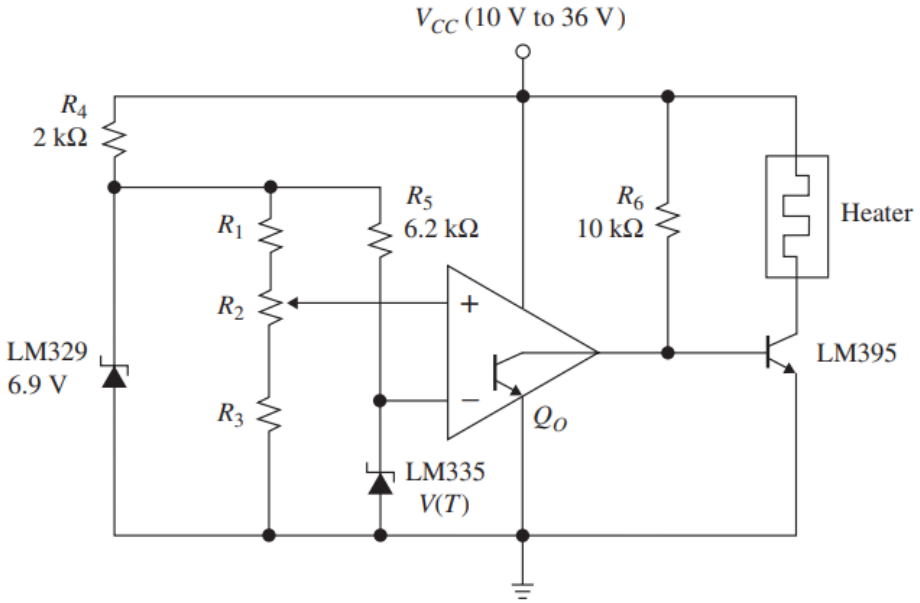
c. The input and output waveforms of the precision half-wave rectifier circuit and its quadrant of operation are given in the figures below.



7. Referring to the on-off temperature controller circuit of figure given below, specify suitable resistances so that the set point can be adjusted anywhere between 50°C and 100°C by means of a 5 kΩ potentiometer. From datasheet of LM335, its temperature coefficient is given as 10 mV/°K (note: that for temperature conversion 0°K = 273.2°C).

The circuit is designed as a comparator circuit using an op amp that drives a power transistor (LM395) for turning on and off of the heater. Notice also the roles of Zener diode (LM335) that provides reference voltage and Zener diode (LM329) for limiting the voltage range. The variable resistor R_2 is provided for fine tuning of the voltage setting of the comparator circuit.

[10 marks]



Solution

For the given op-amp based voltage comparator circuit:

Voltage at 50°C is:

$$V_{(50°\text{C})} = \frac{273.2° + 50°}{100°} = 3.232\ \text{V}$$

Voltage at 100°C is:

$$V_{(100°\text{C})} = \frac{273.2° + 100°}{100°} = 3.732\ \text{V}$$

Since the value R_2 is equal to 5 kΩ, the current that flows through R_2 is:

$$I_2 = \frac{3.732\ \text{V} - 3.232\ \text{V}}{5\text{k}} = 0.1\ \text{mA}$$

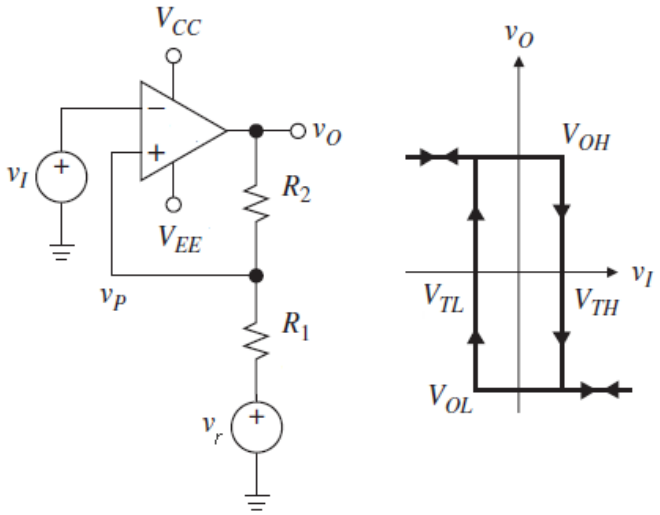
Consequently, the value of resistor R_3 is:

$$R_3 = \frac{3.232\ \text{V}}{0.1\ \text{mA}} = 32.3\ \text{k}\Omega\ (\text{e.g. use } 32.4\ \text{k}\Omega, 1\%)$$

The value of resistor R_1 is:

$$R_1 = \frac{6.9\ \text{V} - 3.732\ \text{V}}{0.1\ \text{mA}} = 31.7\ \text{k}\Omega\ (\text{e.g. use } 31.6\ \text{k}\Omega, 1\%)$$

8. Given in the figure below is a typical Schmitt trigger circuit along with its voltage transfer characteristic graph.



a. Given the output voltage saturated to the supply voltage $= \pm 10$ V. Derive the equations for high-threshold and low-threshold values for V_{TL} = 2 V and V_{TH} = 3 V. [6 marks]

b. Specify suitable resistances of the resistors (R_1 and R_2) and reference voltage (V_r). [24 marks]

Solution

a. By considering that V_{TL} = 2 V and V_{TH} = 3 V for the given Schmitt trigger, use a reference voltage source V_r to make polarity of V_{TL} and V_{TH} same (note: for V_{TL} and V_{TH} with opposite polarity, there is no need of V_r).

V_{sat} = 10 V and therefore $V_{out} = \pm 10$ V

Use superposition theorem to create the following equations:

For the high threshold point (V_{TH}):

$$V_{TH} = V_{sat}\left(\frac{R_1}{R_1 + R_2}\right) + V_r\left(\frac{R_2}{R_1 + R_2}\right)$$

For the lower threshold point (V_{TL}):

$$V_{TL} = -V_{sat}\left(\frac{R_1}{R_1 + R_2}\right) + V_r\left(\frac{R_2}{R_1 + R_2}\right)$$

b. Choose R_2 = 22 kΩ and solve the above equations for R_1 and V_r, we get the following equations for the given Schmitt trigger circuit:

Equation for high threshold point (V_{TH}):

$$\frac{10R_1}{R_1 + 22\ \text{k}\Omega} + \frac{V_r(22\ \text{k}\Omega)}{R_1 + 22\ \text{k}\Omega} = 3$$

Solving the above equation

$$10R_1 + V_r(22\ \text{k}\Omega) = 3(R_1 + 22\ \text{k}\Omega)$$

So, the equation for the V_{TH} is:

$$7R_1 + V_r(22\ \text{k}\Omega) = 66\ \text{k}\Omega \qquad (Eq.1)$$

Equation for low threshold point (V_{TL}):

$$\frac{-10R_1}{R_1 + 22\ \text{k}\Omega} + \frac{V_r(22\ \text{k}\Omega)}{R_1 + 22\ \text{k}\Omega} = 2$$

Solving the above equation

$$-10R_1 + V_r(22\ \text{k}\Omega) = 2(R_1 + 22\ \text{k}\Omega)$$

So, the equation for the V_{TL} is:

$$-12R_1 + V_r(22\ \text{k}\Omega) = 44\ \text{k}\Omega \qquad (Eq.2)$$

Solving the equations Eq.1 and Eq.2, we can find the value for R_1

$$7R_1 + V_r(22\ \text{k}\Omega) = 66\ \text{k}\Omega$$

$$-12R_1 + V_r(22\ \text{k}\Omega) = 44\ \text{k}\Omega$$

Subtracting the top part with the second part in the bottom, this yields the value of R_1

$$7R_1 - (-12R_1) = 66\ \text{k}\Omega - 44\ \text{k}\Omega$$

Thus

$$R_1 = \frac{22\ \text{k}\Omega}{19} = 1.15\ \text{k}\Omega$$

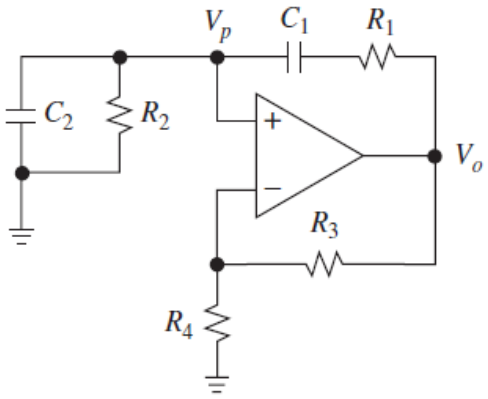
For R_1= 1.15 kΩ (e.g. choose E24 standard value of 1.2 kΩ).

And the value of reference voltage, V_r is determined as follow:

$$V_r = \frac{[66\ \text{k}\Omega - 7(1.15\ \text{k}\Omega)]}{22\ \text{k}\Omega}$$

As a result, the reference voltage, V_r = 2.6 V.

9. For a given Wien-Bridge oscillator circuit as shown below.



a. Determine the values of the components of the oscillator circuit when frequency of the oscillator f = 1 kHz and if the value of the capacitor is assumed to be 10 pF. Use E24 values standard (see Appendix). [6 marks]

b. Determine the values of the resistors R_3 and R_4. [4 marks]

Solution

a. Frequency of the oscillation is determined from the following equation for the Wien-Bridge oscillator:

$$f = \frac{1}{2\pi RC} \quad or \quad R = \frac{1}{2\pi fC}$$

Given that frequency of oscillation, f is 1 kHz and C = 10 pF, entering the values into the equation above.

$$R = \frac{1}{2\pi(1000)(10 \times 10^{-9})} = 15.9 \times 10^3$$

Thus, assign $R_1 = R_2 = 15\ \text{k}\Omega$ (e.g. to the nearest E24 standard value).

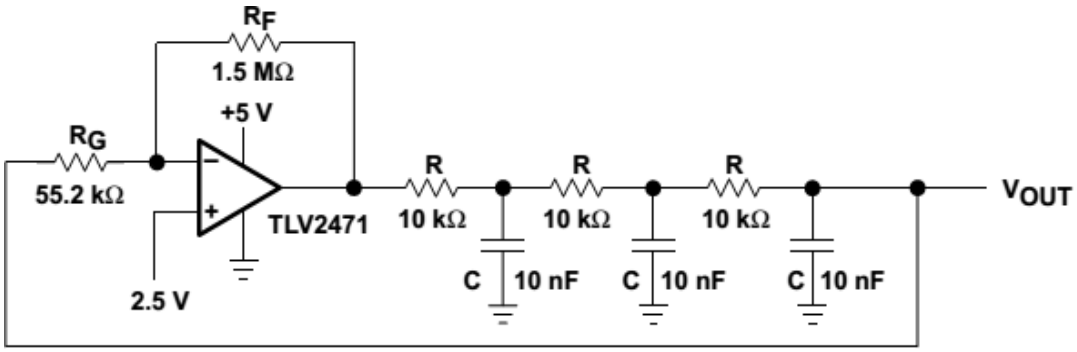
b. The gain of the amplifier in the Wien-Bridge oscillator is determined from:

$$1 + \left(\frac{R_3}{R_4}\right) = 3 \quad \text{or} \quad \frac{R_3}{R_4} = 2$$

Therefore, the values of the resistor $R_3 = 2R_4$ to meet the required condition of the oscillator.

Since $R_3/R_4 = 2$, so let $R_4 = 1\ \text{k}\Omega$ and $R_3 = 2\ \text{k}\Omega$ (e.g. use 4.7 kΩ potentiometer for fine corrections).

10. Given in the figure below is a single amplifier phase-shift oscillator circuit. The oscillator circuit is realised with TLV2471 op amp and relevant resistors and capacitors for amplifier and RC section circuits.



a. Describe the advantage of this type of oscillator compared with Wien-Bridge oscillator. [2 marks]

b. What is the phase angle for each of the RC section in the oscillator? Determine the frequency of oscillation for the above oscillator circuit. [4 marks]

c. Determine the gain of the oscillator to ensure constant amplitude oscillation. [6 marks]

Solution

a. This oscillator has less distortion from Wien-Bridge. This occurs when output distortion is very low e.g. -0.46 %, although this design is less popular these days.

b. The three RC sections of the oscillator are cascaded to get the steep slope between phase and resonant frequency. With the three RC sections, the angle for each section is -π/3.

$$\omega = 2\pi f = \frac{1.732}{RC} \qquad (\text{e.g. } \tan 60° = 1.732)$$

The frequency of the oscillation of the given oscillator circuit is:

$$f = \frac{1.732}{2\pi RC} = \frac{1.732}{2\pi \times (10 \times 10^3) \times (10 \times 10^{-9})} = 2.76\ \text{kHz}$$

c. Assuming that the RC stages do not load each other, the gain of feedback loop is:

$$\beta = \left(\frac{1}{sRC+1}\right)^3$$

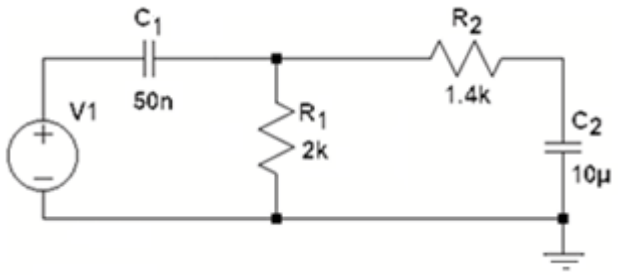
The magnitude of frequency response at oscillation frequency is:

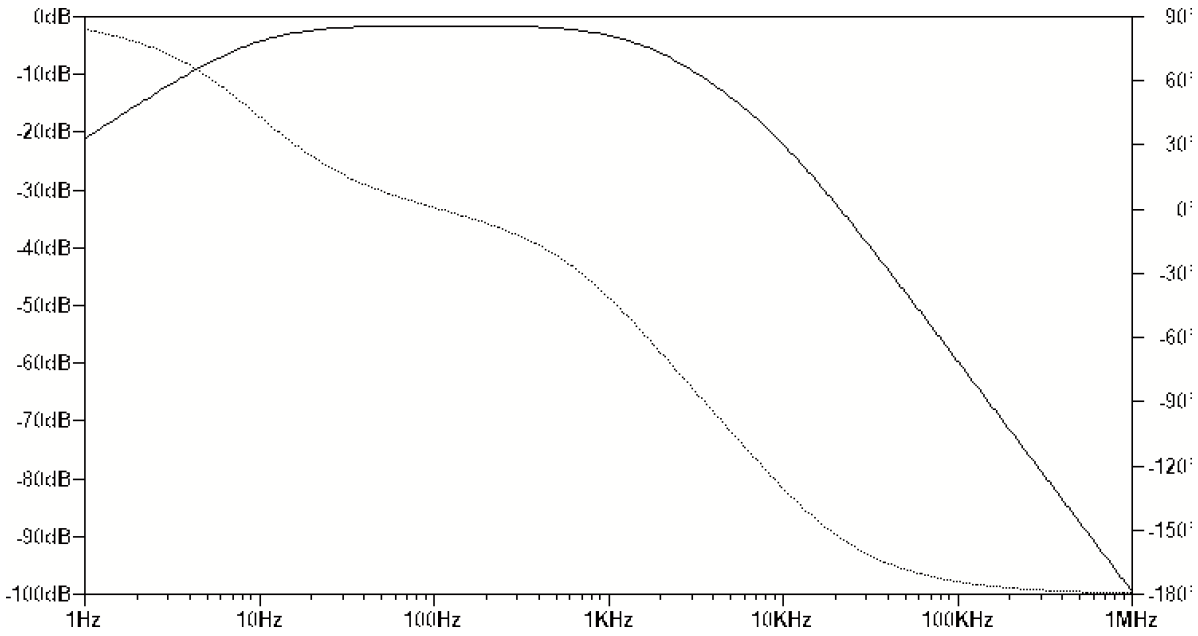
$$|\beta|_{s=\frac{j1.73}{RC}} = \left(\frac{1}{\left(\frac{j1.73}{RC}\right)RC+1}\right)^3 = \left(\frac{1}{2}\right)^3 = \frac{1}{8}$$

The three RC stages have a cumulative gain of 1/8. So, to satisfy Barkhausen criterion, the gain of the oscillator A = 8. In practice, a gain $\gg$ 8 is required for the oscillation.

D. Analogue Filter

11. Given in the figures below are an RC filter circuit and its frequency response plot with the output voltage of the filter circuit is taken across capacitor C_2. Selected values of the plots taken from the circuit measurements in the lab are also listed in the table below.





Frequency (Hz)	Gain (dB)	Phase (degree)
9.5	-4.5	45
15	-3	32
109	-1.5	0
910	-3	-38
1.1 k	-3.6	-45
1.4 k	-4.5	-53

a. Calculate the cut-off frequency of the filter circuit above. [4 marks]

b. From the table and graph, find the high-pass cut-off frequency for this filter. [2 marks]

c. Explain the difference between the calculated and the measured values. [2 marks]

Solution

a. The band-pass filter circuit as given above can be treated as two stages filter that consists of high-pass and low-pass filters.

Upper cut-off frequency of the filter stage:

$$f_H = \frac{1}{2\pi C_2 R_2} = \frac{1}{2\pi \times (50 \times 10^{-9}) \times (2 \times 10^3)} = 1.592 \times 10^3 \text{ Hz}$$

Lower cut-off frequency of the filter stage:

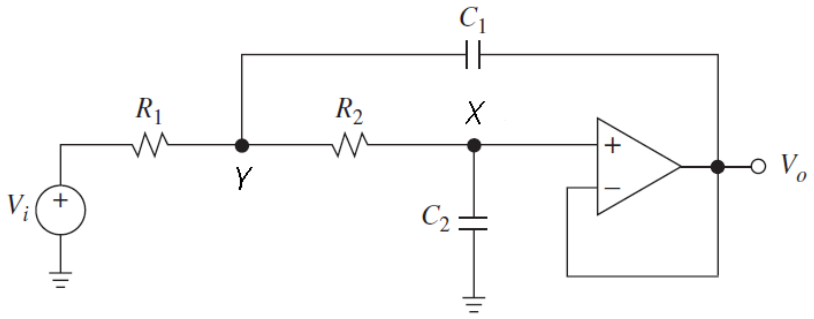
$$f_L = \frac{1}{2\pi C_1 R_1} = \frac{1}{2\pi \times (10 \times 10^{-6}) \times (1.4 \times 10^3)} = 11.37 \text{ Hz}$$

As a result, the upper and lower cut-off frequencies of the band-pass filter are 1.592 kHz and 11.37 Hz respectively.

b. The cut-off frequency of the filter circuit is approximately 9.5 Hz from the table and graph.

c. The differences are due to tolerances of the components used in the filter circuit and also due to errors of testing instruments used in measuring the variables.

12. For a given active filter shown in the figure below, perform the following tasks.



a. If an active filter used for attenuating signal application, which of the standardized filter design e.g. Butterworth, Bessel, and Chebyshev will be best to realize a stop band filter. Give a reason for your answer. [2 marks]

b. Compare passive and active filters. Give an advantage for each filter and state applications where each type of filter is particularly well suited. [5 marks]

c. Calculate the cut-off frequency and Q-factor for the low-pass Sallen-Key filter shown in figure given above, where R_1 = 1600 Ω, R_2 = 400 Ω, C_1 = 40 nF, and C_2 = 10 nF. [10 marks]

Solution

a. For a given active filter, the order for the best design of signal attenuation application is the Chebyshev Type II.

The reason is Chebyshev response filter has the sharpest roll-off slope compared with other standard filters. The stop band response can be realized more precisely with this type of filter with narrower cut-off frequency of the filter.

Furthermore, the ripples that exist in the stop band (e.g. due to type II Chebyshev response filter) could be useful for maximizing signal attenuation.

b. Comparison between passive and active filters:

Advantage:

- Passive filter: more precise design outcome and cost effective.
- Active filter: design flexibilities and application beyond conventional usages.

Application:

- Passive filter: application that requires more precise result
- Active filter: application that requires advanced signal treatment e.g. amplification, conversion, rectification, etc.

c. The cut-off frequency of the low-pass Sallen-Key filter is:

$$f_c = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}}$$

$$= \frac{1}{\sqrt{1600 \times 400 \times 40 \times 10^{-9} \times 10 \times 10^{-9}}}$$

$$= 62{,}500 \text{ rad/sec} = 9{,}947\text{Hz}$$

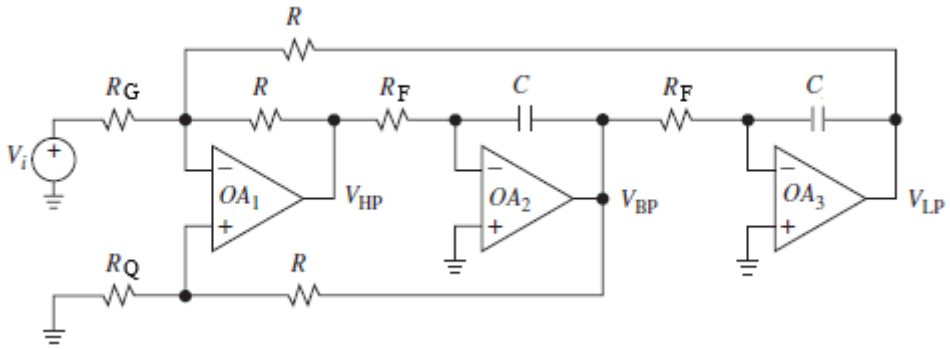
The Q-factor of the low-pass Sallen-Key filter is:

$$Q = \frac{1}{R_1 + R_2}\sqrt{R_1 R_2 \frac{C_1}{C_2}}$$

$$= \frac{1}{1600 + 400}\sqrt{1600 \times 400 \times \frac{40 \times 10^{-9}}{10 \times 10^{-9}}}$$

$$= 0.8$$

13. Given in the following figure is a state-variable filter circuit.



a. Describe Q-factor of an analogue filter. [4 marks]

b. Determine the high-level components that make up the state-variable filter circuit. [2 marks]

c. Determine the characteristics of the state-variable filter e.g. cut-off frequency, Q-factor and gain of the band-pass filter implementation of the state-variable filter when values of $= 10$ nF , $R_F = 10$ kΩ, $R = 10$ kΩ , $R_Q = 5$ kΩ , and $R_G = 2.2$ kΩ. [6 marks]

Solution

a. Q-factor of a filter is a measure just how close to perfect a filter or filter component can be. This same factor affects bandwidth and selectivity. The higher the Q, the better the filter, the lower the losses, the closer the filter is to being perfect.

Q-factor can be defined in a way that allows it to be used for tuned circuits as a measure of

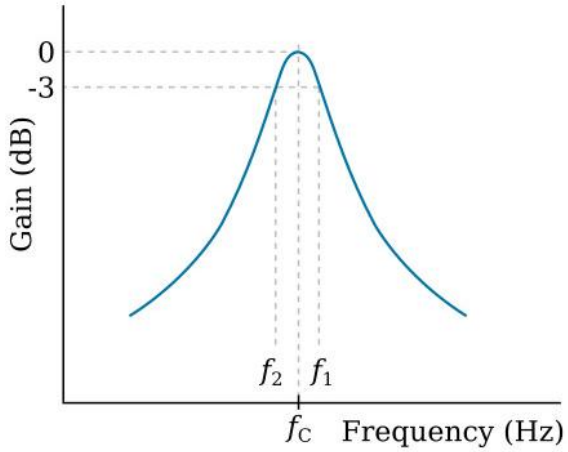
the selectivity or sharpness of tuning. The response curve for a tuned circuit is shown in the figure above, and the quality factor, Q, may be obtained as follows:

$$Q = \frac{f_c}{f_1 - f_2}$$

Where: f_c is the center frequency of the tuned circuit, f_1 is the upper cut-off frequency, and f_2 is the lower cut-off frequency.

Notice that since Q is a ratio of two frequencies, it is a dimensionless quantity, so that the following equation is also valid:

$$Q = \frac{\omega_c}{\omega_1 - \omega_2}$$



b. For the given state variable filter, it consists of three stages e.g. high pass, band pass and low pass. For its circuit configuration, the filter is made up of one summing amplifier and two RC integrators.

c. For a band-pass filter implementation of the state-variable filter, when values of $= 10\ \text{nF}$, $R_F = 10\ \text{k}\Omega$, $R = 10\ \text{k}\Omega$, $R_Q = 5\ \text{k}\Omega$, and $R_G = 2.2\ \text{k}\Omega$, the parameters and characteristics of the state variable filter can be approximated as follow.

The cut-off frequency is:

$$f_o = \frac{1}{2\pi C R_F} = \frac{1}{2\pi(10\ \text{nF})(10\ \text{k}\Omega)} = 6369.4\ \text{Hz}$$

The Q factor is:

$$Q = \frac{1}{2}\left(1 + \frac{R}{R_Q}\right) = \frac{1}{2}\left(1 + \frac{10\ \text{k}\Omega}{5\ \text{k}\Omega}\right) = 1.5$$

The gain of the band-pass filter part is:

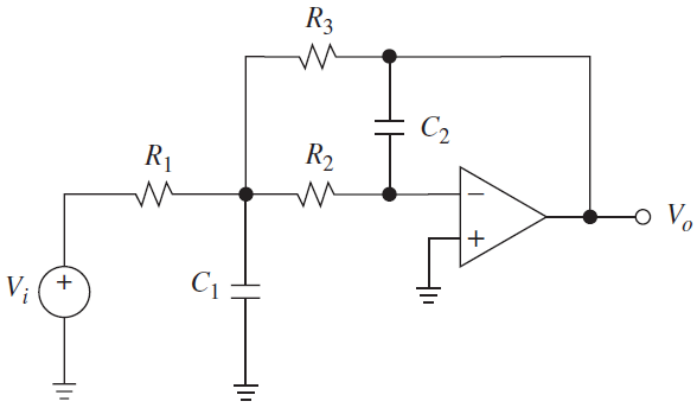
$$A_{BP} = \frac{R}{R_G} = \frac{10\ \text{k}\Omega}{2.2\ \text{k}\Omega} = 4.55$$

14. The circuit in the figure given below is a multi-feedback filter.

a. Describe the characteristics of this type of filter compared with other active filter examples e.g. Sallen-Key filter, state-variable filter, etc. [2 marks]

b. Calculate the cut-off frequency of this filter when the values of resistors are $R_1 = 1\ \text{k}\Omega$, $R_2 = 1\ \text{k}\Omega$, $R_3 = 10\ \text{k}\Omega$ and the values of the capacitors are $C_1 = 1\ \text{nF}$ and $C_2 = 10\ \text{nF}$. [2 marks]

c. Determine the Q-factor characteristic of the filter. [4 marks]



Solution

a. The multi-feedback filter is a type of second-order active filters e.g. it has two-pole arrangement. It has a reduced sensitivity to component values compared with other examples of active filter circuits, meaning that its performance is less prone from components tolerance or variation.

b. Cut-off frequency of the filter circuit is:

$$f_c = \frac{1}{2\pi\sqrt{C_1 C_2 R_2 R_3}} = \frac{1}{2\pi\sqrt{(1\text{nF})(10\text{nF})(1\text{k}\Omega)(10\text{k}\Omega)}} = 15.92\ \text{kHz}$$

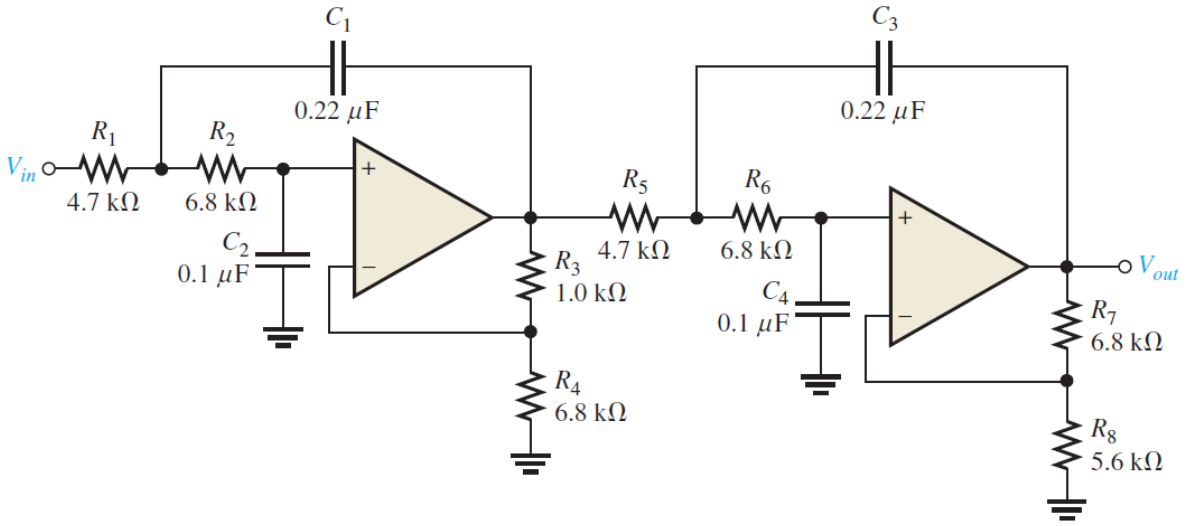
c. Q-factor characteristic of the filter circuit is:

$$Q = \frac{1}{2\zeta} = \frac{2\pi\sqrt{C_1 C_2 R_2 R_3}}{(R_2 + R_3 + |K|R_2)C_2} = \frac{2\pi\sqrt{(1\ \text{nF})(10\ \text{nF})(1\text{k}\Omega)(10\text{k}\Omega)}}{(1\text{k}\Omega + 10\text{k}\Omega + |10|1\text{k}\Omega)(10\ \text{nF})} = 0.3$$

Where:

$$K = -\frac{R_3}{R_1} = \frac{10\ \text{k}\Omega}{1\ \text{k}\Omega} = 10$$

15. Given in the figure below is a fourth-order filter derived from two multi feedback (MFB) filter circuit.



a. By using the table of standard Butterworth response filter design specification given below, is the four-pole filter approximately optimised for a Butterworth response? What is its roll-off rate? [10 marks]

Order	Roll-Off dB/Decade	1st Stage			2nd Stage			3rd Stage		
		Poles	DF	R_1/R_2	Poles	DF	R_1/R_2	Poles	DF	R_1/R_2
1	-20	1	Optional							
2	-40	2	1.414	0.586						
3	-60	2	1.00	1	1	1.00	1			
4	-80	2	1.848	0.152	2	0.765	1.235			
5	-100	2	1.00	1	2	1.618	0.382	1	0.618	1.382
6	-120	2	1.932	0.068	2	1.414	0.586	2	0.518	1.482

b. Determine the critical frequency of the filter. [4 marks]

c. Without changing the response curve, adjust the component values in the filter to make it an equal-value components filter. Select C = 0.22 µF for both stages and use E24 component standard (see Appendix). [10 marks]

Solution

a. The filter circuit is a type of fourth-order high-pass filter circuit that has double two-pole parts e.g. first stage and second stage. Thus, its design is determined as follows.

The damping factor of the 1st stage is:

$$DF = 2 - \left(\frac{R_3}{R_4}\right) = 2 - \left(\frac{1\ \text{k}\Omega}{6.8\ \text{k}\Omega}\right) = 1.85$$

The damping factor of the 2nd stage is:

$$DF = 2 - \left(\frac{R_7}{R_8}\right) = 2 - \left(\frac{6.8\ \text{k}\Omega}{5.6\ \text{k}\Omega}\right) = 0.786$$

From the filter response table, the 1st stage DF = 1.848 and the 2nd stage DF = 0.765. Therefore, this filter is approximately Butterworth.

With double two-pole parts, the filter circuit has a roll-off rate = 80 dB/decade.

b. The cut-off frequency of the filter circuit is calculated when:

$$f_0 = \frac{1}{2\pi\sqrt{R_1R_2C_1C_2}} = \frac{1}{2\pi\sqrt{R_5R_6C_3C_4}}$$

Thus, it is:

$$f_0 = \frac{1}{2\pi\sqrt{(4.7\text{k}\Omega)(6.8\text{k}\Omega)(0.22\mu\text{F})(0.1\mu\text{F})}} = 190\ \text{Hz}$$

c. Considering the values of the resistor, $R_1 = R_2 = R_5 = R_6 = R$ and the capacitor, $C_1 = C_2 = C_3 = C_4 = C$, then let the capacitor, C = 0.22 µF for both stages.

The cut-off frequency of the filter is:

$$f_0 = \frac{1}{2\pi\sqrt{R^2C^2}} = \frac{1}{2\pi RC}$$

Thus, the value of the resistor is:

$$R = \frac{1}{2\pi f_c C} = \frac{1}{2\pi(190\ \text{Hz})(0.22\ \mu\text{F})} = 3.81\ \text{k}\Omega$$

Referring to E24 component standard, choose R = 3.9 kΩ.

E. Power Amplifier

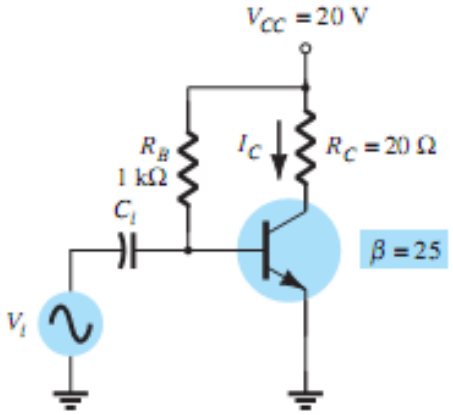
16. You are given a Class A amplifier circuit as shown below. For the given amplifier circuit, determine and calculate the following:

    a. Q-point of the amplifier. [6 marks]

    b. Input power. [8 marks]

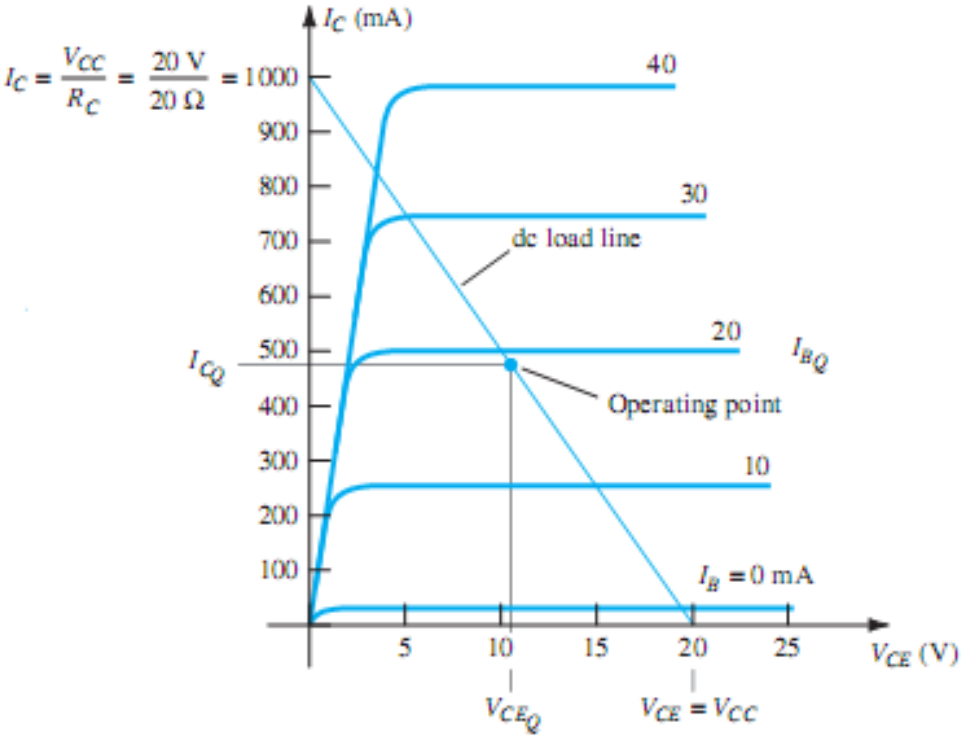
    c. Output power. [2 marks]

d. Efficiency of the amplifier circuit for an input voltage that results in a base current of 10 mA (peak). [2 marks]



Solution

a. Using equations for determining bias points of Class A amplifier's load-line, we can determine the Q -point of the given amplifier as follows.



The quotient base current of the amplifier is:

$$I_{B_Q} = \frac{V_{CC} - 0.7\text{ V}}{R_B} = \frac{20\text{ V} - 0.7\text{ V}}{1\text{ k}\Omega} = 19.3\text{ mA}$$

The quotient collector current of the amplifier is:

$$I_{C_q} = \beta I_B = 25(19.3\text{ mA}) = 482.5\text{ mA}$$

The quotient voltage drop across the collector-emitter junction of the transistor in the amplifier is:

$$V_{CE_q} = V_{CC} - I_C R_C = 20\text{ V} - (482.5\text{ mA})(20\,\Omega) = 10.4\text{ V}$$

This bias point is marked on the transistor collector characteristic of figure given above.

b. The AC variation of the output signal can be obtained graphically using the dc load line drawn as illustrated on the figure above by connecting maximum V_{CE} with maximum I_C.

Maximum collector-emitter voltage (x-axis):

$$V_{CE} = V_{CC} = 20\text{ V}$$

Maximum collector current (y-axis):

$$I_C = V_{CC}/R_C = 20\text{ V}/20\,\Omega = 1\text{ A}$$

When the input AC base current increases from its DC bias level, the collector current rises by:

$$I_C(\text{peak}) = \beta I_B(\text{peak}) = 25(10\text{ mA}) = 250\text{ mA}$$

The AC output power of the amplifier is:

$$P_o(ac) = I_C^2(\text{rms})R_C = \left[\frac{I_C^2(\text{peak})}{2}\right]R_C = \frac{(250\text{ mA})^2}{2}(20\,\Omega) = 0.625\text{ W}$$

c. The DC input power of the amplifier is:

$$P_i(dc) = V_{CC} I_{C_q} = (20\text{ V})(482.5\text{ mA}) = 9.6\text{ W}$$

d. The amplifier's power efficiency can then be calculated using equation for efficiency:

$$\%\,\eta = \left(\frac{P_o(ac)}{P_i(dc)}\right) \times 100\% = \left(\frac{0.625\text{ W}}{9.6\text{ W}}\right) \times 100\% = 6.5\%$$

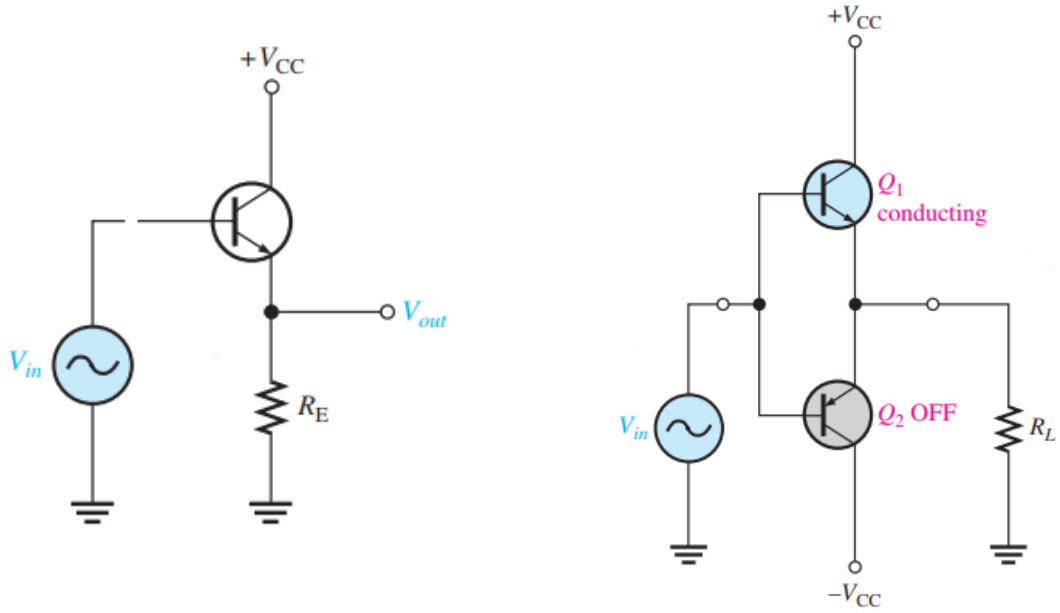
17. You are given a Class B amplifier circuit below that provides a 20-V peak signal to a 16 Ω load (speaker) and requires a power supply of V_{CC} = 30 V.

a. Briefly describe, with the aid of diagrams, two methods that can be used to reduce the crossover distortion of a Class B amplifier. [4 marks]

b. Determine the input power, output power, and circuit efficiency of the amplifier. [10 marks]

c. Determine the amplifier's maximum input power, output power, and transistor dissipation.

[10 marks]



Note: Class B amplifier (left) and push-pull Class B amplifier (right).

Solution

a. To reduce the crossover distortion of a Class B amplifier, for Class B, add feedback resistor across the biasing points of the amplifier and adding diodes to provide biasing to dead zone associated with the amplifier cross over distortions.

b. For the given Class B amplifier, the input power, output power, and circuit efficiency are:

A 20-V peak signal across a 16 Ω load provides a peak load current of

$$I_L(\text{peak}) = \frac{V_L(\text{peak})}{R_L} = \frac{20\ \text{V}}{16\ \Omega} = 1.25\ \text{A}$$

The dc value of the current drawn from the power supply is then

$$I_{dc} = \left(\frac{2}{\pi}\right) I_L(\text{peak}) = \left(\frac{2}{\pi}\right)(1.25\ \text{A}) = 0.796\ \text{A}$$

As a result, the input power delivered by the supply voltage is:

$$P_i(dc) = V_{CC} I_{dc} = (30\ \text{V})(0.796\ \text{A}) = 23.9\ \text{W}$$

The output power delivered to the load is

$$P_o(ac) = \frac{V_L^2(\text{peak})}{2R_L} = \frac{(20\ \text{V})^2}{2(16\ \Omega)} = 12.5\ \text{W}$$

This gives a result of the efficiency figure of the amplifier of:

$$\%\,\eta = \left(\frac{P_o(ac)}{P_i(dc)}\right) \times 100\% = \left(\frac{12.5\text{ W}}{23.9\text{ W}}\right) \times 100\% = 52.3\%$$

c. The maximum input power, output power, and transistor dissipation of the given Class B amplifier can be determined as follows.

The maximum output power of Class B amplifier is:

$$\text{Maximum } P_o(\text{ac}) = \frac{V_{CC}^2}{2R_L} = \frac{(30\text{ V})^2}{2(16\,\Omega)} = 28.125\text{ W}$$

The maximum input power drawn from the voltage supply is:

$$\text{Maximum } P_i(\text{dc}) = \frac{2V_{CC}^2}{\pi R_L} = \frac{2\,(30\text{ V})^2}{\pi(16\,\Omega)} = 35.81\text{ W}$$

The circuit efficiency is then:

$$\text{Maximum } \%\,\eta = \left[\frac{P_o(ac)}{P_i(dc)}\right] \times 100\% = \left[\frac{28.125\text{ W}}{35.81\text{ W}}\right] \times 100\% = 78.54\%$$

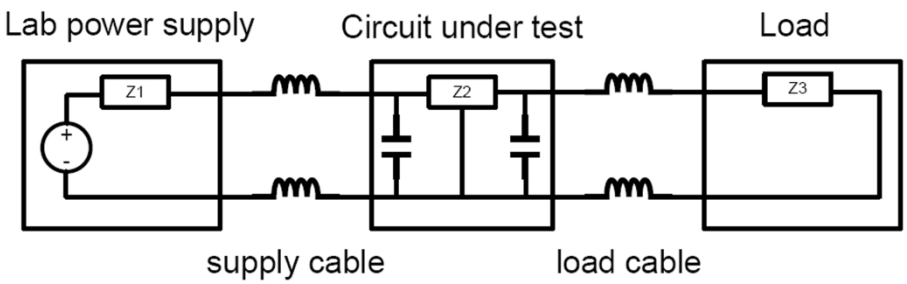
It is as expected. The maximum power dissipated by each transistor is:

$$\text{Maximum } P_Q = \frac{\text{Maximum } P_{2_Q}}{2} = 0.5\left(\frac{2V_{CC}^2}{\pi^2 R_L}\right) = 0.5\left[\frac{2(30\text{ V})^2}{\pi^2 16\,\Omega}\right] = 5.7\text{ W}$$

Under maximum conditions a pair of transistors each handling 5.7 W at most can deliver 28.125 W to a 16 Ω load while drawing 35.81 W from the supply.

F. Power Supply

18. In the electronic laboratory, you are tasked to test a power supply circuit. With given testing equipment and power supply circuit testing set up as shown in the figure below, you managed to take some measurements from the circuit.



a. Using a DC and AC voltmeter to measure the output signal from a filter circuit, readings of 25 V DC and 1.5 V rms are observed in the DMM. Calculate the ripple of the filter output

voltage. [2 marks]

b. A DC voltage supply provides 60 V when the output is unloaded. When connected to a load, the output drops to 56 V. Calculate the value of voltage regulation. [2 marks]

c. Calculate the ripple voltage of a full-wave rectifier with a 100-mF filter capacitor connected to a load drawing 50 mA. [2 marks]

d. If the peak rectified voltage for the filter circuit is 30 V, calculate the filter DC voltage. [4 marks]

e. Calculate the ripple of a capacitor filter for a peak rectified voltage of 30 V, capacitor C = 50 mF, and a load current of 50 mA. [2 marks]

f. If the RC filter section has R = 120 Ω, C = 10 mF, calculate the DC voltage across a 1 kΩ load when the DC voltage across the initial filter capacitor is V_{dc} = 60 V. [2 marks]

Solution

a. The ripple of the filter output voltage is.

$$r = \left[\frac{V_r(\text{rms})}{V_{dc}}\right] \times 100\% = \left[\frac{1.5\ \text{V}}{25\ \text{V}}\right] \times 100\% = 6\%$$

b. The value of voltage regulation is.

$$\%\ \text{Voltage Regulation} = \left[\frac{V_{NL} - V_{FL}}{V_{FL}}\right] \times 100\% = \left[\frac{60\ \text{V} - 56\ \text{V}}{56\ \text{V}}\right] \times 100\% = 7.1\%$$

c. The ripple voltage of a full-wave rectifier with a 100-mF filter capacitor connected to a load drawing 50 mA is.

$$V_r(\text{rms}) = \frac{2.4(50)}{100} = 1.2\ \text{V}$$

d. The filter DC voltage is:

$$V_{dc} = V_m - \frac{4.17(I_{dc})}{C} = 30 - \frac{4.17(50)}{100} = 27.9\ \text{V}$$

e. The ripple of a capacitor filter for a peak rectified voltage of 30 V, capacitor C = 50 mF, and a load current of 50 mA is as follows.

$$r = \left[\frac{2.4I_{dc}}{CV_{dc}}\right] \times 100\% = \left[\frac{(2.4)(50 \times 10^{-3})}{(2 \times 50 \times 10^{-3})(27.9)}\right] \times 100\% = 4.3\%$$

We could also calculate the ripple using the basic definition:

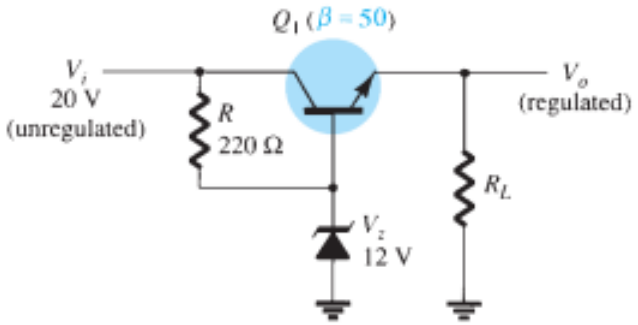
$$r = \left[\frac{V_r(\text{rms})}{V_{dc}}\right] \times 100\% = \left[\frac{1.2\ \text{V}}{27.9\ \text{V}}\right] \times 100\% = 4.3\%$$

f. The DC voltage across a 1 kΩ load for an RC filter section (R = 120 Ω, C = 10 mF) when the DC voltage across the initial filter capacitor is V_{dc} = 60 V is as follows.

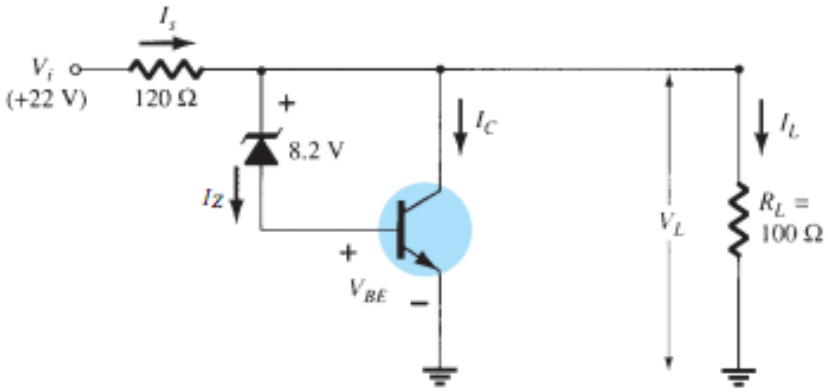
$$V'_{dc} = \left(\frac{R_L}{R + R_L}\right) V_{dc} = \left(\frac{1000}{120 + 1000}\right)(60\ \text{V}) = 53.6\ \text{V}$$

19. You are given a set of components for constructing a linear regulator in the laboratory. There are two contrasting options available to set up the regulator: linear series regulator and shunt regulator.

a. Calculate the output voltage and the Zener current in the series regulator circuit as given below for R_L = 1 kΩ. [12 marks]



b. Determine the regulated voltage and circuit currents for the shunt regulator circuit as given below. [10 marks]



c. Compare the performance of series-linear regulator with the shunt-linear regulator. [4 marks]

Solution

a. For the given series voltage regulator circuit, the output voltage and the Zener current are.

$$V_O = V_Z - V_{BE} = 12\text{ V} - 0.7\text{ V} = 11.3\text{ V}$$

$$V_{CE} = V_i - V_o = 20\text{ V} - 11.3\text{ V} = 8.7\text{ V}$$

$$I_R = \frac{20\text{ V} - 12\text{ V}}{220\ \Omega} = \frac{8\text{ V}}{220\ \Omega} = 36.4\text{ mA}$$

For R_L = 1 kΩ:

$$I_L = \frac{V_O}{R_L} = \frac{11.3\text{ V}}{1\text{ k}\Omega} = 11.3\text{ mA}$$

$$I_B = \frac{I_C}{\beta} = \frac{11.3\text{ mA}}{50} = 226\ \mu\text{A} \qquad (\text{assuming that } I_C = I_L)$$

$$I_Z = I_R - I_B = 36.4\text{ mA} - 226\ \mu\text{A} \approx 36\text{ mA}$$

b. For the given shunt voltage regulator, the load voltage is:

$$V_L = V_Z + V_{BE}$$

Entering the values into the equation above:

$$V_L = 8.2\text{ V} + 0.7\text{ V} = 8.9\text{ V}$$

For the given load, the current at the load is:

$$I_L = \frac{V_L}{R_L} = \frac{8.9\text{ V}}{100\ \Omega} = 8.9\text{ mA}$$

With the unregulated input voltage at 22 V, the current through R is:

$$I_S = \frac{V_i - V_L}{R_S} = \frac{22\text{ V} - 8.9\text{ V}}{120\ \Omega} = 109\text{ mA}$$

So that the collector current is:

$$I_C = I_S - I_L = 109\text{ mA} - 89\text{ mA} = 20\text{ mA}$$

The current through the Zener and transistor base-emitter is smaller than I_L by the transistor beta.

c. If you compare series linear regulator vs. shunt linear regulator, it will have several advantages:

- Less complexity in terms of operation and design.
- Less dissipated power in the circuit (no shunt resistor required).

The disadvantages of series linear regulator vs. shunt linear regulator are:

- Not as responsive as shunt regulator for load changing condition and operation.
- Prone for short circuit issues and exposure to swinging high supply voltage.

20. You are given a task to design a power supply unit that will have its input from 120 V rms AC supply and using 7805 series linear voltage regulator integrated circuit.

    a. Draw a voltage supply using a full-wave bridge rectifier, capacitor filter, and the given IC regulator to provide an output of +5 V. [4 marks]

    b. For a transformer output of 15 V and a filter capacitor of 250 mF, calculate the minimum input voltage when connected to a load drawing 400 mA. [10 marks]

    c. Determine the maximum value of load current at which regulation is maintained. [6 marks]

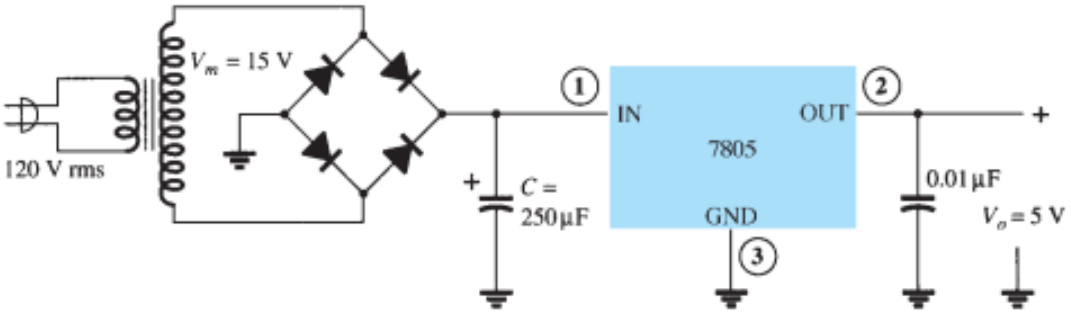
    Note: The tables given below provide some information on the input voltage minimum requirement for given output voltage of the positive and negative voltage regulators of the 7800 and 7900 series.

IC Part	Output Voltage (V)	Minimum V_i (V)
7805	+5	7.3
7806	+6	8.3
7808	+8	10.5
7810	+10	12.5
7812	+12	14.6
7815	+15	17.7
7818	+18	21.0
7824	+24	27.1

IC Part	Output Voltage (V)	Minimum V_i (V)
7905	−5	−7.3
7906	−6	−8.4
7908	−8	−10.5
7909	−9	−11.5
7912	−12	−14.6
7915	−15	−17.7
7918	−18	−20.8
7924	−24	−27.1

Solution

a. The resulting +5 V DC fixed-voltage linear-regulator power supply circuit is shown in the figure given below.



b. For a transformer output of 15 V and a filter capacitor of 250 mF, the minimum input voltage when connected to a load drawing 400 mA is found to be.

$$V_r(\text{peak}) = \sqrt{3}V_r(\text{rms}) = \sqrt{3}\left[\frac{2.4I_{dc}}{C}\right] = \sqrt{3}\left[\frac{2.4(400)}{250}\right] = 6.65\ \text{V}$$

Knowing that the voltages across the filter capacitor are:

$$V_{dc} = V_m - V_r(\text{peak}) = 15\ \text{V} - 6.65\ \text{V} = 8.35\ \text{V}$$

Since the input swings around this dc level, the minimum input voltage can drop to as low as

$$V_i(\text{low}) = V_{dc} - V_r(\text{peak}) = 15\ \text{V} - 6.65\ \text{V} = 8.35\ \text{V}$$

Since this voltage is greater than the minimum required for the IC regulator (from the table given, V_i = 7.3 V), the IC can provide a regulated voltage to the given load.

c. The maximum value of load current at which regulation is maintained.

In order to maintain $V_i(\text{min}) < 7.3$ V, then as a result.

$$V_r(\text{peak}) \leq V_m - V_i(\text{min}) = 15\ \text{V} - 7.3\ \text{V} = 7.3\ \text{V}$$

So that:

$$V_r(\text{rms}) = \frac{V_r(\text{peak})}{\sqrt{3}} = \frac{7.7\ \text{V}}{1.73} = 4.4\ \text{V}$$

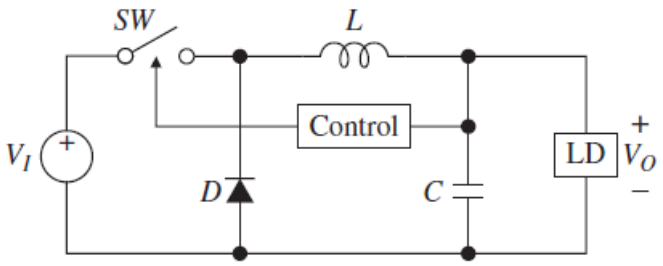
The value of load current is then:

$$I_{dc} = \frac{V_r(\text{rms})C}{2.4} = \frac{(4.4\ \text{V})(250)}{2.4} = 458\ \text{mA}$$

Any current above this value is too large for the circuit to maintain the regulator output at +5 V.

21. You are given a task to design a switching mode power supply.

a. Sketch the control part circuit diagram of a switching-mode Buck converter power supply and briefly explain how it operates. [6 marks]



b. List one advantage and one disadvantage of using switching-mode power supplies. Explain your reasoning. [4 marks]

c. The design specifications of a Buck converter are listed below:

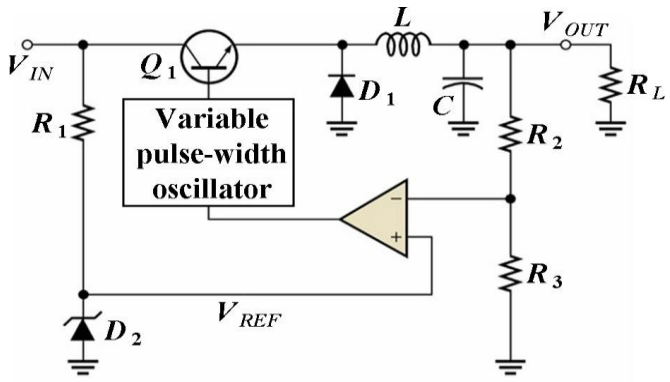
- The converter is a 12 V power source to an output of 5 V and 2 A load.
- The switching frequency is selected at 400 kHz.
- The current ripple will be limited to 30% of maximum load.

Determine the converter's duty cycle ratio, ripple current and inductance of the inductor. [6 marks]

d. Compare at least two advantages and disadvantages between Buck and Boost converters. [4 marks]

Solution

a. The following diagram shows a circuit diagram of a Buck converter with its control part.



Buck converter operates as step-down conversion (e.g. output (V_{out}) is less than the input (V_{in})) configuration. The control element Q_1 is pulsed on and off at variable rate based on the load current. The pulsations are filtered out by the LC filter.

It converts DC from one level to another, with average output voltage is controlled by the on-off switch and Pulse-Width Modulation (PWM) switching employed. The ratio of the lower average output voltage (V_{out}) over the dc input voltage (V_{in}) depends on the duty ratio, D ($D = t_{on}/T_s$).

b. There are several advantages of switch mode power supply compared with conventional power supply:

- More efficient.
- Smaller form factors.
- Easily adapted for any application and condition.

There are several disadvantages as well:

- Complex circuitry.
- Expensive to manufacture (more component counts).
- Difficult to troubleshoot.

c. Following the duty cycle pulses of converter at varying duty cycle ratios, duty cycle (D) of the converter:

$$D = \frac{V_{\text{in}}}{V_{\text{out}}} = \frac{5\text{ V}}{12\text{ V}} = 0.416$$

Ripple current of the converter (typically 30% of output current):

$$I_{\text{ripple}} = 0.3I_{\text{load}} = (0.3)(2) = 0.6$$

For an inductor of the converter circuit, the first-order equation for determining its inductance is derived from:

$$V_L = L\left(\frac{\Delta I}{\Delta T}\right)$$

The inductance-of-the inductor is:

$$L = \frac{(V_{\text{in}} - V_{\text{out}})\left(\frac{D}{f_{sw}}\right)}{I_{\text{ripple}}} = \frac{(12-5)\left(\frac{0.416}{400\times 10^3}\right)}{0.6} = 12.12\ \mu\text{H}$$

d. The comparison of advantages and disadvantages of Buck and Boost converters are given in the table below.

Converter	Advantages	Disadvantages
Buck (step-down)	• Lowest peak current efficient • Modest cost • Low-ripple current in output-filter capacitor • Simple inductor	• V_{OUT} must be less than V_{IN} • High-side switch

	• Low switch-stress voltage	
Boost (step-up)	• Low peak current • Low-side switch • Simple inductor • Low switch-stress voltage	• V_{OUT} must be greater than V_{IN} • Output cannot be completely turned off by removing drive • No short-circuit protection

22. Design a transformer operating at input voltage of 230-V (rms) 50 Hz and output voltage of 18 V. The core has a cross-sectional area of 8 mm x 8 mm and a maximum flux density of 1.3 T. Calculate the following:

    a. The maximum flux of the transformer. [6 marks]

    b. The average output voltage. [4 marks]

    c. The required number of turns of the primary and secondary windings. [6 marks]

Solution

a. For magnetic determination, the cross-sectional area of the core (A_{core}) is given as:

$$A_{\text{core}} = 0.008 \times 0.008 = 6.4 \times 10^{-5}\ \text{m}^2$$

The maximum flux in the core (Φ) is calculated as:

$$\Phi = B \cdot A_{\text{core}} = 1.3 \times (6.4\ \times 10^{-5}) = 8.32 \times 10^{-5}\ \text{Wb}$$

The maximum flux change in the core, however, is double, as the core may be magnetised in both directions, i.e. 16.64 x 10^{-5} Webber.

b. Considering a sinusoidal input voltage from the main, the average input voltage is determined from:

$$V_{\text{ave}} = \frac{2V_p}{\pi}$$

The average voltage is computed as:

$$V_{\text{ave}} = \frac{2 \cdot 230 \cdot \sqrt{2}}{\pi} = 207\ \text{V}$$

c. The number of turns (N) required is determined from:

$$N = \frac{V_{ave} \cdot t}{\Phi}$$

Where: V_{ave} is the average voltage applied to the winding.

When $t = 2 \times 50$ = 100, the required number of turns (N_p) is computed as:

$$N_p = \frac{207 \times 0.01}{16.64 \times 10^{-5}} = 1{,}244 \text{ turns}$$

Hence, expressed in terms of volt/turn, we have 0.166 volts per turn, or 6.024 turns per volt.

If the required secondary voltage is 18 V (which may be suitable for a 12 V linear regulated supply), the required number of secondary turns is:

$$N_s = 6.204 \cdot 18 = 108.4 \text{ turns}$$

23. You are given the task of designing an inductor for a Boost converter operating at 20 kHz, with a 42% duty cycle and supply voltage of 230 V (rms). The magnetic material core is a toroid inductor that has permittivity constant of 10^{-4}, a cross-sectional area of 2 cm^2, and average radius of 0.8 cm. Assume a maximum flux density of 0.055 Tesla at the frequency of operation. Calculate:

    a. The number of turns of the windings in the inductor. [4 marks]

    b. The inductance-of-inductor. [2 marks]

Solution

a. For inductance of inductor determination, the maximum flux in the core is given as:

$$\Phi = B \cdot A = 0.055 \times 2 \times 10^{-4} = 11 \times 10^{-6} \text{ Wb}$$

If the input voltage is 230 V (rms) and $t = 1/(20 \times 10^3) = 50 \times 10^{-6}$ second, the required number of primary turns is given as:

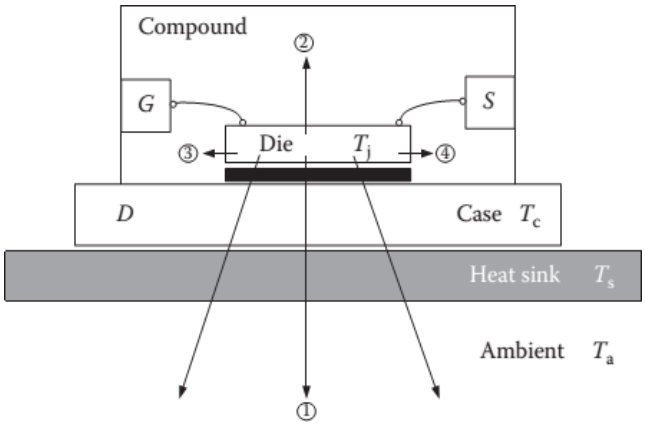
$$N = \frac{V_p \cdot t}{\Phi} = \frac{(\sqrt{2} \times 230) \times 0.42 \times 50 \times 10^{-6}}{11 \times 10^{-6}} = 620 \text{ turns}$$

b. The inductance of a toroid core is approximately given by:

$$L \approx \frac{\mu N^2 A}{2\pi r} = \frac{10^{-4} \times (620)^2 \times (2 \times 10^{-4})}{2 \times \pi \times (0.8 \times 10^{-2})} = 0.153 \text{ H}$$

G. Thermal and Noise Analysis

24. Given below is a thermal circuit setup for heat sink arrangement of a given power transistor in an audio amplifier.



a. Draw the equivalent thermal circuit of the transistor and derive the equation that illustrates the temperature allocations of the thermal circuit given above. [4 marks]

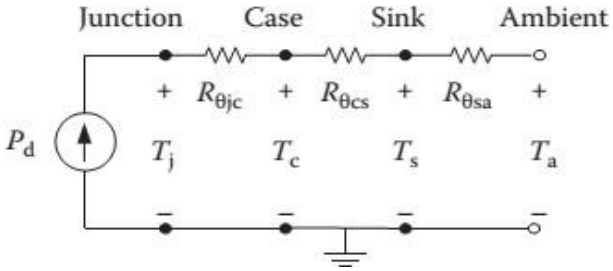
b. Determine what maximum dissipation will be allowed for an 80-W silicon transistor (rated at 25°C) if derating is required above 25°C by a derating factor of 0.5 W/°C at a case temperature of 125°C. [2 marks]

c. A silicon power transistor is operated with a heat sink (θ = 1.5 C/W). The transistor, rated at 150 W (25°C), has θ = 0.5 C/W, and the mounting insulation has θ = 0.6 C/W. What maximum power can be dissipated if the ambient temperature is 40°C and T = 200°C? [2 marks]

Solution

For the given heat sink arrangement of the power transistor.

a. For the given arrangement of the temperature allocation is illustrated with the equivalent thermal circuit given below.



Referring to the thermal circuit as given above, the equations for the circuit are:

$$R_{\theta_{ja}} = R_{\theta_{jc}} + R_{\theta_{cs}} + R_{\theta_{sa}} \qquad \text{and} \qquad R_{\theta_{jc}} = \frac{T_j - T_c}{P_d}\,[°\text{C/W}]$$

Where:

- Thermal resistance is R_θ or θ.
- j is Junction.

- c is Case.
- s is (heat) Sink.
- a is Ambient.
- P_d is power dissipated.

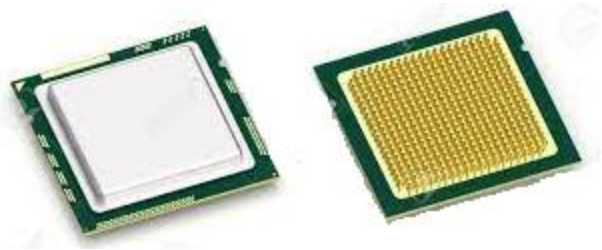
b. The maximum dissipation that will be allowed for an 80-W silicon transistor (rated at 25°C) is.

$$P_d(125°\text{C}) = P_D(25°\text{C}) - (125°\text{C} - 25°\text{C})(0.5\ \text{W}/°\text{C})$$
$$= 80\ \text{W} - 100°\text{C}\ (0.5\ \text{W}/°\text{C}) = 30\ \text{W}$$

c. The maximum power that can be dissipated in the transistor is.

$$P_D = \frac{T_j - T_a}{\theta_{jc} + \theta_{cs} + \theta_{sa}} = \frac{200°\text{C} - 40°\text{C}}{0.5°\text{C/W} + 0.6°\text{C/W} + 1.5°\text{C/W}} \approx 61.5\ \text{W}$$

25. A microprocessor as shown in the figure below is dissipating 100 W worth of heat. From its datasheet, its junction-to-ambient thermal resistance is 0.5°C/W.

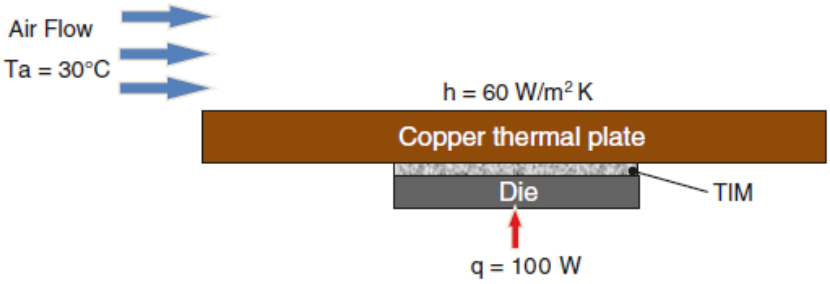


a. What is the junction temperature, T_j? [2 marks]

b. Assume 30°C ambient temperature. If the $T_j(\max)$ is 100°C, what is the thermal design power (TDP) of the microprocessor? [2 marks]

c. Consider the cooling package configuration given below of the microprocessor with a silicon die attached to a thermal plate (heat spreader) with a thermal interface material (TIM). Sketch an equivalent thermal circuit diagram of the microprocessor's cooling package. [4 marks]

d. The die is dissipating power, and the heat is lost from the thermal plate surface. What is the die temperature (T_j) and the junction-to-case thermal resistance (R_{jc})? Assume 1-D conduction. [24 marks]



Note:

Copper thermal plate:

- Thermal conductivity, k = 400 W/mK
- Size = 50 mm × 50 mm
- Thickness = 5 mm

Silicon die:

- Thermal conductivity, k = 120 W/mK
- Size = 15 mm × 15 mm
- Thickness = 0.5 mm

TIM:

- Thermal conductivity, k = 1 W/mK
- Bond line thickness (BLT) = 0.05 mm

Solution

a. Knowing that P_{total} = 100 W, θ_{ja} = 0.5°C/W, and T_a = 30°C, the junction temperature of the microprocessor is calculated as follow:

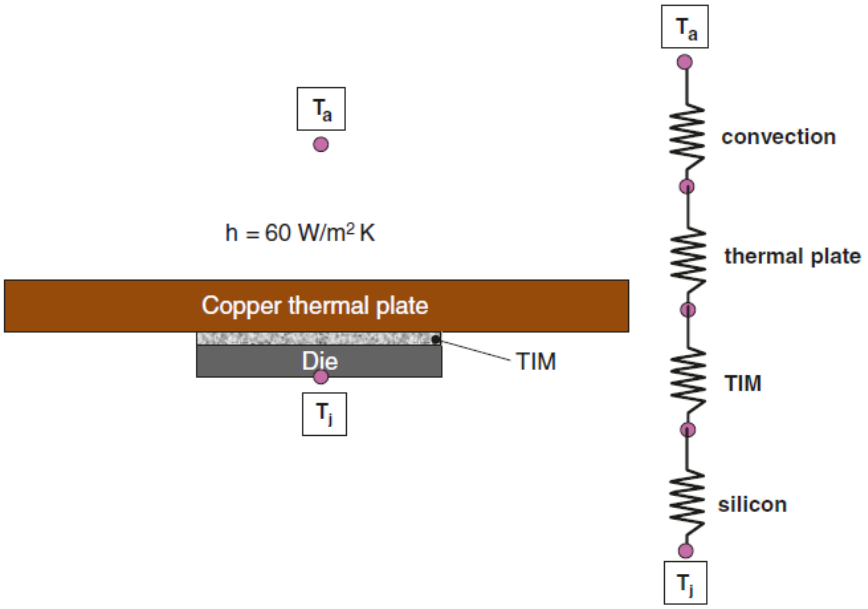
$$T_j = P_{total} \times \theta_{ja} + T_a = 100 \times 0.5 + 30 = 80°\text{C}$$

This means with 100 W input power, the junction temperature of the given microprocessor with the junction to ambient thermal resistance of 0.5°C/W, is 80°C.

b. If the $T_j(\max)$ is higher than 80°C, then the TDP should be higher than 100 W and can be computed using the equation as shown below. Knowing that $T_j(\max)$ = 100°C, θ_{ja} = 0.5°C/W, and T_{ja} = 30°C, the TDP of the microprocessor is:

$$TDP = \frac{T_j - T_a}{\theta_{ja}} = \frac{100 - 30}{0.5} = 140 \text{ W}$$

c. The equivalent thermal circuit of the copper thermal plate cooling arrangement of the microprocessor is as shown in the figure below.



d. Evaluate the thermal resistances for each segment of the package using the equation given below. For a given material, its thermal resistance is calculated from:

$$\theta_{xy} = \frac{\Delta T_{xy}}{P} = \frac{L}{KA}$$

Where:

- θ_{xy} = Thermal resistance of the material with unit of °C/W.
- ΔT_{xy} = Temperature difference between x and y.
- P = Input power.
- L = Length or thickness of the material.
- K = Thermal conductivity.
- A = Cross sectional area of the material.

Thus, the thermal resistances of various layers of materials in the microprocessor are:

$$\theta_{convection} = \frac{1}{hA_s} = \frac{1}{60(50 \times 10^{-3})(50 \times 10^{-3})} = 6.66°\text{C/W}$$

$$\theta_{plate} = \frac{L}{KA} = \frac{0.005}{400(50 \times 10^{-3})(50 \times 10^{-3})} = 0.005°\text{C/W}$$

$$\theta_{TIM} = \frac{L}{KA} = \frac{0.05 \times 10^{-3}}{1(15 \times 10^{-3})(15 \times 10^{-3})} = 0.22°\text{C/W}$$

$$\theta_{silicon} = \frac{L}{KA} = \frac{0.5 \times 10^{-3}}{120(15 \times 10^{-3})(15 \times 10^{-3})} = 0.02°\text{C/W}$$

The total thermal resistance between the junction-to-case can be given as:

$$\theta_{ja} = \theta_{silicon} + \theta_{TIM} + \theta_{plate} + \theta_{convection}$$
$$= 6.66 + 0.005 + 0.22 + 0.02 = 6.9°\text{C/W}$$

Using the equation given above, θ_{ja} is related to T_j as given below.

$$\theta_{ja} = \frac{T_j - T_a}{P} = 6.9°\text{C/W}$$

From the above equation, the unknown T_j can be evaluated as:

$$T_{ja} = \theta_{ja}P + T_a = (6.9)(100) + 30 = 720°\text{C}$$

If the safe operating temperature of the microprocessor from its datasheet is 150-200°C, notice that the junction-to-ambient temperature is way above that limit. As a result, we must attach a heatsink to cool down the microprocessor for this matter. From the equation below, θ_{jc} can be computed as:

$$\theta_{jc} = \left(\frac{T_j - T_c}{P_{uniform}}\right) A_{die} = \frac{l}{k}$$

Where:

- l = Length or thickness of layer between junction-to-case.
- k = Effective thermal conductivity.

Thus, thermal resistance between the junction-to-case is:

$$\theta_{jc} = \frac{l_{silicon}}{k_{silicon}} + \frac{l_{TIM}}{k_{TIM}} + \frac{l_{plate}}{k_{plate}}$$

The contact resistances between the TIM and the thermal plate as well as the TIM and the die interfaces have been assumed to be negligible.

$$\theta_{jc} = \frac{0.5 \times 10^{-3}}{120} + \frac{0.05 \times 10^{-3}}{1} + \frac{5 \times 10^{-3}}{400}$$

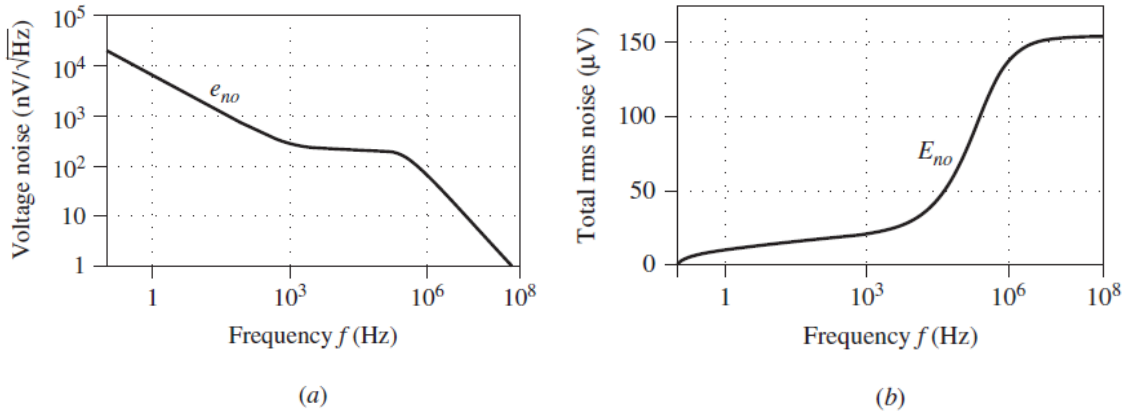
Or

$$\theta_{jc} = 6.67 \times 10^{-5} °\text{C} \cdot \text{m}^2/\text{W}$$

26. A 741 op amp is configured as an inverting amplifier with resistors R_1 = 100 kΩ, R_2 = 200 kΩ, and R_3 = 68 kΩ.

    a. Assuming e_{nw} = 20 nV/√Hz, f_{ce} = 200 Hz, i_{nw} = 0.5 pA/√Hz, and f_{ci} = 2 kHz, find the total output noise above 0.1 Hz, both rms and peak-to-peak. [10 marks]

b. The simulations of the amplifier circuit in the LTspice are given below, describe the performance of the circuit. [4 marks]



c. Scale the resistances of the circuit so that E_{no} = 50 μV. [12 marks]

d. Find the SNR of the circuit if the input is an ac signal with a peak amplitude of 0.5 V. [6 marks]

Solution

a. We have $R_1 \parallel R_2 = 100 \parallel 200 \approx 67$ kΩ, $A_{n0} = 1 + R_2/R_1 = 3$ V/V, and $f_B = 10^6/3 = 333$ kHz.

The noise voltage component of the op amp noise at the output is:

$$E_{noe} = \left(1 + \frac{R_2}{R_1}\right) e_{nw} \left[f_{ce} \ln\left(\frac{f_B}{f_L}\right) + 1.57 f_B - f_L\right]^{1/2}$$

$$= 3 \times 20 \times 10^{-9} \left[200 \ln\left(\frac{333 \times 10^3}{0.1}\right) + 1.57 \times 333 \times 10^3 - 0.1\right]^{1/2} = 43.5\ \mu\text{V}$$

The current noise component of the op amp noise at the output is:

$$E_{noi} = \left(1 + \frac{R_2}{R_1}\right) [R_3^2 + R_1 \parallel R_2]^{1/2} i_{nw} \left[f_{ci} \ln\left(\frac{f_B}{f_L}\right) + 1.57 f_B - f_L\right]^{1/2}$$

$$= 3[(68 \times 10^3)^2 + (67 \times 10^3)^2]^{1/2} \times 0.5 \times 10^{-12} \times [2 \times 10^3 \ln(333 \times 10^4) + 523 \times 10^3]^{1/2} = 106.5\ \mu\text{V}$$

The thermal noise component at the output is:

$$E_{noR} = \left(1 + \frac{R_2}{R_1}\right) [4kT\ (R_3 + R_1 \parallel R_2)(1.57 f_B - f_L)]^{1/2}$$

$$= 3[1.65 \times 10^{-20}(68 + 67) \times 10^3 \times 523 \times 10^3]^{1/2} = 102.4\ \mu\text{V}$$

Finally, total output noise is:

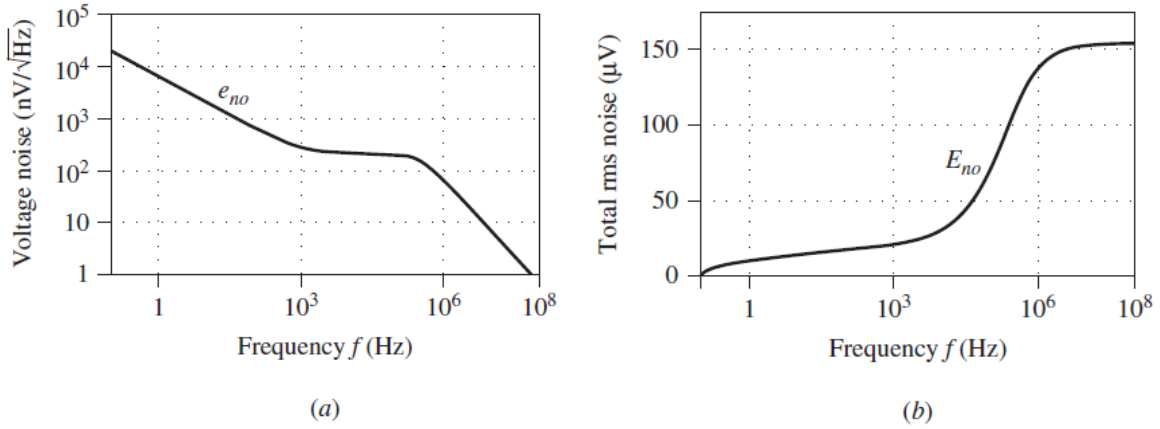
$$E_{no} = \sqrt{E_{noe}^2 + E_{noi}^2 + E_{noR}^2}$$

$$= 43.52 + 106.52 + 102.42 = 154\ \mu\text{V(rms)}$$

Or

$$E_{no} = 6.6 \times 154 = 1.02 \text{ mV(peak} - \text{to} - \text{peak)}$$

b. The results of the simulation are shown in the figures below: (a) plot of the output spectral density e_{no} of the circuit and (b) plot of the total rms output noise E_{no}.



In terms of noise, the amplifier circuit is poorly designed because E_{noi} and E_{noR} far exceed E_{noe}. This can be improved by scaling down all resistances. A good rule of thumb is to impose:

$$E_{noi}^2 + E_{noR}^2 \leq \frac{E_{noe}^2}{3^2}$$

Since this raises E_{no} only by about 5%, or less, above E_{noe}.

c. For scaling the resistances of the circuit so that E_{no} = 50 μV, we want:

$$E_{noi}^2 + E_{noR}^2 = E_{no}^2 - E_{noe}^2$$
$$= (50 \times 10^{-6})^2 - (43.5 \times 10^{-6})^2 = (24.6 \times 10^{-6})^2$$

Letting $R = R_3 + R_1 \parallel R_2$, we have:

$$E_{noi}^2 = (3)^2 \times R^2 (0.5 \times 10^{-12})^2 \times [2 \times 10^3 \ln(333 \times 10^4) + 523 \times 10^3]$$
$$= 1.24 \times 10^{-18} R^2$$

And

$$E_{noR}^2 = (3)^2 \times 1.65 \times 10^{-20} \times R \times 523 \times 10^3 = 7.77 \times 10^{-14} R$$

We want:

$$E_{noi}^2 + E_{noR}^2 = 1.24 \times 10^{-18} R^2 + 7.77 \times 10^{-14} R = (24.6 \text{ μV})^2$$

Which gives R = 7 kΩ. Thus,

$$R_3 = \frac{R}{2} = 3.5\ \text{k}\Omega$$

And

$$\frac{1}{R_1} + \frac{1}{R_2} = \frac{1}{3.5\ \text{k}\Omega}$$

Since $R_2 = 2R_1$, this yields R_1 = 5.25 kΩ and R_2 = 10.5 kΩ.

d. For finding the SNR of the circuit if the input is an ac signal with a peak amplitude of 0.5 V, since A_{s0} = −2 V/V, we have:

$$E_{ni} = \frac{154}{2} = 77\ \mu\text{V}$$

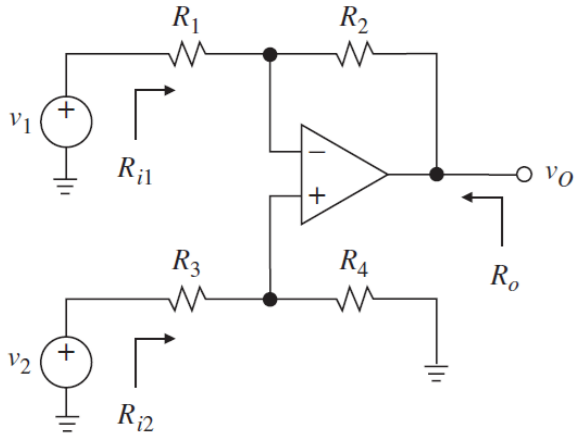
Moreover,

$$V_i(\text{rms}) = \frac{0.5}{\sqrt{2}} = 0.354\ \text{V}$$

So,

$$\text{SNR} = 20\log_10\left[\frac{0.354}{77 \times 10^{-6}}\right] = 73.2\ \text{dB}$$

27. In the difference amplifier of the figure below, let R_1 = R_3 = 10 kΩ and R_2 = R_4 = 100 kΩ.



Find the total output noise E_{no} above 0.1 Hz if the op amp is (a) the 741 type [10 marks], (b) the OP27 type [10 marks], (c) compare also the individual components E_{noe}, E_{noi}, and E_{noR} and comment on the result of analysis [4 marks].

Note:

For the 741 assume f_t = 1 MHz, e_{nw} = 20 nV/√Hz, f_{ce} = 200 Hz, i_{nw} = 0.5 pA/√Hz, and f_{ci} = 2 kHz.

For the OP27 assume f_t = 8 MHz, e_{nw} = 3 nV/√Hz, f_{ce} = 2.7 Hz, i_{nw} = 0.4 pA/√Hz, and f_{ci} = 140 Hz.

Solution

a. For 741 op amp, the noise voltages E_{noe}, E_{noi}, and E_{noR} of the circuit are calculated as follows.

The cut-off frequency of the circuit is:

$$f_B = \beta f_T = \frac{10^6}{11} = 91 \text{ kHz}$$

The noise voltage density at the output is:

$$E_{noe} = 11 \times 20 \times 10^{-9}\left[200 \ln\left(\frac{91 \times 10^3}{0.1}\right) + 1.57 \times 91 \times 10^3\right]^{1/2} \cong 84.0 \text{ μV}$$

The noise voltage density at the input is:

$$E_{noi} = 11 \times 91 \times 10^3\sqrt{2} \times 0.5 \times 10^{-12}\left[2 \times 10^3 \ln\left(\frac{91 \times 10^3}{0.1}\right) + 1.57 \times 91 \times 10^3\right]^{1/2}$$
$$\cong 292 \text{ μV}$$

The noise voltage density due to the resistor is:

$$E_{noR} = 11 \times [1.65 \times 10^{-20} \times 2 \times 91 \times 10^3 \times 1.57 \times 91 \times 10^3]^{1/2} = 228 \text{ μV}$$

The total noise voltage density at the output is:

$$E_{no} = (84^2 + 292^2 + 228^2)^{1/2} = 380 \text{ μV}$$

b. For OP27, the noise voltages E_{noe}, E_{noi}, and E_{noR} of the circuit are calculated as follows.

The cut-off frequency of the circuit is:

$$f_B = \beta f_T = \frac{8 \times 10^6}{11} = 727 \text{ kHz}$$

The noise voltage at the output is:

$$E_{noe} = 11 \times 3 \times 10^{-9}\left[2.7 \ln\left(\frac{727 \times 10^3}{0.1}\right) + 1.57 \times 727 \times 10^3\right]^{1/2} \cong 35.3 \text{ μV}$$

The noise voltage at the input is:

$$E_{noi} = 11 \times 91 \times 10^3\sqrt{2} \times 0.4 \times 10^{-12}\left[140 \ln\left(\frac{727 \times 10^3}{0.1}\right) + 1.57 \times 727 \times 10^3\right]^{1/2}$$
$$\cong 605 \text{ μV}$$

The noise voltage due to resistor is:

$$E_{noR} = 11 \times [1.65 \times 10^{-20} \times 2 \times 91 \times 10^3 \times 1.57 \times 727 \times 10^3]^{1/2} = 644 \text{ μV}$$

The total noise voltage at the output is:

$$E_{no} = (35.3^2 + 605^2 + 644^2)^{1/2} = 885\ \mu V$$

c. In both circuits current and thermal noise far exceed voltage noise, indicating that the resistances ought to be suitably reduced. Moreover, under the given conditions, the OP-27 circuit is noisier because of the higher f_t.