XMUT303 Analogue Electronics

Tutorial 7: Thermal and Noise Analysis (Solution)

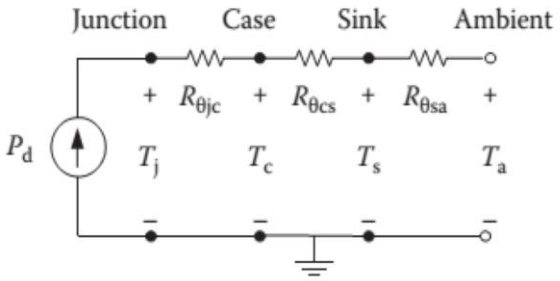
Section A. Thermal Analysis

1. When power loss occurs in electronics, it is turned into heat and the temperature of the device or component increases.

   a. Describe how the increase in device's temperature could affect the performance and characteristics of the device. [4 marks]

   b. With a help of a diagram, illustrate how heat produced at the die junction of a transistor is dissipated in the device. [4 marks]

   c. Referring to the equivalent thermal model of an electronic device given below, derive the relevant thermal equations and describe their uses. [12 marks]

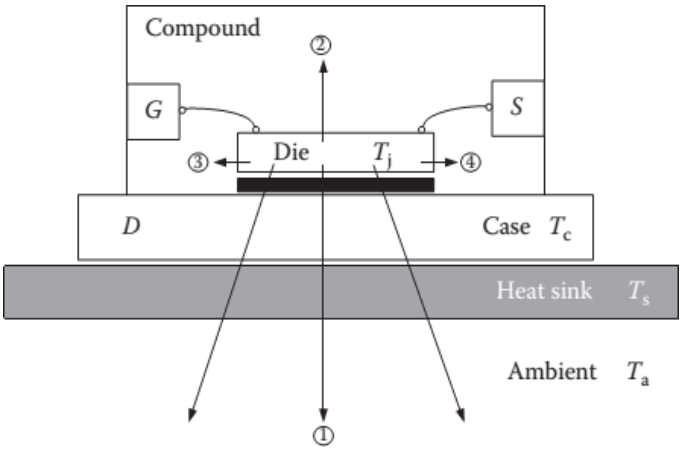


Solution

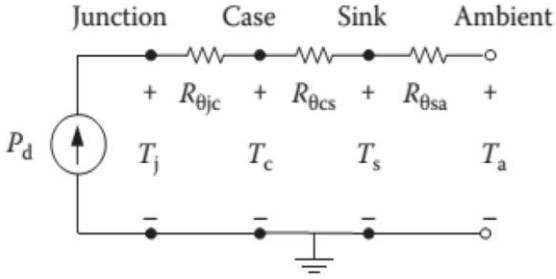
a. Increase in the device's temperature could influence the device in terms of:

- Short term - Leads to device failure (e.g. thermal cycling).
- Long term - Degrades the device characteristics (e.g. shorter life span).

b. As illustrated in the figure below, heat produced at the die junction of a transistor due to power dissipations of the component flows to the compound, case, heatsink and before it is dissipated in the ambient. About 80 % of the heat radiates in the direction of 1 and a further 20 % in direction of 2, 3, and 4.



c. For a given equivalent thermal model of a device given below, the equations used for determining thermal analysis are:



The temperature at the junction node of the device (note: R_θ is the same as θ):

$$T_j = P_d * \theta_{ja} + T_a \qquad (1)$$

The thermal resistance between the junction node and ambient of the device:

$$\theta_{ja(max)} = \left(T_{j(max)} - T_{a(max)}\right)/P_{d(max)} \qquad (2)$$

The maximum power dissipated in the device:

$$P_{d(max)} = \left(T_{j(max)} - T_{a(max)}\right)/\theta_{ja} \qquad (3)$$

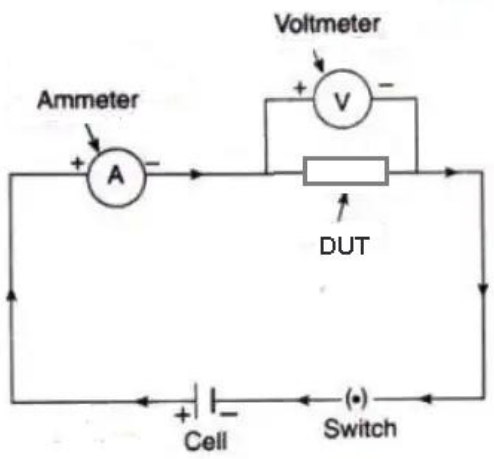
The maximum ambient temperature:

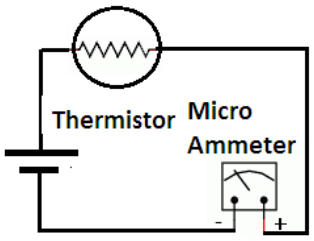
$$T_{a(max)} = T_{j(max)} - \left(P_{d(max)} * \theta_{ja}\right) \qquad (4)$$

Descriptions of the thermal equations' uses:

- Equation 1 is used for analysing the existing system.
- Equation 2 is used for designing the heat sink.
- Equations 3 and 4 are used for establishing the design limits.

2. This experiment is conducted to determine the junction-to-case thermal resistance of an electronic component as shown in the figure below.





Power is supplied to the component from a 15-V source, and the variations in the electric current and in the junction and the case temperatures with time are observed. When things are stabilized, the current is observed to be 0.1 A and the temperatures to be 80°C and 55°C at the junction and the case respectively.

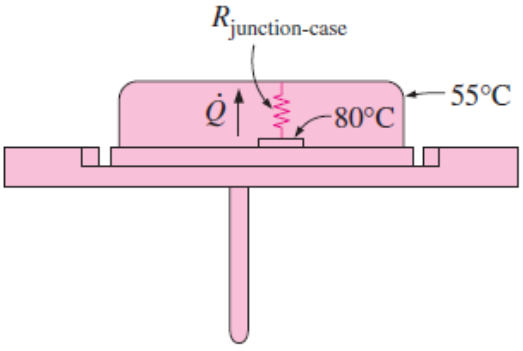
Calculate the junction-to-case resistance of this component. [8 marks]

Solution

In this experiment, the power dissipated by an electronic component as well as the junction and case temperatures are measured. The junction-to-case resistance is to be determined. We made assumptions that steady operating conditions exist when performing the measurements.

For thermal analysis, the schematic of the component is given in the figure below. The electric power consumed by this electronic component is:

$$P = VI = (15)(0.1) = 1.5\ \text{W}$$



In steady operation, this is equivalent to the heat dissipated by the component. That is,

$$P = \left(\frac{\Delta T}{\theta}\right)_{junction-case} = \frac{T_{junction} - T_{case}}{\theta_{junction-case}} = 1.5\ \text{W}$$

Then, rearranging the equation above, the junction-to-case resistance is determined to be:

$$\theta_{junction-case} = \frac{\Delta T_{junction}}{P} = \frac{(80 - 55)}{1.5} = 16.7°\text{C/W}$$

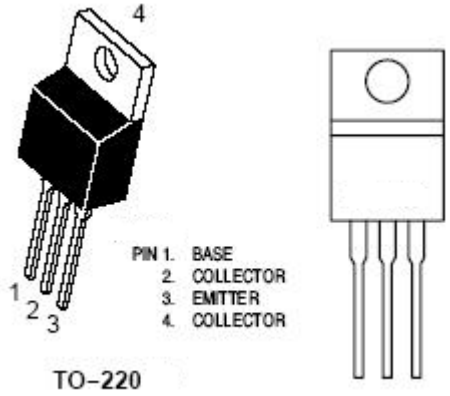
For discussion, note that a temperature difference of 16.7°C will occur between the electronic circuitry and the case of the chip carrier for each W of power consumed by the component.

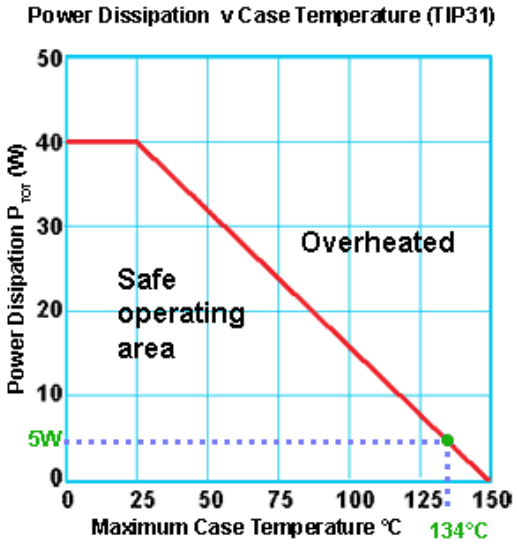
3. For the thermal analysis of an electronic device such as a transistor TIP31 as given below, it has a quoted maximum power output P_{tot} of 40 W.

   It has a TO 220 packaging and can only handle 40 W of power if the case temperature (slightly less than the junction temperature) is kept below 25°C.

   The performance of the transistor is closely dependant on its ability to dissipate the heat generated at the collector base junction.

   The following figures show TO-220 packaging (left) and graph of power dissipation vs. case temperature of TIP31 (right).





   For the thermal analysis of the given transistor, calculate as follows:

   a. Thermal resistance between junction and case. [10 marks]

   b. Maximum case temperature when dissipating 5 Watts. [4 marks]

   c. Maximum heatsink temperature. [4 marks]

   d. Thermal resistance of heatsink required. [6 marks]

Solution

a. Typical thermal resistance (R_{th} or θ) calculation for a TIP31 transistor (TO220 package) required to dissipate 5 Watts.

   - Maximum junction temperature = 150°C
   - Ambient (air) temperature = 25°C.

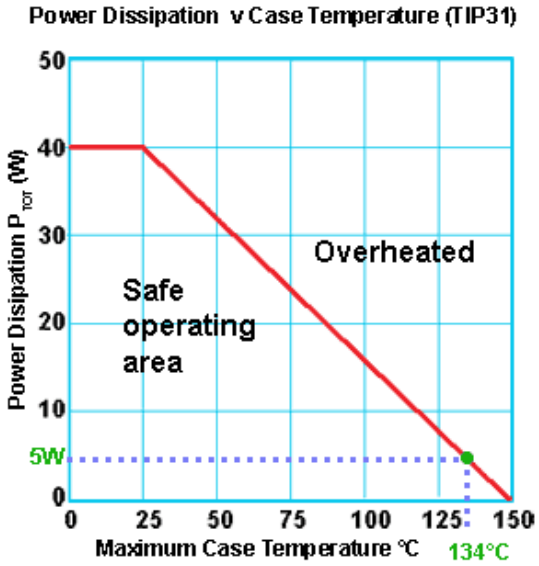
   Thermal resistance between junction and case calculated from power derating graph as shown below.

Note: assume the case temperature is the same as the ambient temperature and total power dissipated is the maximum power output.

$$\theta_{jc} = (T_j - T_c)/P_d$$

Entering the values into equation:

θ_{jc} = (150°C − 25°C) / 40 W = 3.125°C/W.

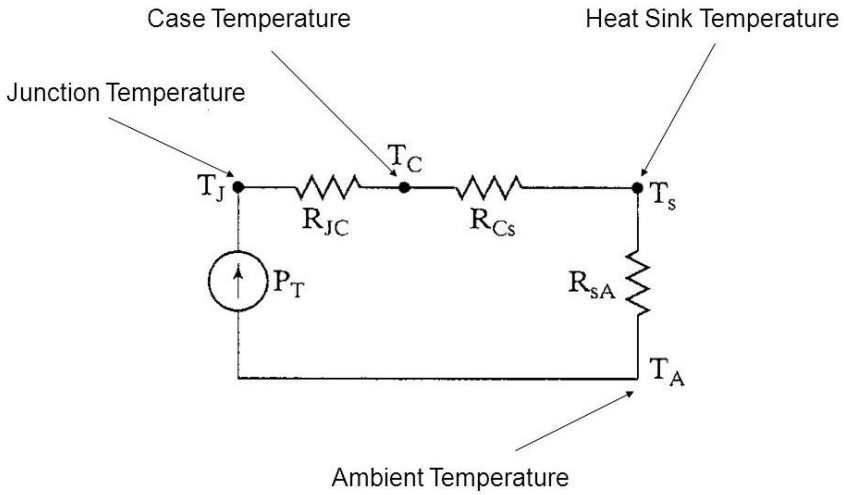


b. Maximum case temperature when dissipating 5 W is:

$$T_c = T_j - (P_d * \theta_{jc})$$

Entering values into the equation:

T_c = 150 − (5 x 3.125) = 134°C (approx)



c. Thermal resistance θ_{cs} between case and heatsink (allowing for mica washer) = 2°C/W. So, maximum heatsink temperature is:

$$T_{cs} = T_c - (P_d * \theta_{cs})$$

Entering values into the equation:

$$T_{cs} = 134 - (5 \times 2) = 124°C$$

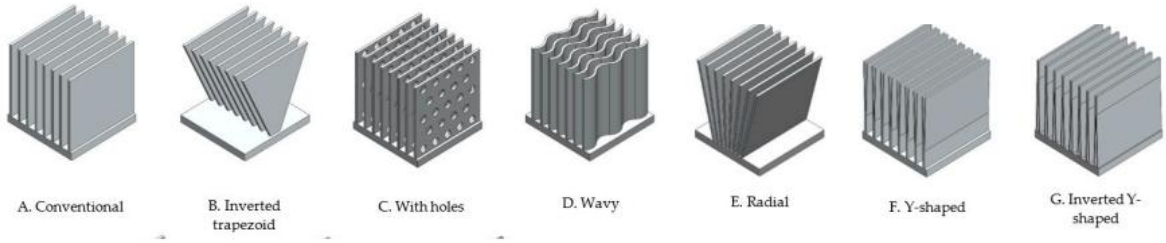
d. To reach ambient air temperature = 25°C, thermal resistance of heat-sink must be better than

$$\theta_{sa} = (T_s - T_a)/P_d$$

Entering values into the equation:

$$\theta_{sa} = (124 - 25) / 5 = 19.8°C/W$$

A better choice, to avoid operating the transistor at its maximum permitted temperature, would be to choose a heatsink with a thermal resistance of about 10 to 15°C/W.



4. A power MOSFET as shown in the figure below with its cooling arrangement has a total computed power dissipation of 10 watts. The device's maximum junction temperature is 150°C. The actual case temperature of the MOSFET must be maintained equal to or below 100°C for a reliable operation. The MOSFET thermal resistance from junction to case is 3 K/W.

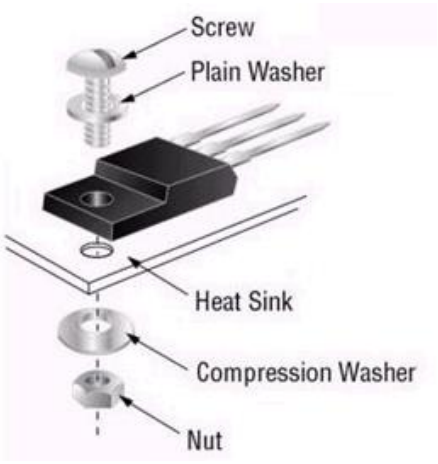
   a. Sketch the thermal analysis model of the transistor. [10 marks]

   b. Derive equation for relating temperatures and thermal resistances. [6 marks]

   c. Describe the thermal resistance between the MOSFET case and the heat sink (θ_{cs}). [4 marks]

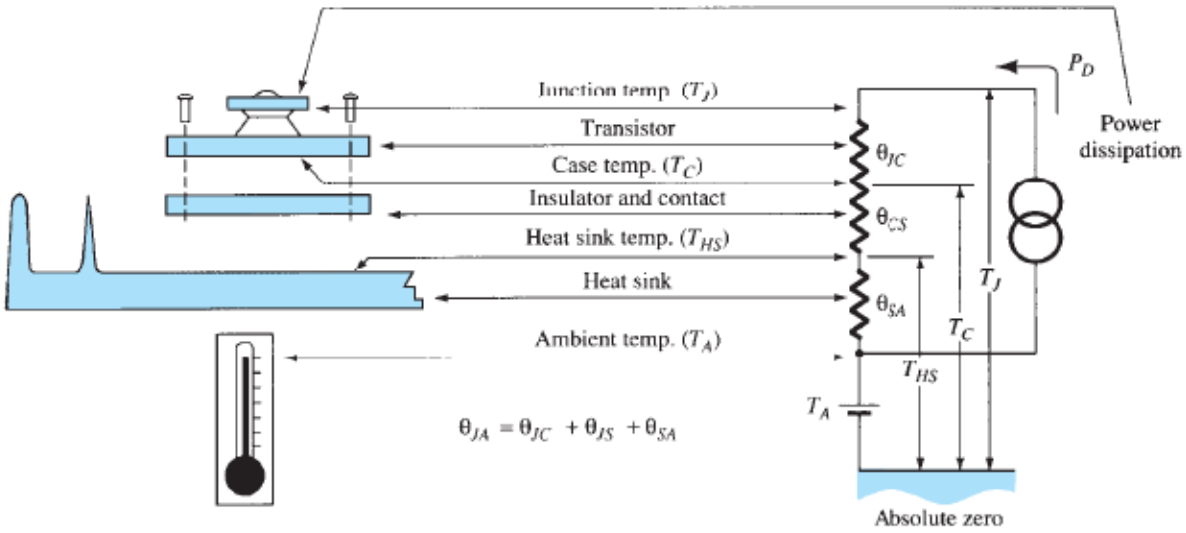
   d. Derive equation for calculating the minimum heat sink size needed. [2 marks]

   e. Calculate the minimum heatsink size needed if we neglect the thermal resistance from case to heat sink. [2 marks]



Solution

a. In between temperatures, there is a thermal resistance as illustrated in the figure below.



These temperatures and thermal resistances are:

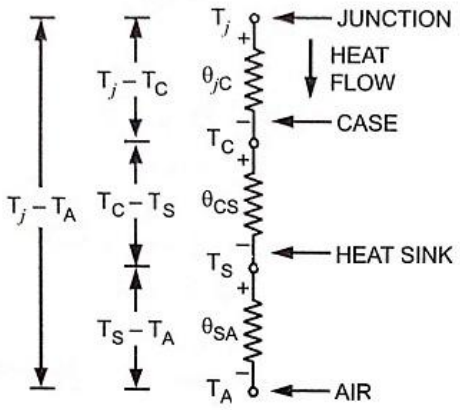
- T_j is semiconductor junction temperature.
- T_c is case temperature.
- T_s is heatsink temperature.
- T_a is ambient temperature.
- θ_{jc} is device thermal resistance from junction to case.
- θ_{cs} is thermal resistance from case to heat sink.
- θ_{sa} is thermal resistance from heat sink to air.

b. Below is an equation relating the temperatures and thermal resistances of the thermal analysis model in part (a).

$$P_d = \frac{T_{j(\max)} - T_{c(\max)}}{\theta_{jc} + \theta_{cs} + \theta_{sa}}$$

Where:

- P_d = Device total power dissipation.
- $T_{j(\max)}$ = Device maximum junction temperature.
- $T_{c(\max)}$ = Maximum allowable case temperature.
- θ_{jc} = Device thermal resistance from junction to case.
- θ_{cs} = Thermal resistance from case to heat sink.
- θ_{sa} = Thermal resistance from heat sink to air.



c. The thermal resistance between the MOSFET case and the heat sink (θ_{cs}) is the thermal resistance of the element that binds the case and the heat sink. This can be a laminate, a screw, a bolt, a clip and so on.

In power supply application, laminate is popular since it will not consume space. In this heat sink thermal resistance calculation example, the thermal resistance between MOSFET case and the heat sink is not provided. We can just neglect this one considering that the MOSFET body is perfectly binds with the heat sink.

d. What we are after of is the term θ_{sa} which is the thermal resistance of the heat sink. Modifying the above equation, we get:

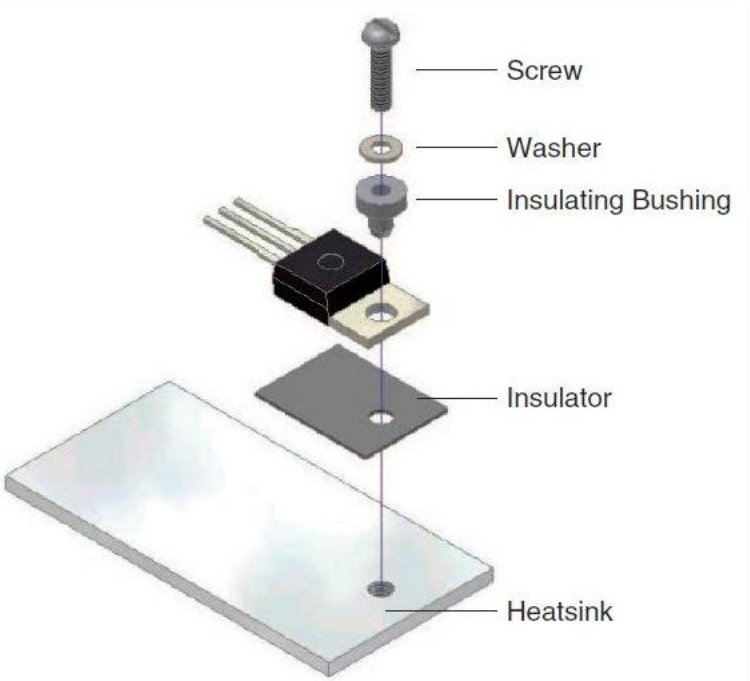
$$\theta_{sa} = \left(\frac{T_{j(\max)} - T_{c(\max)}}{P_D}\right) - \theta_{jc} - \theta_{cs}$$

e. Thus, entering the values to the equation:

$$\theta_{sa} = \left(\frac{150°\text{C} - 100°\text{C}}{10\ \text{W}}\right) - 3°\text{K/W} - 0 = 5°\text{C/W} - 3°\text{K/W} = 2°\text{K/W}$$

Remember that we are neglecting the thermal resistance from MOSFET case to heat sink. You may use a heat sink with thermal resistance that is very much lower than 2°K/W.

5. The figure below shows the thermal arrangement of a power diode. For the thermal analysis, we will suppose that the application in question has a transistor housed in a TO-220 package, where conduction and switching losses equal a power dissipation of 2.78 W.



From the datasheet, the thermal impedance from junction-to-ambient is 62°C/W and maximum operating temperature of the silicon junction is 125°C. In addition, the ambient operating temperature is expected will not go above 50°C.

a. Is a heat sink necessary for this device? [6 marks]

b. Describe how you establish thermal impedance paths. [4 marks]

c. Sketch and describe the thermal analysis model of the given power diode. [4 marks]

d. If there are sometimes irregularities in the two surfaces in thermal analysis, describe the significant of thermal insulation material (TIM). [4 marks]

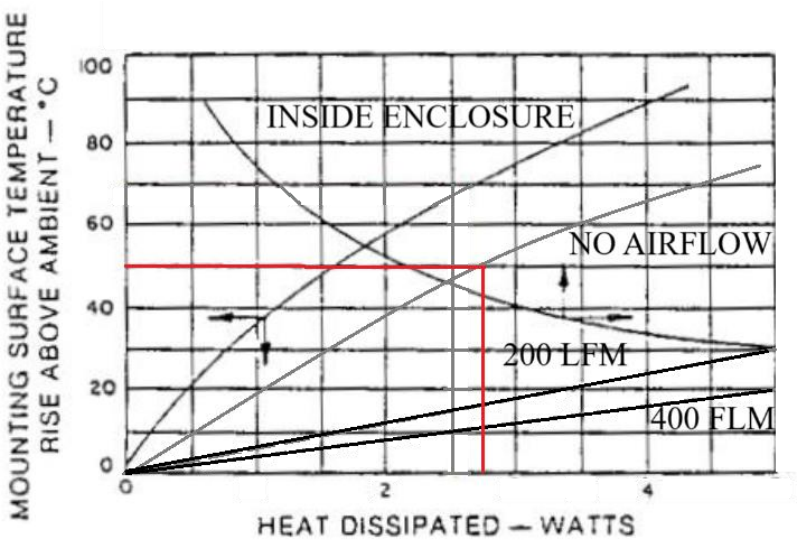
e. Calculate the thermal resistance of the thermal interface materials required. [10 marks]

f. Describe how the use of the graph from the datasheet for thermal analysis given below will help you to determine the heatsink required. Furthermore, calculate the sink-to-ambient thermal impedance based on the indicated operating point as shown in the graph. [6 marks]

g. Describe any difference observed between the required thermal resistance of the heatsink from calculation as in part (e) with the determination from the graph as in part (f). [4 marks]

h. Calculate the maximum junction temperature of the power diode. [4 marks]

i. Describe the significant of having heatsink in the thermal arrangement of the power diode.
[2 marks]



Solution

a. Firstly, one must assemble and analyse the features of all the thermal impedances that are likely to prevent the 2.78 W from being dissipated away into ambient air. If they cannot be dispersed efficiently then the junction temperature within the TO-220 package will increase above the maximum desired operating temperature, which, for this application, we will establish to be 125°C.

In general, transistor suppliers record any junction-to-ambient thermal impedance, shown with the symbol θ_{ja} and measured in units of °C/W. The unit signifies the amount the junction temperature is expected to increase above the ambient temperature around the TO-220 package for each unit of power (Watt) dissipated within the device.

To put this into context, from the transistor datasheet that the thermal impedance from junction-to-ambient is 62°C/W, the 2.78 W of dissipation inside the TO-220 package will make the junction temperature increase to 172°C above the ambient temperature e.g. calculated as:

$$\Delta T = 2.78\ \text{W} \times 62°\text{C/W} = 172°\text{C}$$

If the worst-case ambient temperature for this device is assumed to be 50°C, then the junction temperature will reach 222°C, calculated as:

$$T_J = 50°\text{C} + 172°\text{C} = 222°\text{C}$$

Since this far outstrips the specified maximum silicon temperature of 125°C, a heat sink is required.

Connecting a heat sink to the application will significantly reduce the junction-to-ambient thermal impedance. At the next stage, decide how low the thermal impedance pathway is required to be to deliver a safe and reliable operation.

b. To determine the thermal impedance pathway, begin with the greatest tolerable rise in temperature. If the largest ambient operating temperature of the device is 50°C, and we have already established that the silicon junction needs to stay at 125°C or less, then the highest permissible temperature rise sits at 75°C e.g. that is calculated as:

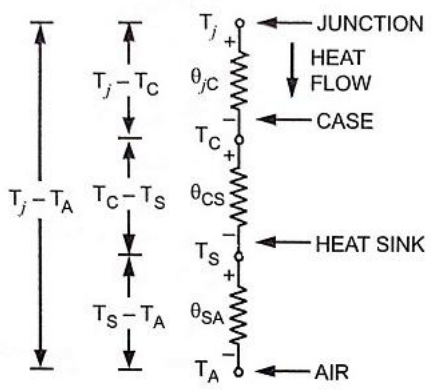
$$\Delta T = 125°C - 50°C = 75°C$$

The next step is to calculate the greatest tolerable thermal impedance between the junction itself and the ambient air. If the highest permissible temperature increase stands at 75°C and the Watts dissipated within the TO-220 package are measured at 2.78 W, then the greatest permissible thermal impedance is 27°C/W e.g. calculated as:

$$\theta_{JA} = 75°C / 2.78\ W = 27°C/W$$

Lastly, sum up all the thermal impedance pathways, from silicon junction to ambient air, and confirm that their sum is less than the largest permissible thermal impedance which is 27°C/W as calculated above.

c. In the figure below, the first thermal impedance needed is the 'junction-to-case', represented with the symbol θ_{jc}. This denotes how easy it is for heat to be transferred from the junction where heat is generated, and out to the device's surface, denoted as TO-220 in this example.



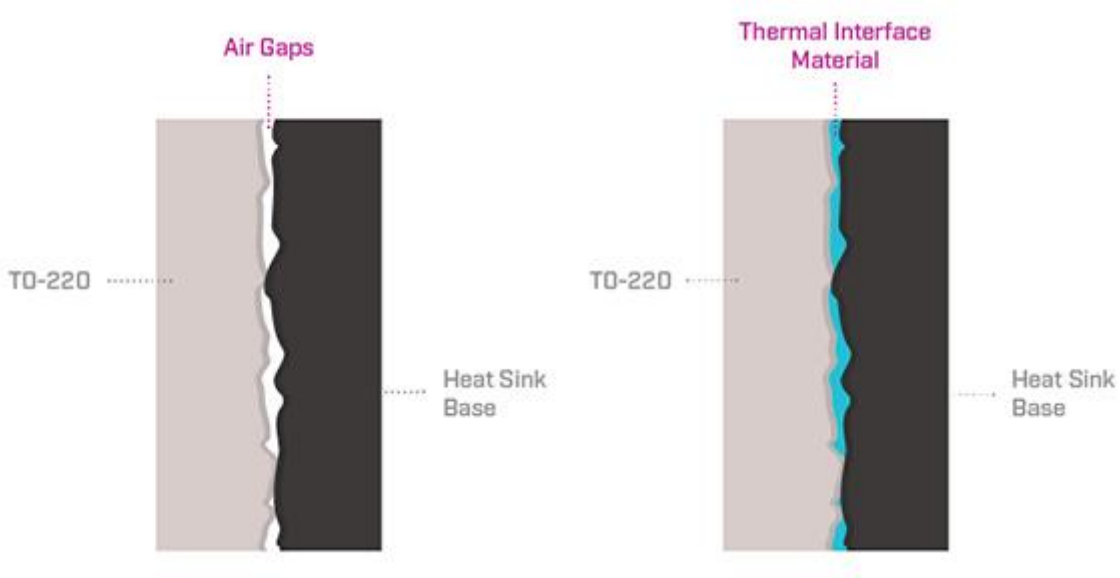
Generally, manufacturers' datasheets will list this impedance, together with the junction-to-ambient value. Here, the assumed junction-to-case thermal impedance is rated at 0.5°C/W.

Represented by the symbol θ_{cs}, the second thermal impedance needed is the 'case-to-sink', a gauge of how easily heat can be transferred from the devices outside case to the surface of the heat sink.

d. If there are sometimes irregularities in the two surfaces, it is normally recommended to apply a thermal interface material – TIM or 'thermal compound' – between the surfaces of the TO-220 case and the heat sink base to make sure, from a thermal standpoint, that they are both fully engaged.

The application of a TIM will significantly improve the transfer of heat from the TO-220's surface to the heat sink, although its associated thermal impedance must be considered.

The figure below shows a magnified surface-to-surface illustration depicting the need for a Thermal Interface Material (TIM).



Generally speaking, TIMs are characterized by their thermal conductivity, in units of measurement by Watts per Meters-Celsius (W/(m °C)) or Watts per Meters-Kelvin (W/(m K)).

In this example, Celsius and Kelvin are transposable as both use the same increase of temperature measurement, where the rise and fall of temperature are being calculated; for example, a rise in temperature of 45°C is the same as a 45°K temperature rise.

The unit of meters is included because the TIM's impedance relies upon the ratio of thickness (TIM thickness in meters) over the whole area (the area over which the TIM covers in meter square), resulting in 1/m (calculated as $m/m^2 = 1/m$).

e. In this example, a thin layer of TIM is applied over the metal tab area of TO-220's case surface, with specific properties and application details as follows:

$$\text{TIM Thermal Conductivity ('K')} = 0.79\ \text{W/m °C} = 0.79\ \text{W/m °K}$$

The area of the application is:

$$\text{TIM Application Area} = 112\ \text{mm}^2 = 112 \times 10^{-6}\ \text{m}^2$$

The thickness of the application is:

$$\text{TIM Application Thickness} = 0.04\ \text{mm} = 0.04 \times 10^{-3}\ \text{m}$$

Using the properties listed above, the thermal impedance of the TIM can be calculated with the following equation, using meters for consistency:

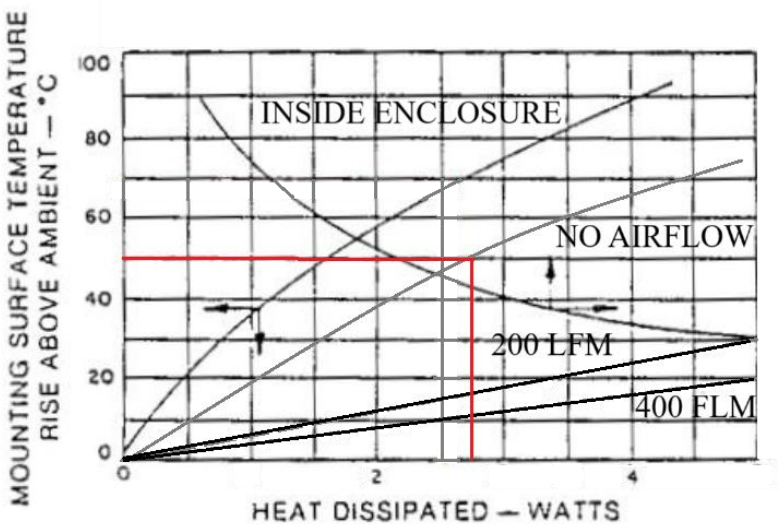
$$\theta_{cs} = \left(\frac{\text{thickness}}{\text{area}}\right)\left(\frac{1}{\text{conductivity}}\right)$$

Entering the values into equation:

$$\theta_{cs} = \left(\frac{0.04 \times 10^{-3}}{112 \times 10^{-6}}\right)\left(\frac{1}{0.79}\right) = 0.45°\text{C/W} \quad \text{or} \quad 0.45°\text{K/W}$$

The last thermal impedance needed is the 'sink-to-ambient', which is represented by the symbol θ_{sa}. This calculation reveals how easily heat can be transferred from the base of the heat sink out to surrounding ambient air.

f. Given a graph from the datasheet from a manufacturer of heatsink devices likes the one pictured in the figure below showing the typical heat sink mounting surface temperature rise above ambient, demonstrate how easily heat can be transferred from the heat sink to ambient air via different airflow loads and conditions (note in the graph: LFM = linear feet per meter).



In this example, it is assumed that the device operates under natural convection conditions without any airflow. The graph can be used to calculate the final thermal impedance, sink-to-ambient, for this specific heat sink.

The amount the surface temperature rises above ambient, divided by the heat dissipated, gives a result for thermal impedance at that specific operating condition. Here, the dispersed heat is 2.78 W, resulting in a surface temperature rise above ambient of 53°C. Dividing 53°C by 2.78 W will result in a sink-to-ambient thermal impedance of 19.1°C/W.

$$\theta_{SA} = 53°\text{C}/2.78\ \text{W} = 19.1°\text{C/W}$$

g. In previous calculations, the maximum impedance permitted between the junction and ambient air stood at 27°C/W. Subtracting the impedance of the junction-to-case (0.5°C/W) and the impedance of the case-to-sink (0.45°C/W) results in the maximum allowance for the heat sink, calculated as 26.05°C/W; worked out as:

$$\theta_S = 27°\text{C/W} - 0.5°\text{C/W} - 0.45°\text{C/W} = 26.05°\text{C/W}$$

For the purposes of this example, under these assumed conditions, a thermal impedance of 19.1°C/W for this heat sink falls well below the previous calculation of an allowance of 26.05°C/W.

This converts to a cooler silicon junction temperature inside the TO-220 package as well as a wider thermal margin within the design.

h. The maximum temperature of the junction (T_j) can be approximated by adding together all of the thermal impedances (e.g. $\theta_{jc} + \theta_{cs} + \theta_{sa}$), then multiplying them by the number of Watts dissipated at the junction (P_d), and, finally, adding the result to the maximum ambient temperature (T_a), as follows:

$$T_j = T_a + P_d \times (\theta_{jc} + \theta_{cs} + \theta_{sa})$$

Entering the values into the equation:

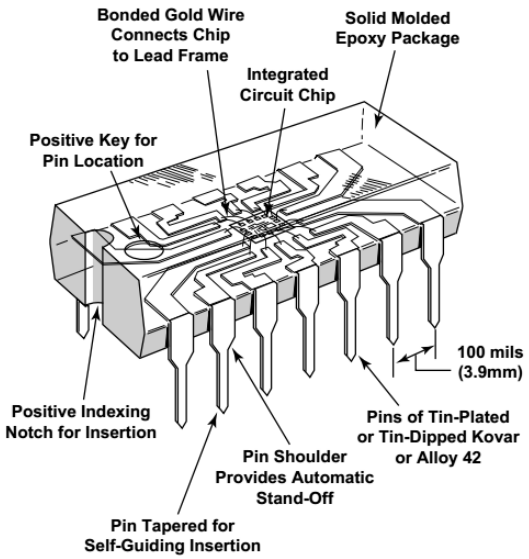
$$T_j = 50°\text{C} + 2.78 \times (0.5 + 0.45 + 19.1) = 105.7°\text{C}$$

i. The example demonstrated here reveals just how important heat sinks are in the thermal management of an application.

If the heat sink had been omitted, the silicon junction within the TO-220 package would have exceeded the design's rated limit of 125°C by a wide margin.

The process used in this question can simply be modified and repeated to help designers select the right heat sinks that are properly sized for a range of different applications.

6. A semiconductor integrated circuit chip as illustrated in the figure below is dissipating 0.6 W of power in a dual in-line package (DIP) packaging with 12 pin leads.



Parts and materials of the integrated circuit device:

- Integrated circuit chip.
- Eutectic bond.
- Bonded gold wire.
- Lead frames.
- Plastic separator insulator.
- Solid moulded epoxy package.
- Pin leads.

The materials and the dimensions of various sections of this electronic device are as given in the table below.

Section and Material	**Thermal Conductivity (W/m · °C)**	**Thickness (mm)**	**Heat Transfer Surface Area**
Junction constriction	-	-	diameter 0.4 mm
Silicon chip	120†	0.4	3 mm x 3 mm
Eutectic bond	296	0.03	3 mm x 3 mm
Copper lead frame	386	0.25	3 mm x 3 mm
Plastic separator	1	0.2	12 x 1 mm x 0.25 mm
Copper leads	386	5	12 x 1 mm x 0.25 mm

†The thermal conductivity of silicon varies greatly with temperature from 153.5 W/m · °C at 27°C to 113.7 W/m · °C at 100°C, and the value 120 W/m · °C reflects the anticipation that the temperature of the silicon chip will be close to 100°C.

a. State assumptions made for thermal analysis of the chip. [6 marks]

b. Sketch an equivalent thermal circuit of the chip. [6 marks]

c. Calculate various thermal resistances on the path of primary heat flow. [14 marks]

d. Determine the total heat resistance of the chip. [4 marks]

e. If the temperature of the leads is 40°C, estimate the temperature at the junction of the chip. [6 marks]

f. Discuss the choice of materials used in the chip and its impact towards heat dissipation. [2 marks]

Solution

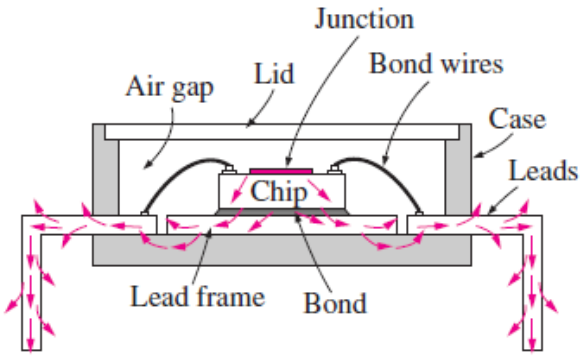
a. In this thermal analysis, the dimensions and power dissipation of a chip are given. The junction temperature of the chip is to be determined. Some of the assumptions made for the analysis are:

   i. Steady operating conditions exist.

   ii. Heat transfer through various components is one-dimensional.

   iii. Heat transfer through the air gap and the lid on top of the chip is negligible because of the very large thermal resistance involved along this path.

b. For thermal analysis, the geometry of the device is as shown in the figure below.

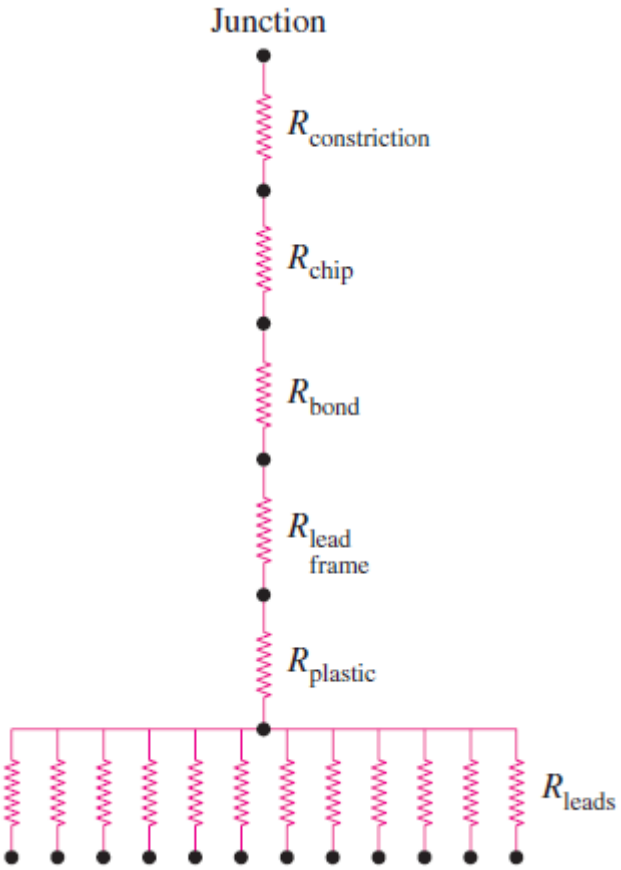


We take the primary heat flow path to be the chip, the eutectic bond, the lead frame, the plastic insulator, and the 12 leads.

When the constriction resistance between the junction and the chip is considered, the thermal resistance network for this problem becomes as shown in the figure below.

Notice that thermal resistances in the diagram and calculation assume that $R = \theta$.

- $R_{constriction}$ is thermal resistance between the junction and chip.
- R_{chip} is thermal resistance inside the chip.
- R_{bond} is thermal resistance of the bond to hold the chip in the package.
- $R_{lead\ frame}$ is thermal resistance of lead connecting the chip with the leads.
- $R_{plastic}$ is thermal resistance of the plastic separator insulator.
- R_{leads} is lead pin of the integrated circuit device (e.g. 12 of them).



c. The various thermal resistances on the path of primary heat flow are determined as follows.

$$\theta_{constriction} = \frac{1}{2\sqrt{\pi}dk} = \frac{1}{\sqrt{\pi}(0.4\times10^{-3})(120)} = 5.88°\text{C/W}$$

$$\theta_{chip} = \left(\frac{L}{kA}\right)_{chip} = \frac{0.4\times10^{-3}}{(120)(9\times10^{-6})} = 0.37°\text{C/W}$$

$$\theta_{bond} = \left(\frac{L}{kA}\right)_{bond} = \frac{0.03\times10^{-3}}{(296)(9\times10^{-6})} = 0.01°\text{C/W}$$

$$\theta_{lead\ frame} = \left(\frac{L}{kA}\right)_{lead\ frame} = \frac{0.25\times10^{-3}}{(386)(9\times10^{-6})} = 0.07°\text{C/W}$$

$$\theta_{plastic} = \left(\frac{L}{kA}\right)_{plastic} = \frac{0.2\times10^{-3}}{(1)(12\times0.25\times10^{-6})} = 66.67°\text{C/W}$$

$$\theta_{leads} = \left(\frac{L}{kA}\right)_{leads} = \frac{5\times10^{-3}}{(386)(12\times0.25\times10^{-6})} = 4.32°\text{C/W}$$

Note that for heat transfer purposes, all 12 leads can be considered as a single lead whose cross-sectional area is 12 times as large. The alternative is to find the resistance of a single lead and to calculate the equivalent resistance for 12 such resistances connected in parallel. Both approaches give the same result.

d. All the resistances determined here are in series. Thus, the total thermal resistance between the junction and the leads is determined by simply adding them up:

$$\begin{aligned}\theta_{total} &= \theta_{junction-lead} \\ &= \theta_{constriction} + \theta_{chip} + \theta_{bond} + \theta_{lead\ frame} + \theta_{plastic} + \theta_{leads} \\ &= (5.88 + 0.37 + 0.01 + 0.07 + 66.67 + 4.32)°\text{C/W} \\ &= 77.32°\text{C/W}\end{aligned}$$

e. Heat transfer through the chip can be expressed as

$$P = \left(\frac{\Delta T}{\theta}\right)_{junction-lead} = \frac{T_{junction} - T_{leads}}{\theta_{junction-lead}}$$

Solving for $T_{junction}$ and substituting the given values, the junction temperature is determined to be:

$$\begin{aligned}T_{junction} &= T_{leads} + P \cdot \theta_{junction-leads} \\ &= 40°\text{C} + (0.6\ \text{W})(77.32°\text{C/W}) = 86.4°\text{C}\end{aligned}$$

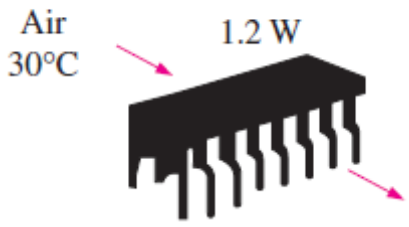
Note that the plastic layer between the lead frame and the leads accounts for 66.67/77.32 = 86 percent of the total thermal resistance and thus the 86 percent of the temperature drop (0.6 x 66.67 = 40°C) between the junction and the leads.

In other words, the temperature of the junction would be just 86.5 - 40 = 46.5°C if the thermal resistance of the plastic was eliminated.

f. For discussion, the simplified analysis given here points out that any attempt to reduce the thermal resistance in the chip carrier and thus improve the heat flow path should start with the plastic layer.

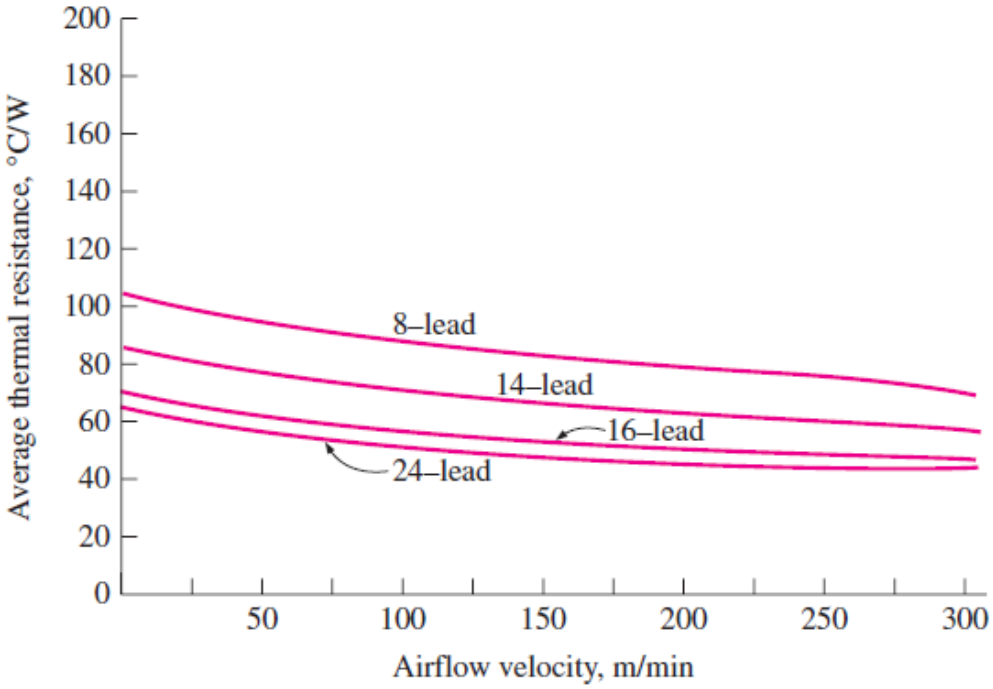
We also notice from the magnitudes of individual resistances that some sections, such as the eutectic bond and the lead frame, have negligible thermal resistances, and any attempt to improve them further will have practically no effect on the junction temperature of the chip.

7. A fan blows air at 30°C and a velocity of 200 m/min over a 1.2-W plastic DIP with 16 leads mounted on a PCB, as shown in the figure below.



a. Using data from graph of thermal resistance vs. airflow velocity given below, determine the junction temperature of the electronic device. [6 marks]

b. What would the junction temperature be if the fan were to fail? [6 marks]



Solution

a. A plastic DIP with 16 leads is cooled by forced air. Using data supplied by the manufacturer, the junction temperature is to be determined. Assume that steady operating conditions exist during temperature measurements.

For thermal analysis of the device, the junction-to-ambient thermal resistance of the device with 16 leads corresponding to an air velocity of 200 m/min is determined from the graph above to be:

$$\theta_{junction-ambient} = 55°\text{C/W}$$

Then the junction temperature can be determined from the equation below to be:

$$T_{junction} = T_{ambient} + P \cdot \theta_{junction-ambient}$$
$$= 30°\text{C} + (1.2\ \text{W})(55°\text{C/W}) = 96°\text{C}$$

b. When the fan fails, the airflow velocity over the device will be zero. The total thermal resistance in this case is determined from the same chart by reading the value at the intersection of the curve and the vertical axis to be

$$\theta_{junction-ambient} = 70°\text{C/W}$$

which gives

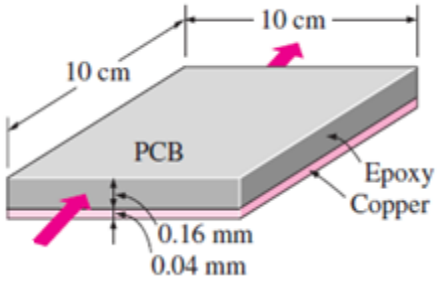
$$T_{junction} = T_{ambient} + P \cdot \theta_{junction-ambient}$$

$$= 30°\text{C} + (1.2\ \text{W})(70°\text{C/W}) = 114°\text{C}$$

For discussion, note that the temperature of the junction will rise by 18°C when the fan fails. Of course, this analysis assumes the temperature of the surrounding air still to be 30°C, which may no longer be the case.

Any increase in the ambient temperature due to inadequate airflow will reflect on the junction temperature, which will seriously jeopardize the safety of the electronic device.

8. Heat is to be conducted along a PCB with copper cladding on one side. The PCB is 10 cm long and 10 cm wide, and the thickness of the copper and epoxy layers are 0.04 mm and 0.16 mm, respectively, as shown in the figure below.



a. Disregarding heat transfer from side surfaces, determine the percentages of heat conduction along the copper (k = 386 W/m·°C) and epoxy (k = 0.26 W/m·°C) layers. [14 marks]

b. Also, determine the effective thermal conductivity of the PCB. [4 marks]

Solution

a. A PCB with copper cladding is given. The percentages of heat conduction along the copper and epoxy layers as well as the effective thermal conductivity of the PCB are to be determined. These are several assumptions for thermal analysis of the PCB:

   i. Heat conduction along the PCB is one-dimensional since heat transfer from side surfaces is negligible.

   ii. The thermal properties of epoxy and copper layers are constant.

   For the PCB thermal analysis, the length and width of both layers are the same, and so is the temperature difference across each layer.

   Heat conduction along a layer is proportional to the thermal conductivity–thickness product kt, which is determined for each layer and the entire PCB to be:

$$(kt)_{copper} = (386\ \text{W/m} \cdot °\text{C})(0.04 \times 10^3\text{m}) = 15.44 \times\ 10^3\ \text{W/°C}$$

$$(kt)_{epoxy} = (0.26\ \text{W/m} \cdot °\text{C})(0.16 \times 10^3\ \text{m})\ =\ 0.04 \times 10^3\ \text{W/°C}$$

$$(kt)_{PCB} = (kt)_{copper} + (kt\ )_{epoxy} = (15.44 +\ 0.04)10^3\ \text{m} = 15.48 \times 10^3\ \text{W/°C}$$

   Therefore, heat conduction along the epoxy board will constitute

$$f = \frac{(kt)_{epoxy}}{(kt)_{PCB}} = \frac{0.04 \times 10^{-3}}{15.48 \times 10^{-3}} = 0.0026$$

or 0.26 % of the thermal conduction along the PCB, which is negligible.

Therefore, heat conduction along the epoxy layer in this case can be disregarded without any reservations.

b. The effective thermal conductivity of the board is determined from the equation above to be:

$$k_{\text{eff}} = \frac{(kt)_{epoxy} + (kt)_{copper}}{t_{epoxy} + t_{copper}} = \frac{(15.44 + 0.04) \times 10^{-3}}{(0.16 + 0.04) \times 10^{-3}} = 77.4\ \text{W/m} \cdot \text{°C}$$

That is, the entire PCB can be treated as a 0.20-mm-thick single homogeneous layer whose thermal conductivity is 77.4 W/m·°C for heat transfer along its length.

Section B. Noise Analysis

1. Most electronic devices exhibit some form of noise. They exhibit a spectrum of voltage and/or current fluctuations that an ideal component would not.

   a. Describe three most commonly found noises in electronics. [6 marks]

   b. What is the main difference between white noise and pink noise? [4 marks]

   c. Why are we mostly dealing with spectral noise density than noise power densities when performing noise analysis? [2 marks]

   d. Derive the equation for determining the root mean square value of the noise. [8 marks]

Solution

a. The three most commonly found noise in electronics are:

- Thermal noise (charge carriers are always in motion),
- Shot noise (charge in carriers is quantised),
- Flicker noise (real devices are not perfect).

There are also some other (rarer) noise sources worth knowing about:

- Random walk noise.
- Burst noise.
- Avalanche noise.

b. The main difference between white noise and pink noise:

- White noise is not frequency dependence.
- Pink noise has power densities that are proportional to $1/f$.

c. In the noise analysis in electronics, it is more common to compare noises in terms of their signal level/amplitude (either in V or A), not in terms of power of the noise.

d. Derivation of noise equation for determining the root mean square value of the noise X_n as:

$$X_n = \left(\frac{1}{T}\int_0^T x_n^2\, dt\right)^{1/2}$$

We can also derive an expression for the sum of two noise sources. Consider the sum of two noise waveforms $x_{n1}(t)$ and $x_{n2}(t)$.

$$X_n^2 = \frac{1}{T}\int_0^T (x_{n1} + x_{n2})^2 dt$$

$$= \frac{1}{T}\int_0^T (x_{n1}^2 + x_{n2}^2 + 2x_{n1}x_{n2}) dt$$

$$= X_{n1}^2 + X_{n2}^2 + + \frac{2}{T}\int_0^T (x_{n1}x_{n2}) dt$$

Typically, in electronics, we find that there is no correlation between various noise sources. As a result, the last term in the previous expression therefore disappears. Thus, we can write:

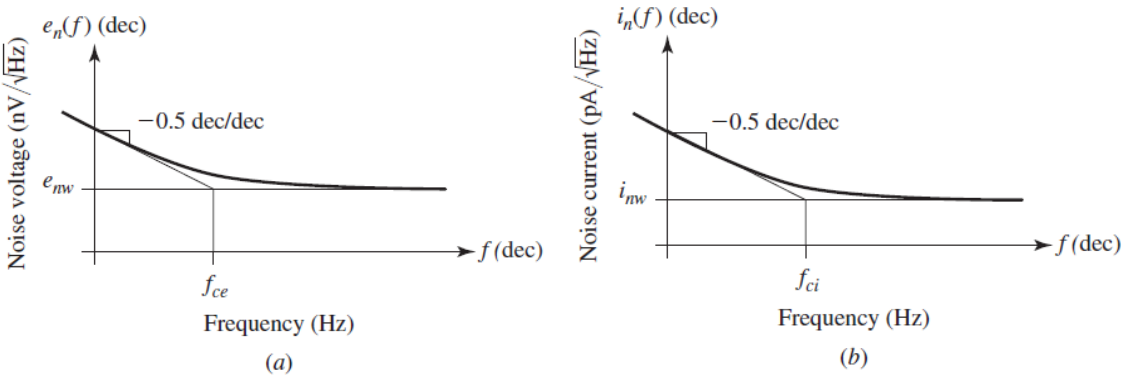
$$X_n = \sqrt{X_{n1}^2 + X_{n2}^2}$$

Or, more generally, to combine N noise sources we use:

$$X_n = \sqrt{\sum_{1=0}^{N} X_{ni}^2}$$

In other words, we add noise sources in quadrature.

2. The following diagram shows a typical spectral densities plot of integrated device circuit noise: (a) noise voltage and (b) noise current.



a. Derive the expressions for the noise voltage and current of integrated circuit device. [14 marks]

b. With regard to the spectral densities plot of integrated circuit noise given above, describe the characteristics of the noise at various frequencies in the plot. [6 marks]

c. Find E_n for the 741 op amp over the audio range (20 Hz to 20 kHz). [4 marks]

d. Repeat, but for the wide-band range of 0.1 Hz to 1 MHz, compare with part (c), and comment. [4 marks]

Solution

a. The expressions for the noise voltage and current are to be derived as follows.

The frequency distribution of noise power is specified via the noise power densities $e_n^2(f)$ and $i_n^2(f)$, each representing the average noise power over a 1-Hz bandwidth as a function of frequency f. We use the power densities to calculate analytically the rms values over an arbitrary frequency interval f_L to f_H as:

$$E_n = \sqrt{\int_{f_L}^{f_H} e_n^2(f)df} \qquad (Eq.1)$$

And

$$I_n = \sqrt{\int_{f_L}^{f_H} i_n^2(f)df} \qquad (Eq.2)$$

Since E_n is in V and f in Hz, it follows that $e_n^2(f)$ is in V²/Hz; similarly, $i_n^2(f)$ is in A²/Hz. As an example, the power densities of integrated-circuit (IC) noise take on the analytical forms:

$$e_n^2(f) = e_{nw}^2\left(\frac{f_{ce}}{f} + 1\right) \qquad (Eq.3)$$

And

$$i_n^2(f) = i_{nw}^2\left(\frac{f_{ci}}{f} + 1\right) \qquad (Eq.4)$$

So, substituting both Eqs (3) and (4) above into Eqs. (1) and (2) respectively and integrating, we obtain:

$$E_n = e_{nw}\sqrt{f_{ce}\ln\left(\frac{f_H}{f_L}\right) + f_H - f_L} \qquad (Eq.5)$$

And

$$I_n = i_{nw}\sqrt{f_{ci}\ln\left(\frac{f_H}{f_L}\right) + f_H - f_L} \qquad (Eq.6)$$

Data sheets usually show the square roots of the noise power densities, or $e_n(f)$ and $i_n(f)$. Called, if improperly, the noise voltage and the noise current for short (e.g. beware that their units are nV/$\sqrt{\text{Hz}}$ and pA/$\sqrt{\text{Hz}}$, not nV and pA), they are plotted in the figure above.

b. Referring to the given spectral densities plot of integrated circuit noise, we make the following observations:

- For $f \gg f_{ce}$ we have $e_n \to e_{nw}$, and for $f \gg f_{ci}$ we have $i_n \to i_{nw}$, indicating highfrequency asymptotes that are constant with frequency. This type of noise is called white noise by analogy with white light, which contains all frequency components, and e_{nw} and i_{nw} are aptly called white-noise floors.
- For $f \ll f_{ce}$ we have $e_n^2(f) \propto 1/f$, and for $f \ll f_{ci}$ we have $i_n^2(f) \propto 1/f$, indicating low-frequency asymptotes with slopes of -1 dec/dec. (By contrast, the plots of the square roots of the figure above exhibit slopes of -0.5 dec/dec). Noise with a power density inversely proportional to frequency f is aptly called $1/f$ noise.
- The frequencies f_{ce} and f_{ci}, representing the borderlines between $1/f$ noise and white noise are called the corner frequencies by analogy with filters. As a practical example, the data sheets of the popular 741 op amp give:

$$e_{nw} = 20\ \text{nV}\sqrt{\text{Hz}},\ f_{ce} = 200\ \text{Hz},\ i_{nw} = 0.5\ \text{pA}/\sqrt{\text{Hz}},\ \text{and}\ f_{ci} = 2\ \text{kHz}$$

c. Using the equation derived in part (a), for the audio range frequencies, the noise voltage of the op amp is:

$$E_n = e_{nw}\sqrt{f_{ce}\ln\left(\frac{f_H}{f_L}\right) + f_H - f_L}$$

$$= 20\times10^{-9}\sqrt{200\ln\left(\frac{2\times10^3}{20}\right) + 20\times10^3 - 20}$$

$$= 2.92\times10^{-6}\ \text{V rms}$$

d. Likewise, for the wide-band range frequencies, the noise voltage of the op amp is now:

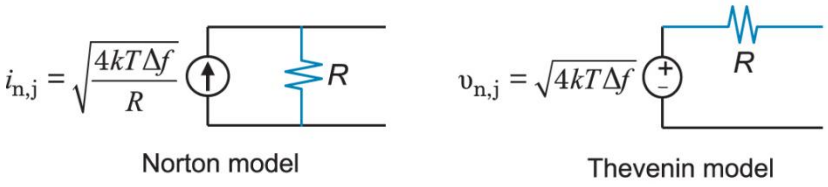
$$E_n = e_{nw}\sqrt{f_{ce}\ln\left(\frac{f_H}{f_L}\right) + f_H - f_L}$$

$$= 20\times10^{-9}\sqrt{200\ln\left(\frac{10^6}{20}\right) + 10^6 - 0.1}$$

$$= 2.92\times10^{-6}\ \text{V rms}$$

Increasing the bandwidth increases both the $1/f$ noise and the white noise contributions. However, due to its logarithmic dependence, the $1/f$ noise contribution increases less noticeably than the white noise contribution, which increases with the square root of the bandwidth.

3. Given a carbon resistor with a specific resistance value for noise measurement and analysis.



a. How is resistor noise modelled? [2 marks]

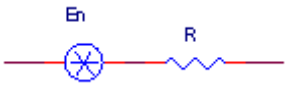
b. What is power spectral density? [2 marks]

c. How this noise is represented in the frequency spectrum. [2 marks]

d. What is voltage spectral spectra density? [2 marks]

Solution

a. Typically, it is a noise voltage in series with the resistor.



b. The power spectral density simply describes how much noise power would be generated by a resistor in a 1 Hz bandwidth.

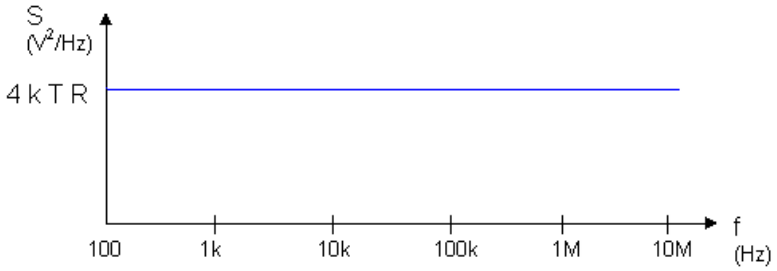
$$e_n^2 = 4kTR \quad (\text{V}^2/\text{Hz})$$

Where:

- e_n^2 = Noise power spectral density
- k = Boltzmans constant ($1.38\cdot10^{-23}$)
- T = temperature in Kelvin (e.g. room temp = 27°C = 300°K)

- R = resistance

c. This noise power is the same at all frequencies - commonly called white noise!



Note: If you want to reduce the total noise in your circuit, then reduce your bandwidth.

d. The voltage spectral density is simply the square root of the power spectral density.

$$e_n^2 = \sqrt{4kTR} \quad (\mathrm{V}/\sqrt{\mathrm{Hz}})$$

Many manufacturers will specify the noise of their components (op amps for example) using these units. Notice the noise voltage units has the units of Volts per square root of the bandwidth.

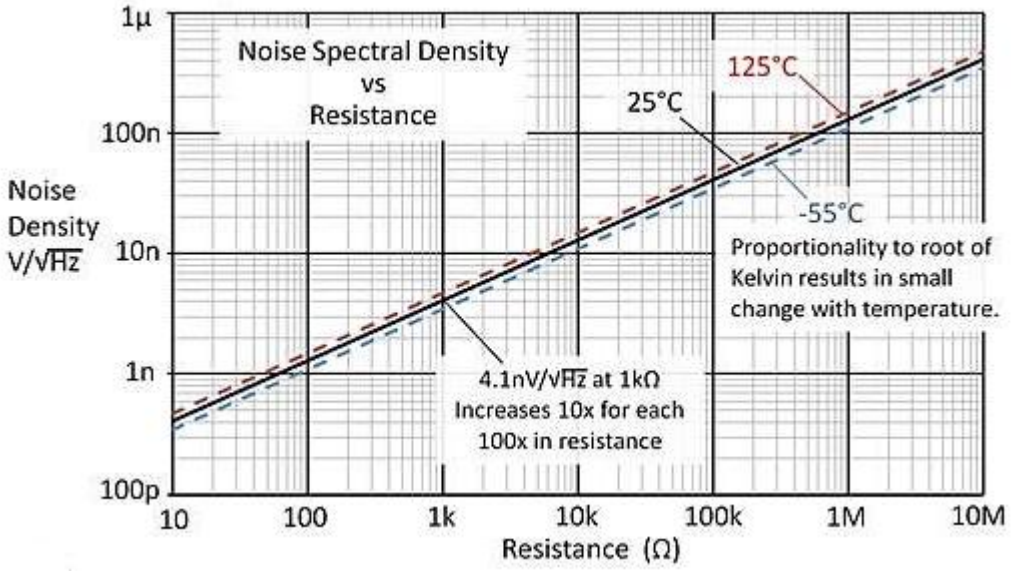
4. For a 100 kΩ resistor, attempt the following noise analysis tasks:

a. Noise power spectral density. [4 marks]

b. Noise voltage spectral density. [4 marks]

c. Describe the significant of the calculated results in parts (a) and (b). [2 marks]

d. By referring to the graph of noise density vs. resistance below, describe how resistance and temperature could influence the noise characteristics of a given resistor. [2 marks]



Solution

a. The noise power spectral density of the resistor is:

$$\begin{aligned} e_n^2 &= 4kTR \\ &= 4(1.38 \times 10^{-23})(300)(100\ \text{k}\Omega) \\ &= 1.66 \times 10^{-15}\ (\text{V}^2/\text{Hz}) \end{aligned}$$

b. The noise voltage spectral density of the resistor is:

$$\begin{aligned} e_n &= \sqrt{(4kTR)} \\ &= \sqrt{(1.66 \times 10^{-15})} \\ &= 40.7 \times 10^{-9}\ (\text{V}/\text{Hz}^{½}) \end{aligned}$$

c. At first, 40 nV/$\sqrt{\text{Hz}}$ does not sound like much. But, suppose that you design a low-noise design amplifier using a quiet op amp with an input voltage noise of only 4 nV/$\sqrt{\text{Hz}}$. Smaller R values around 1 kΩ would be a better choice.

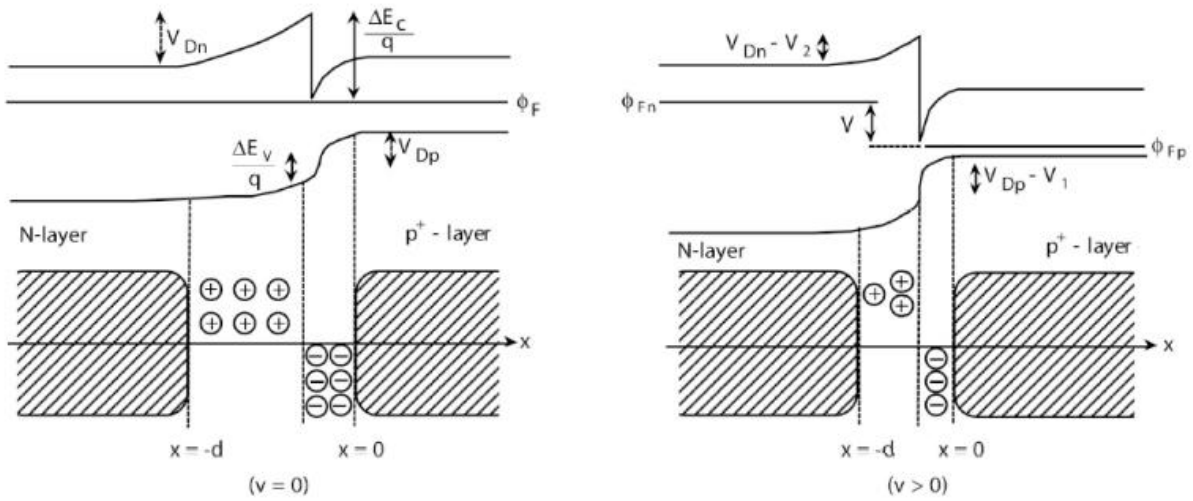
d. As shown in the given graph, the noise voltage density is linearly proportional to the resistance of the resistor. The higher the resistance, the higher the noise voltage density.

The temperature influence slightly and linearly the noise voltage density. Higher temperature could result in a slight increase of noise voltage density.

5. Noise voltage density and noise current density contributions of a PN diode are mainly due to its thermal noise of equivalent resistance in the diode and shot noise due to potential difference in the PN junction as shown below respectively.

   a. Find the signal-to-noise ratio for diode current over a 1-MHz bandwidth if (i) I_D = 1 μA and (ii) I_D = 1 nA and comment on the difference. [6 marks]

   b. Find a resistance that will produce the same amount of room-temperature noise as a diode operating with (i) a forward-bias current of 50 μA, and (ii) a reverse-bias current of 1 pA. [12 marks]



Solution

a. Before we calculate the SNR, we need to determine the noise current spectral density of the diode first.

i. At I_D = 1 μA, the noise current spectral density of the diode is:

$$I_n = \sqrt{2qI_D f_H}$$

$$= \sqrt{2(1.62 \times 10^{-19})(10^{-6})(10^{6})} = 0.57 \text{ nA (rms)}$$

The signal-to-noise ratio of the diode is:

$$\text{SNR} = 20\log_{10}\left(\frac{I_D}{I_n}\right) = 20\log_{10}\left(\frac{1 \times 10^{-6}}{0.57 \times 10^{-9}}\right) = 64.9 \text{ dB}$$

ii. By similar procedure, at I_D = 1 nA, SNR = 34.9 dB. We observe that the SNR deteriorates as the operating current is lowered.

b. The equivalent noise resistance of a resistor that corresponds to a noise of a diode is calculated as follow.

i. The thermal noise of a resistor is calculated from:

$$i_n^2 = \frac{4kT}{R} \qquad (Eq.1)$$

The shot noise in a diode is determined from:

$$i_n^2 = 2qI_D \qquad (Eq.2)$$

Assuming shot noise in the diode is equal to the thermal noise of the resistor, equate equations (1) and (2), thus:

$$\frac{4kT}{R} = 2qI_D$$

Rearranging the equation above, the equivalent noise resistance can be calculated from:

$$R = \frac{4kT}{2qI_D}$$

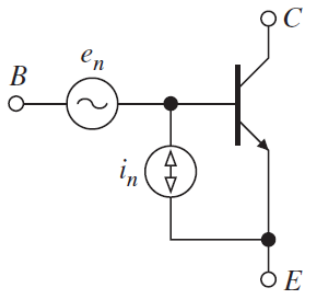
For a forward-bias current of 50 μA, the equivalent resistance is:

$$R = \frac{4kT}{2qI_D}$$

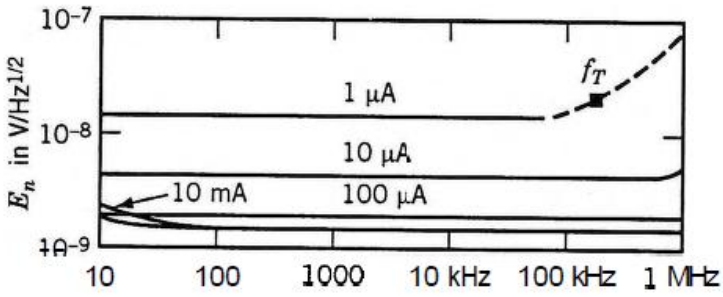
$$= \frac{4(1.38 \times 10^{-23})(298)}{2(1.6 \times 10^{-19})(50 \times 10^{-6})} = 1.03\ \text{k}\Omega$$

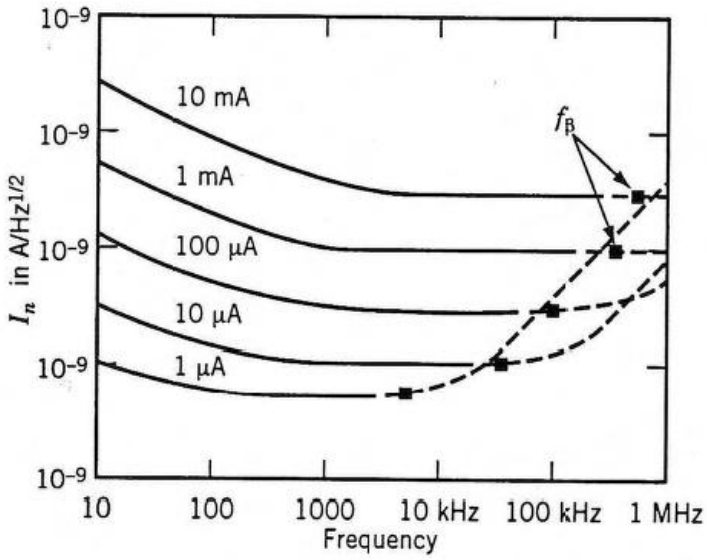
ii. By similar procedure, for a reverse-bias current of 1 pA, the equivalent resistance is 51.5 GΩ.

6. Determine the mean square equivalent input noise voltage, E_{ni}^2 for a 2N4250 BJT operating at a collector current of I_c = 1.0 mA, with a source resistance of R_s = 10 kΩ in a Δf = 10 Hz band of frequencies centred at 1 kHz.



Noise data of voltage (E_n) and current (I_n) noise densities for the 2N4250 transistor are shown in the figures below.





a. Using the graph provided above. [6 marks]

b. Using the calculation method. [6 marks]

Solution

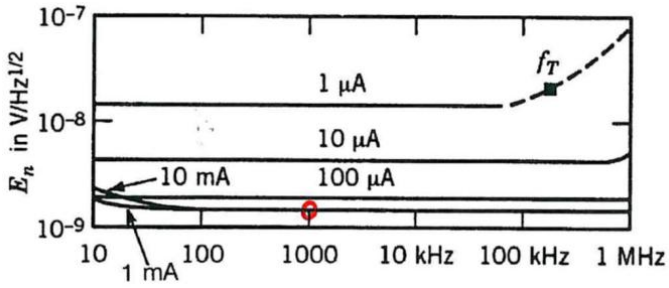
a. Using the graph provided, the noise of the given BJT transistor is determined from the following equation:

$$E_{ni}^2 = (E_t^2 + E_n^2 + I_n^2 R_s^2)\Delta f$$

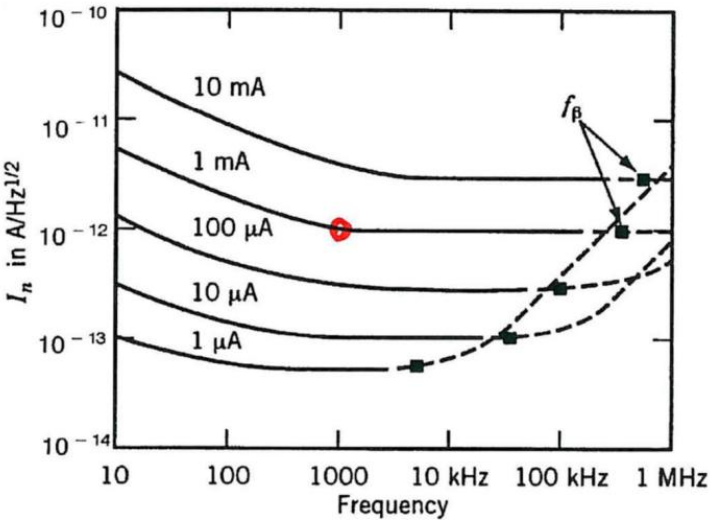
First, the noise in the source resistance, E_t can be calculated:

$$E_t^2 = 4kTR_s = 4(1.38 \times 10^{-23}\text{WsK}^{-1})(300°\text{ K})(10\text{ k}\Omega) = 1.65 \times 10^{-16}\text{ Ws}\Omega$$

The profile of the 2N4250 transistor's noise spectral voltage density, E_n at 1 kHz is as shown in the figure below.



The profile of the 2N4250 transistor's noise spectral current density, I_n at 1 kHz is as shown in the figure below.



Thus, the transistor's noise spectral voltage density, E_n and spectral current density, I_n from the figures above are E_n = 2 nV/$\sqrt{\text{Hz}}$ and I_n = 1 pA/$\sqrt{\text{Hz}}$ both read at 1 kHz.

Then, we calculate E_{ni}^2 using the equation given above:

$$E_{ni}^2 = (E_t^2 + E_n^2 + I_n^2 R_s^2)\Delta f$$
$$= [1.65 \times 10^{-16} + (2 \times 10^{-9})^2 + (10^{-12})^2 (10^4)^2](10)$$
$$= 2.64 \times 10^{-15}\ \text{V}^2/\sqrt{\text{Hz}}$$

As a result, the voltage noise spectral density of the BJT, $E_{ni} = 51.4\ \text{nV}/\sqrt{\text{Hz}}$.

In this example, the dominant noise contributions are from the thermal noise of the source resistance E_t^2 and from the $I_n^2 R_s$ term. The E_n^2 term is negligible here.

b. Using the calculation method, we must first calculate r_e, I_B, and transconductance g_m of the BJT transistor before we calculate the spectral voltage and current densities.

Considering the gain of the BJT, β is, the value of r_e is calculated from:

$$r_e \cong \frac{V_T}{I_c} = \frac{0.026}{10^{-3}} = 26\ \Omega$$

The value of I_B is calculated from:

$$I_B = \frac{I_C}{\beta} = \frac{10^{-3}}{\square}$$

The transconductance of the transistor is:

$$g_m = \frac{qI_c}{kT} = \frac{(1.6 \times 10^{-19})(10^{-3})}{(6.626 \times 10^{-34})(273° + 27°)} =$$

The voltage noise spectral density of the BJT is calculated from:

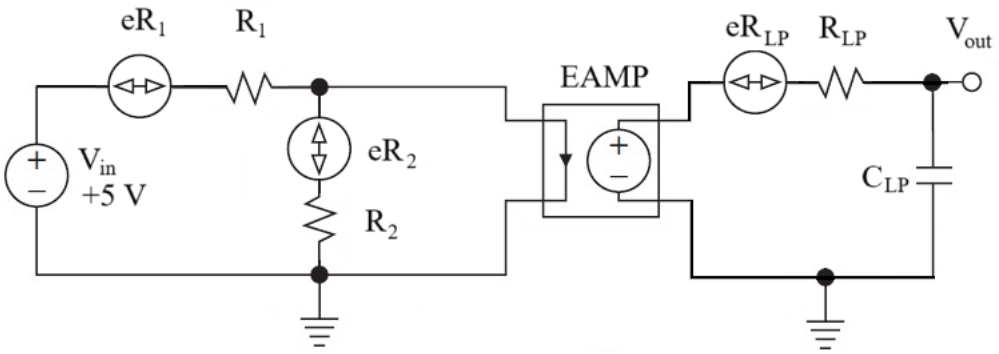
$$e_n^2(f) = 4kT\left(r_d + \frac{1}{2g_m}\right) = 4(6.626 \times 10^{-34})(273° + 27°)\left(+\frac{1}{2(\square)}\right)$$

The current noised spectral density of the BJT is calculated from:

$$i_n^2(f) = 2q\left\{I_B + \left(\frac{kI_B}{f}\right) + \frac{I_C}{[\beta(f)^2]}\right\} = 2(1.6\times10^{-19})\left\{+\frac{(6.626\times10^{-34})}{10^3} + \frac{10^{-3}}{10^2}\right\} =$$

7. Given the following equivalent circuit model of an op-amp based amplifier, our circuit below is a simple resistor divider with gain = 0.5 which is followed by a voltage amplifier with gain = 1 and a low-pass filter with f_c = 1 MHz. Resistors R_1 = R_2 = 100 kΩ and R_{LP} = 100 Ω and capacitor C_{LP} = 1 µF.

   Notice that the voltage amplifier EAMP does not have any internal noise source and all noise sources in the circuit are from thermal noise of the resistors. Assuming we are seeking the noise density at low frequencies where the low-pass filter has no effect.



   Determine how much noise from various resistors contribute at the output of the circuit by calculating the following parameters in the noise analysis:

   a. Noise power spectral density of R_1. [4 marks]

   b. Output noise power spectral density from R_1. [8 marks]

   c. Output noise power spectral density from R_2. [4 marks]

   d. Output noise power spectral density from R_{LP}. [4 marks]

   e. Total output noise power spectral density. [4 marks]

   f. Total output noise voltage spectral density. [4 marks]

Solution

We calculate the contribution of the resistors in the circuit towards the total noise of the circuit.

a. First, calculate the noise power spectral density, e_n^2 from R_1 = 100 kΩ.

$$\begin{aligned} e_n^2 &= 4kTR \\ &= 4(1.38\times10^{-23})(300)(100\ \text{k}\Omega) \\ &= 1.66\times10^{-15}\ (\text{V}^2\text{Hz}^{-1}) \end{aligned}$$

b. Find the voltage gain A_v from the noise source to the output

$$A_v = \frac{R_2}{R_1 + R_2} = \frac{1}{2}$$

Then, applying superposition principle in the circuit, calculate the noise spectral density of each of the noise source and its contribution towards the overall noise at the output of the given amplifier circuit.

Thus, use A_v to calculate the output noise power spectral density of R_1. Notice A^2 is actually used because we are dealing with power here. For R_1 = 100 kΩ, its noise power density at the output of the amplifier circuit is:

$$\begin{aligned} e_{no(R1)}^2 &= e_{nR1}^2 A^2 \\ &= (1.66 \times 10^{-15}) \left(\frac{1}{2}\right)^2 \\ &= 4.14 \times 10^{-16}\ (\mathrm{V^2 Hz^{-1}}) \end{aligned}$$

c. For R_2 = 100 kΩ, we get the same answer as R_1, that is:

$$\begin{aligned} e_{no(R2)}^2 &= e_{nR2}^2 A^2 \\ &= 1.66 \times 10^{-15} \left(\frac{1}{2}\right)^2 \\ &= 4.14 \times 10^{-16}\ (\mathrm{V^2 Hz^{-1}}) \end{aligned}$$

d. For R_{LP} = 100 Ω, we get:

$$\begin{aligned} e_{no(RLP)}^2 &= e_{nRLP}^2 A^2 \\ &= 1.66 \times 10^{-18}\ (1)^2 \\ &= 1.66 \times 10^{-18}\ (\mathrm{V^2 Hz^{-1}}) \end{aligned}$$

e. Adding the contributions from all resistors, we get a total noise power spectral density of:

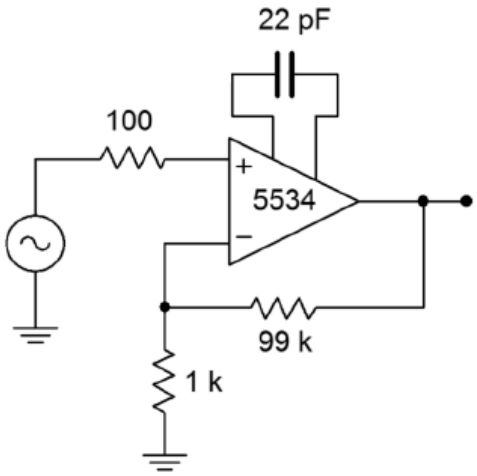
$$\begin{aligned} e_{tot}^2 &= e_{no(R1)}^2 + e_{no(R2)}^2 + e_{no(RLP)}^2 \\ &= 4.14 \times 10^{-16} + 4.14 \times 10^{-16} + 1.66 \times 10^{-18} \\ &= 8.30 \times 10^{-16}\ (\mathrm{V^2 Hz^{-1}}) \end{aligned}$$

f. Now take the square root to get the total noise voltage spectral density of:

$$\begin{aligned} e_{no(tot)} &= \sqrt{(8.30 \times 10^{-16})} \\ &= 2.88 \times 10^{-8}\ (\mathrm{V\sqrt{Hz}}) \end{aligned}$$

At low frequencies, the resistors in the circuit contribute a total of 28.8 nV/$\sqrt{\mathrm{Hz}}$ at the circuit's output noise.

8. You are given an op-amp based amplifier circuit as shown in the figure below. Notice that the op amp in the circuit is already compensated with a 22 pF capacitor. So, its operational characteristics are different from uncompensated op amp.



The manufacturer datasheet of NE5534 shows the following specs, V_n = 4 nV/$\sqrt{\text{Hz}}$, I_n = 0.6 pA/$\sqrt{\text{Hz}}$. These values do rise at lower frequencies, but we will ignore this effect for now. Also, f_{unity} is 10 MHz.

a. Determine the output noise voltage for the circuit. [20 marks]

b. For a nominal output of 1 V (rms), what is the signal-to-noise ratio? Assume T = 300° Kelvin (room temperature). [4 marks]

Solution

a. The voltage gain of the non-inverting amplifier is:

$$A_v = 1 + \left(\frac{R_f}{R_i}\right)$$

$$= 1 + \left(\frac{99\ \text{k}\Omega}{1\ \text{k}\Omega}\right) = 100 = 40\ \text{dB}$$

For the non-inverting amplifier, $A_v = A_{noise}$, so the noise gain of the amplifier is:

$$A_{noise} = 100 = 40\ \text{dB}$$

The total noise resistance at the input is:

$$R_{noise} = R_s + \left(R_f \parallel R_i\right)$$

$$= 100 + (99\ \text{k}\Omega \parallel 1\text{k}\Omega) = 1090\ \Omega$$

The noise voltage density of the Thevenin equivalent resistors in the amplifier is:

$$e_{th}^2 = 4\text{k}\text{T}R_{noise}$$

$$= 4(1.38 \times 10^{-23})(300)(1090\ \Omega)$$

$$= 1.805 \times 10^{-17}\ \text{V}^2/\text{Hz}$$

Knowing V_n = 4 nV/$\sqrt{\text{Hz}}$, I_n = 0.6 pA/$\sqrt{\text{Hz}}$, the total noise voltage of the amplifier is:

$$e_{total} = \sqrt{V_n^2 + (I_n R_{noise})^2 + e_{th}^2}$$

$$= \sqrt{(4 \times 10^{-9})^2 + (0.6 \times 10^{-12} \times 1090\ \Omega)^2 + 1.805 \times 10^{-17}}$$

$$= \sqrt{1.6 \times 10^{-17} + 4.277 \times 10^{-19} + 1.805 \times 10^{-17}}$$

$$= 5.87 \times 10^{-9}\ \text{V}/\sqrt{\text{Hz}}$$

Note that the major noise contributors are V_n and e_{th}. Now, to find BW_{noise}.

The cut-off frequency of the amplifier is:

$$f_c = \frac{f_{unity}}{A_{noise}} = \frac{10\ \text{MHz}}{100} = 100\ \text{kHz}$$

The noise bandwidth of the amplifier is:

$$\text{BW}_{noise} = 1.57 f_c$$

$$= 1.57(100\ \text{kHz}) = 157\ \text{kHz}$$

The noise voltage density of the amplifier is:

$$e_n = e_{total}\sqrt{\text{BW}_{noise}}$$

$$= (5.87 \times 10^{-9})\sqrt{157 \times 10^3} = 2.33 \times 10^{-6}\ \text{V (rms)}$$

To find the noise voltage at the output of amplifier circuit, multiply noise voltage density by the noise gain.

$$e_{n(out)} = e_n A_{noise}$$

$$= (2.33 \times 10^{-6})(100) = 233 \times 10^{-6}\ \text{V (rms)}$$

b. For a nominal output signal of 1 V (rms), the signal-to-noise ratio (SNR) is:

$$\text{SNR} = \frac{\text{Signal}}{\text{Noise}}$$

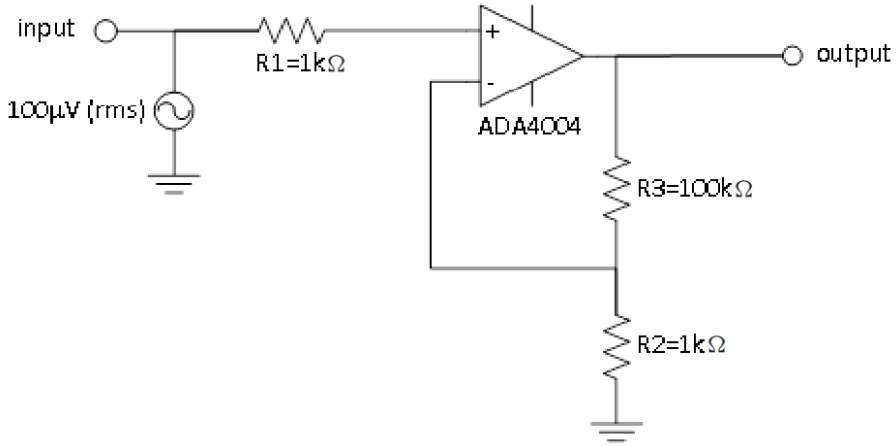
$$= \frac{1\ \text{V}}{233 \times 10^{-6}\ \text{V}} = 4{,}290$$

Normally SNR is given in dB, it is:

$$\text{SNR(dB)} = 20 \log(\text{SNR})$$

$$= 20 \log 4290 = 72.6\ \text{dB}$$

9. Given in the circuit below is a non-inverting audio preamplifier with operating frequency of 100 Hz to 20 kHz.



From the datasheet of AD4004 op amp (at V_{CC} = ±15 Volts and T_A = 25° C):

- Noise voltage density at 1 kHz, $V_{n(OA)}$ = 1.8 nV/$\sqrt{\text{Hz}}$
- Noise current density at 200 Hz, $I_{n(OA)}$ = 1.2 pA/$\sqrt{\text{Hz}}$

The non-inverting amplifier, at operating bandwidth of the circuit from 100 Hz to 20 kHz, is connected with a 100 μV (rms) signal source.

a. Determine noise model of the circuit with all noise sources included. [5 marks]

b. Determine the gain of non-inverting and inverting amplifiers. [4 marks]

c. Determine the noise spectral density of 1kΩ and 100kΩ resistors at 25°C. [4 marks]

d. Calculate the noise voltage densities at the output of the amplifier circuit due to the resistors in the circuit. [6 marks]

e. Calculate the noise voltage densities at the output of the amplifier circuit due to the op amp noise sources. [6 marks]

f. Calculate the total noise voltage densities at the output of the amplifier. [4 marks]

g. Calculate total noise at the output of the op amp. [4 marks]

h. Determine signal-to-noise ratio of the amplifier circuit at input. [6 marks]

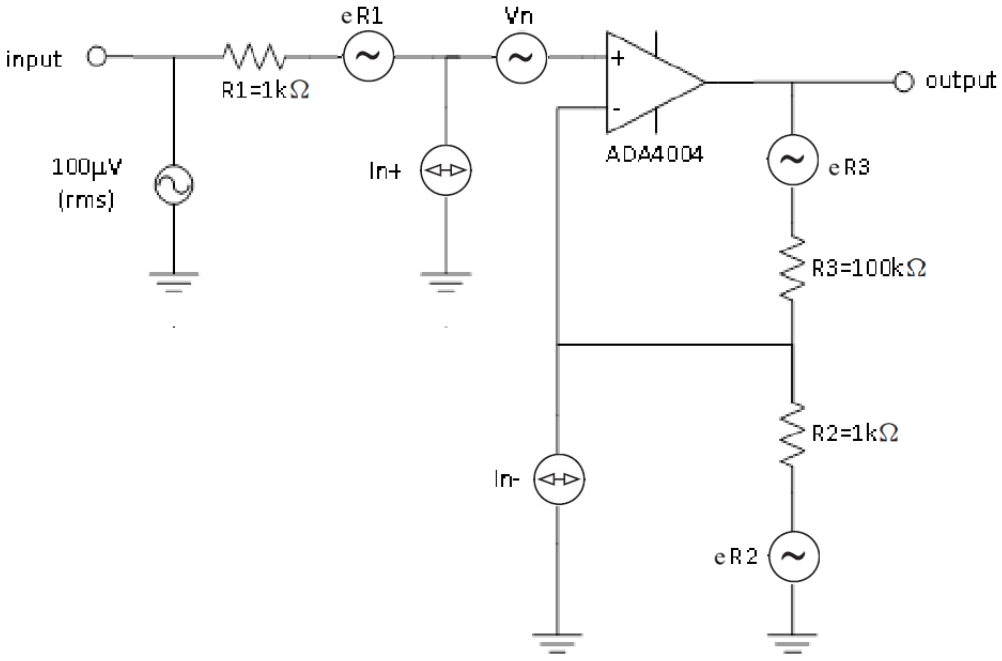
i. Determine signal-to-noise ratio of the amplifier circuit at output. [6 marks]

j. Determine noise factor of the circuit. [2 marks]

k. Determine noise figure of the circuit. [2 marks]

Solution

a. The circuit of the non-inverting amplifier given above with all noise sources included is as shown below.



In the given noise analysis model, we have noise sources represented as independent voltage sources that are related to the resistors and noise sources in the op amp in the circuit.

The noise sources from the resistors are noise sources related to R_1, R_2 and R_3 resistors in the circuit.

The noise sources in the op amp are modelled as (differential) noise source voltage source ($V_n(OA)$), non-inverting noise current source ($I_n(OA+)$) and inverting noise current source ($I_n(OA+)$).

b. For the non-inverting amplifier given above:

The gain of non-inverting the amplifier is given as:

$$A_v(\text{non} - \text{inverting}) = 1 + \left(\frac{R_2}{R_1}\right) = 1 + \left(\frac{100\ \text{k}\Omega}{1\ \text{k}\Omega}\right) = 101$$

The gain of the inverting amplifier is given as:

$$A_v(\text{inverting}) = -\left(\frac{R_2}{R_1}\right) = -\left(\frac{100\ \text{k}\Omega}{1\ \text{k}\Omega}\right) = -100$$

c. Thermal/Johnson noise spectral density for a resistor is:

$$V_n = \sqrt{4\text{kTR}}$$

Where:

k = Boltzmann's constant (1.374 x 10^{-23} J/K)
T = temperature in Kelvin (°C + 273.16),

R = resistance in ohms

Thermal/Johnson noise spectral density for a 1 kΩ resistor at 25°C is:

$$V_n(1\text{k}) = \sqrt{4\text{kTR}}$$
$$= \sqrt{4(1.374 \times 10^{-23})(25 + 273.16)(10^3)}$$
$$= 4 \text{ nV}/\sqrt{\text{Hz}}$$

Thermal/Johnson noise spectral density for a 100 kΩ resistor at 25°C is:

$$V_n(100\text{k}) = \sqrt{4\text{kTR}}$$
$$= \sqrt{4(1.374 \times 10^{-23})(25 + 273.16)(100 \times 10^3)}$$
$$= 40 \text{ nV}/\sqrt{\text{Hz}}$$

d. Noise sources due to resistors in the circuits e.g. R_1, R_2 and R_3 resistors:

Noise voltage density due to 1 kΩ resistor of R_1:

$$V_n(R_1) = V_n(1\text{ k}\Omega) \times A_v(\text{non} - \text{inverting})$$
$$= 4\text{nV}/\sqrt{\text{Hz}} \times 101$$
$$= 404 \times 10^{-9}\text{ V}/\sqrt{\text{Hz}}$$

Noise voltage density due to 1 kΩ resistor of R_2:

$$V_n(R_2) = V_n(1\text{ k}\Omega) \times A_v(\text{inverting})$$
$$= 4\text{nV}/\sqrt{\text{Hz}} \times 100$$
$$= 400 \times 10^{-9}\text{ V}/\sqrt{\text{Hz}}$$

Noise voltage density due to 100 kΩ resistor of R_3:

$$V_n(R_3) = V_n(100\text{ k}\Omega)$$
$$= 40\text{nV}/\sqrt{\text{Hz}}$$
$$= 40 \times 10^{-9}\text{ V}/\sqrt{\text{Hz}}$$

e. Noise sources of the op amp are transformed to the output side of the op amp (with current sources of the op amp are also transformed to noise voltage densities):

Noise voltage density of the noise voltage source of the op amp at the non-inverting pin:

$$V_n(OA) = V_n(OA) \times A_v(\text{non} - \text{inverting})$$
$$= 1.8\text{nV}/\sqrt{\text{Hz}} \times 101$$
$$= 182 \times 10^{-9}\text{ V}/\sqrt{\text{Hz}}$$

Noise voltage density due to noise current source of the op amp at the non-inverting pin:

$$V_n(OA+) = I_n(OA+) \times R_1 \times A_v(\text{non}-\text{inverting})$$
$$= 1.2 \times 10^{-12} \times 10^3 \times 101 = 121 \times 10^{-9}\ \text{V}/\sqrt{\text{Hz}}$$

Noise voltage density due to noise current source of the op amp at the inverting pin:

$$V_n(OA-) = I_n(OA-) \times R_3 \times A_v(\text{inverting})$$
$$= 1.2 \times 10^{-12} \times 10^3 \times 100 = 120 \times 10^{-9}\ \text{V}/\sqrt{\text{Hz}}$$

f. The total noise voltage density in the output of the amplifier is the quadrature sum of noise voltage densities of all noise sources at the output of the amplifier:

$$V_n(\text{out}) = \sqrt{(V_n(\text{R}_1))^2+(V_n(\text{R}_2))^2+(V_n(\text{R}_3))^2+(V_n(\text{OA}))^2+(V_n(\text{OA+}))^2+(V_n(\text{OA-}))^2}$$
$$= \sqrt{(404)^2 + (400)^2 + (40)^2 + (182)^2 + (121)^2 + (120)^2}$$
$$= 622 \times 10^{-9}\ \text{V}/\sqrt{\text{Hz}}$$

The total noise voltage density in the output of the amplifier is 622 nV/$\sqrt{\text{Hz}}$

g. For a bandwidth of the circuit (BW) from 100 Hz to 20 kHz, then the noise at the output of amplifier is:

$$V_n(\text{total}) = V_n(\text{out}) \times \sqrt{\text{BW}} = (622 \times 10^{-9})\sqrt{20 \times 10^3 - 100} \cong 87.7 \times 10^{-6}\ \text{V (rms)}$$

The noise at the output of the amplifier is found to be approximately 87.7 μV (rms).

h. Signal-to-noise ratio (SNR) of the amplifier circuit at the input:

The signal at the input of the circuit is:

$$V(\text{input}) = 100 \times 10^{-6}\ \text{V(rms)}$$

The noise at the input is due to R_1 = 1 kΩ resistor, and knowing that the bandwidth of the circuit (BW) is from 100 Hz to 10 kHz, the noise at the input is approximately:

$$V_n(R_1) = V_n(1\ \text{k}\Omega) \times \sqrt{\text{BW}} = 4 \times 10^{-9} \times \sqrt{20 \times 10^3 - 100} \cong 0.56 \times 10^{-6}\ \text{V}$$

As a result, the signal-to-noise ratio (SNR) at the input of the amplifier is found to be:

$$\text{SNR(input)} = \frac{\text{Signal(input)}}{\text{Noise(input)}} = \frac{100 \times 10^{-6}}{0.56 \times 10^{-6}} = 178.6$$

If it is in dB:

$$\text{SNR}_{\text{dB}}(\text{input}) = 20 \log \text{SNR(input)} = 20 \log(178.6) = 45\ \text{dB}$$

The SNR at the input of the amplifier circuit is 45 dB.

i. Signal-to-noise ratio (SNR) of the amplifier circuit at the output:

The signal at the output is found from:

$$V(\text{output}) = V(\text{input}) \times A_v(\text{non} - \text{inverting}) = (100 \times 10^{-6})(101) = 10.1 \times 10^{-3}\ \text{V}$$

The noise at the output, $V_n(\text{output}) = 87.7 \times 10^{-6}\ \text{V(rms)}$, so the signal-to-noise ratio (SNR) at the output of the amplifier is found to be:

$$\text{SNR(output)} = \frac{\text{Signal(output)}}{\text{Noise(output)}} = \frac{10.1 \times 10^{-3}}{87.7 \times 10^{-6}} = 115.17$$

If it is in dB:

$$\text{SNR}_{\text{dB}}(\text{output}) = 20 \log \text{SNR(output)} = 20 \log(115.17) = 41.22\ \text{dB}$$

The SNR at the output of the amplifier circuit is 41.22 dB.

j. Noise factor (F) of the amplifier circuit:

$$F = \frac{\text{SNR(input)}}{\text{SNR(output)}} = \frac{178.6}{115.17} = 1.55$$

As a result, the noise factor of the amplifier circuit is 1.55.

k. Noise figure (NF) of the amplifier circuit:

$$NF = 20 \log F = 20 \log(1.55) = 3.81\ \text{dB}$$

As a result, the noise figure of the amplifier circuit is 3.81 dB.