Victoria University of Wellington

DEGREE EXAMINATIONS — 2001   COMP203

END-YEAR

COMP 203

Computer Organisation

Time Allowed: 3 Hours (180 minutes)

Instructions:
- Attempt all questions.
- Make sure your answers are clear and to the point.
- Non-programmable calculators without full alphabetic keys are permitted.
- Non-electronic foreign language dictionaries are permitted.
- No reference material is allowed.
- There are 180 possible marks on the exam.
- Answer in the appropriate heavily outlined boxes or follow the instructions given in the questions.

Question	Topic	Marks
1	General	*10 marks*
2	Machine Language	*20 marks*
3	Arithmetic	*30 marks*
4	Logic Design Basics	*20 marks*
5	Processor Data Path and Control	*25 marks*
6	Pipelined Data Path	*25 marks*
7	Memory Hierarchy	*15 marks*
8	Input/ Output	*35 marks*

Question 1: Basic Concepts   [10 marks]

Given the words/phrases below:

1)	Assembler	7)	Binary number
2)	Memory	8)	Bit
3)	CPU	9)	Cache
4)	Datapath	10)	Controller
5)	Compiler	11)	DRAM
6)	Operating System	12)	Instruction

Select the word or phrase from the list above that best matches the description in the following questions. Write the number of your answer for each question. Each word/phrase should be used only once.

A. Active part of the computer, following the instructions of the programs to the letter. It adds numbers, tests numbers, and so on.
B. Base 2 number.
C. Binary digit.
D. Component of the processor that performs arithmetic operations.
E. Component of the processor that tells the datapath, memory, and I/O devices what to do according to the instructions of the program.
F. Individual command to a computer.
G. Integrated circuit commonly used to construct main memory.
H. Location of programs when they are running, containing the data needed as well.
I. Program that manages the resources of a computer for the benefit of the programs that run on that machine.
J. Program that translates a symbolic version of an instruction into the binary version.
K. Program that translates from a high level notation to assembly language.
L. Small, fast memory that acts as a buffer from the main memory.

ANSWER

A: [   ]   B: [   ]   C: [   ]   D: [   ]

E: [   ]   F: [   ]   G: [   ]   H: [   ]

I: [   ]   J: [   ]   K: [   ]   L: [   ]

Question 2: Machine Language   [20 marks]

a) [7 marks] Write a sequence of MIPS instructions for the following C
statement:

```
a[10] = a[1] + b;
```

Assume that register *$t0* holds variable `b` and the array `a` has a base
address of `0x0356a450`.

ANSWER

b) [13 marks] Consider the following fragment of C code:

```
/*  while-loop  */
i = 0;
while (i < 100)
{
    a[i] = b[i] + c;
    i++;
}
```

Assume that `a` and `b` are arrays of words, the base address of array `a` is in register *$s0* and the base address of array `b` is in *$s1*. Register *$s2* holds variable *i* and *$s3* holds `c`.

Write a sequence of MIPS instructions that directly corresponds to the `while-loop` fragment. Use temporary registers if necessary.

ANSWER

Question 3: Computer Arithmetic   [30 marks]

a) **[10 marks]** The question focuses on number conversion. Write the **final results only** in the space provided.

I. **[3 marks]** Convert -1024 (decimal) to a 16-bit 2's complement binary number.

ANSWER

II. **[2 marks]** Convert 1111 1111 1111 1111 1111 1111 1111 1111 (2's complement binary) into a decimal number.

ANSWER

III. [3 marks] Convert –0.0625 (decimal) into IEEE 754 binary representation in single precision.

ANSWER

IV. [2 marks] Convert the decimal number 0 into single precision IEEE 754 binary number.

ANSWER

b) [20 marks] This question concerns overflow detection and manipulation.

I. [4 marks] For the following integer addition:

$$C = A + B$$

Suppose that we use signs of the three operands to detect overflows. List all possibilities where an overflow occurs.

ANSWER

II. [4 marks] Write **two** MIPS instructions to determine if there is a carry out of two registers, say, registers $t3 and $t4. Place a 0 or 1 in register $t2 if the carry out is 0 or 1, respectively. Use temporary registers if necessary.
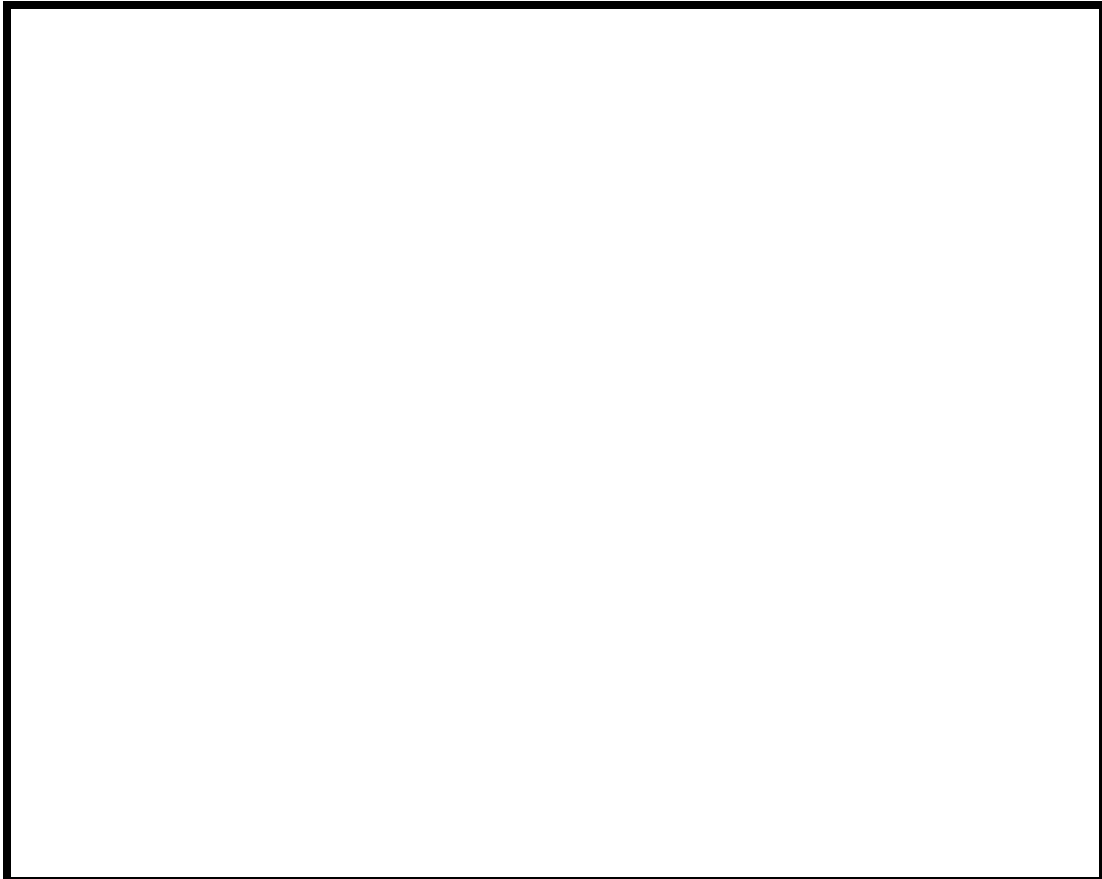
ANSWER

COMP 203   **continued**

III. **[12 marks]** Suppose that two **positive integers** are placed in registers \$t1 and \$t2. Write **at most 7** MIPS instructions to perform the following steps:

- Place the sum of \$t1 and \$t2 in register \$t3;

- if there is no overflow, subtract 5 from the sum and place the result in register \$t4;

- if overflow occurs, set the most significant bit of the sum (\$t3) to 0, and place a carry out of 1 in register \$t5.

Use temporary registers if necessary.

ANSWER

SPARE PAGE FOR EXTRA ANSWERS

Cross out the rough working that you do not want marked.
Specify the question number for work you do want marked.

Question 4: Logic Design Basics   [20 marks]

a) Consider the combinational logic block shown in Figure 4.1.
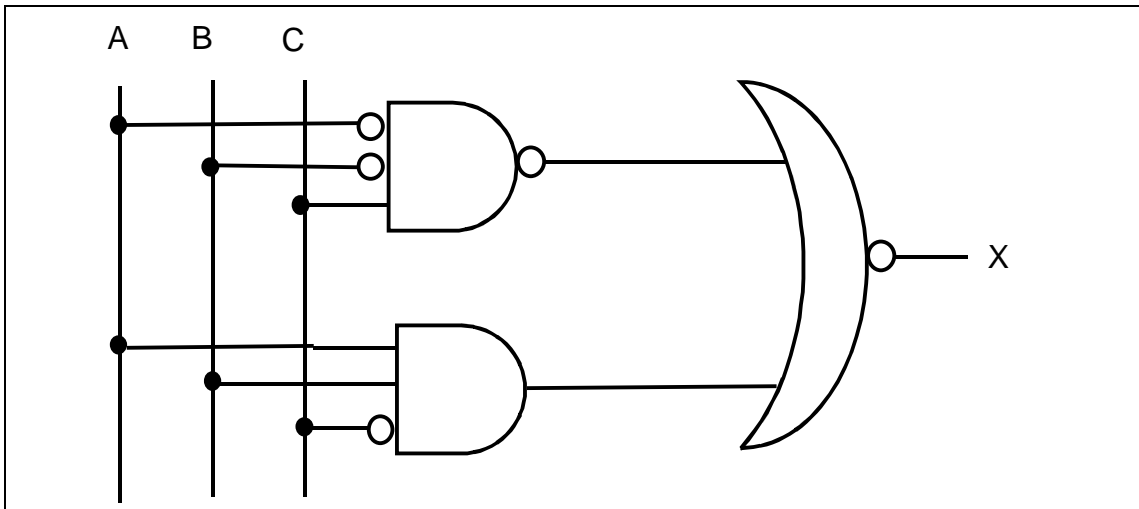

Figure 4.1.

  I. **[3 marks]** Write the Boolean output function X in the form that directly follows from the Figure 4.1 in terms of inputs A, B, and C.

ANSWER

  II. **[5 marks]** Draw a truth table for X.

ANSWER

III. **[2 marks]** Express the resulting output function X in the minimal form.

ANSWER

```



```

b) Describe the operation of a Flip Flop considering it a primitive Finite State Machine (FSM). When describing it:

I. **[5 marks]** Use a State Transition Table (Next State Table) having current state Q, input D, and next state Q'.

ANSWER

```



```

II. **[5 marks]** Use a State Transition Diagram to represent it graphically.

ANSWER

```



```

COMP 203   **continued**

Question 5: Processor DataPath&Control [25 marks]

a) [7.5 marks] Consider the Figure 5.1 showing the MIPS single cycle data path.

Take a pen or pencil and clearly designate on the drawing all the lines and all the equipment (like: PC, memory, register file, multiplexors, ALUs) that will be used to fetch and execute a **beq** MIPS instruction by:
- tracing the lines, and
- circling the equipment.

Designate lines and equipment that will be used in the case the branch instruction is taken and in the case it is not.

COMP 203   **continued**

Figure 5.1.

continued
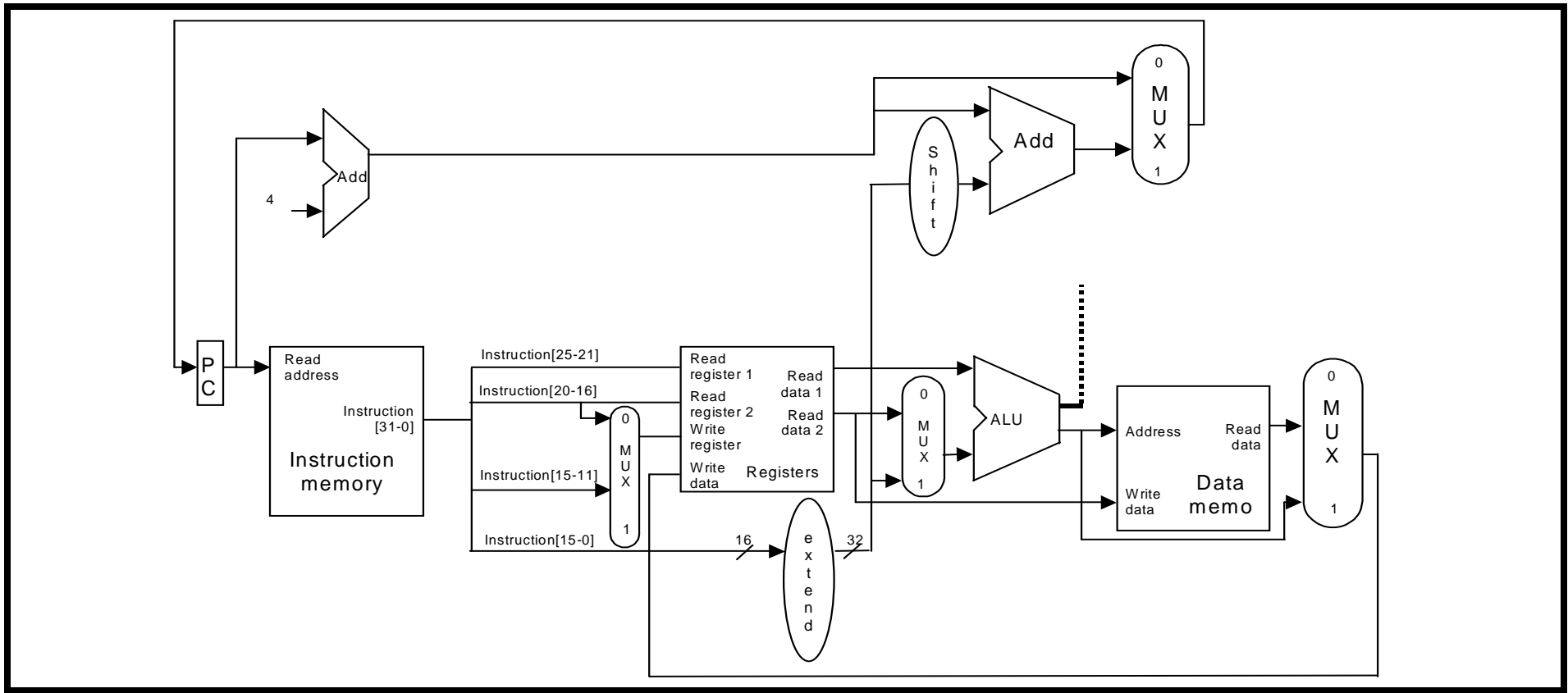
b) [7.5 marks] Consider the Figure 5.2 showing the MIPS multi-cycle data path.

Take a pen or pencil and clearly designate on the drawing all the lines and all the equipment (like: PC, memory, register file, multiplexors, ALUs) that will be used to fetch and execute an **lw** MIPS instruction by:
- tracing the lines, and
- circling the equipment.

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Figure 5.2.

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c) [10 marks] The microinstructions of the multi-cycle processor data path are given in the table Q5.

Table Q5

Address	Label	ALU	SRC1	SRC2	Reg. Con.	Memory	PC Write	Sequen-Cing
1	Fetch	Add	PC	4		Read PC	ALU	Seq
2		Add	PC	Extshft	Read			Dispatch1
3	Mem1	Add	Rs	Extend				Dispatch2
4	LW2					Read ALU		Seq
5					Write Rt			Fetch
6	SW2					Write ALU		Fetch
7	Rfrmt1	Fun-code	Rs	Rt				Seq
8					Write ALU			Fetch
9	BEQ1	Subt	Rs	Rt			Zero	Fetch
10	JUMP1						Jump addr	Fetch

Write the micro code sequence for the MIPS **lw** instruction by copying only the appropriate microinstructions (the addresses will be sufficient) from the Table Q5 into the Table Q5 - ANSWER provided for your answer.

Table Q5 – ANSWER

Address	Label	ALU	SRC1	SRC2	Reg. Con.	Memory	PC Write	Sequen-Cing

COMP 203   **continued**

SPARE PAGE FOR EXTRA ANSWERS

Cross out the rough working that you do not want marked.
Specify the question number for work you do want marked.
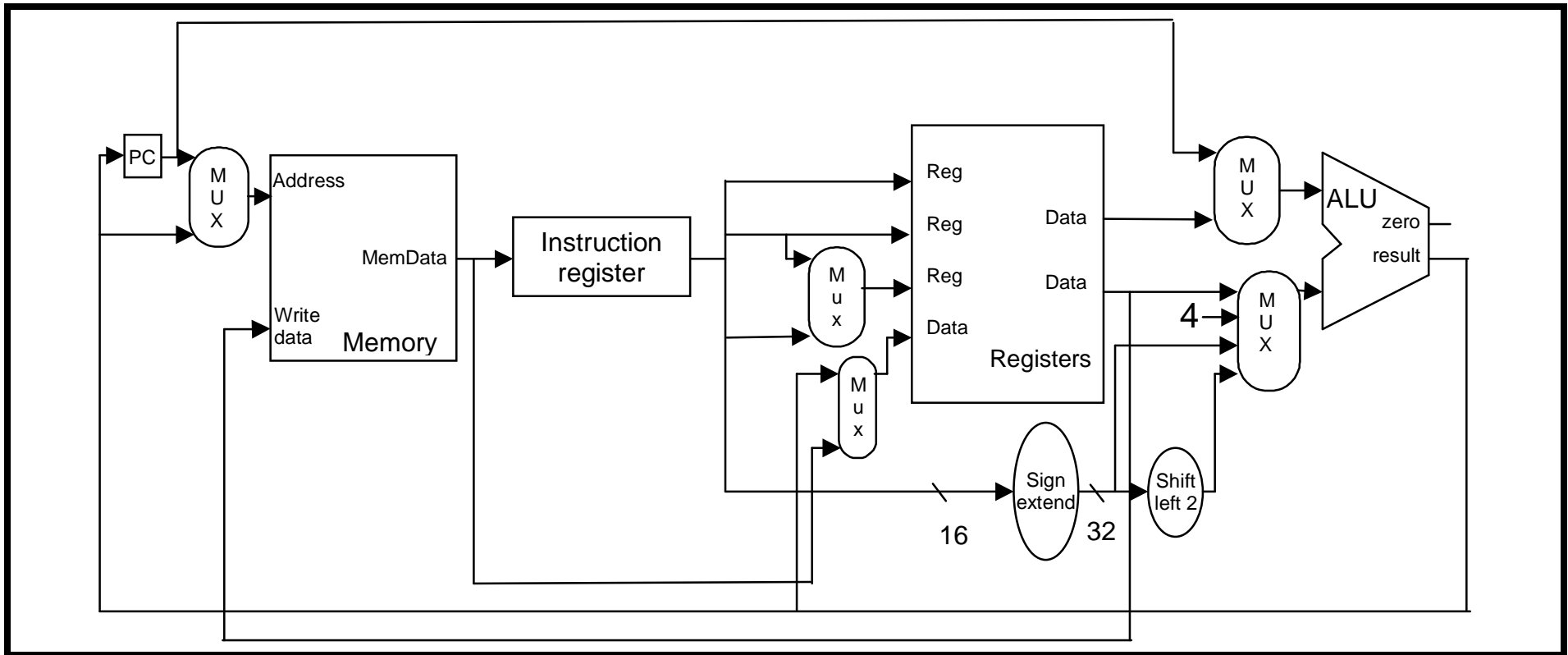
Question 6: Pipelined Data Path [25 marks]

a) **[5 marks]** Consider the Figure 6.1 that contains the forwarding part of the pipelined MIPS datapath.

Take a pen or pencil and clearly designate on the drawing all the lines and all the equipment (like: PC, memory, register file, multiplexors, ALUs) that will be used to forward data to any of the ALU inputs when executing an **lw** MIPS instruction by:
- tracing the lines, and
- circling the equipment.

Consider only data path and exclude control when answering this question.
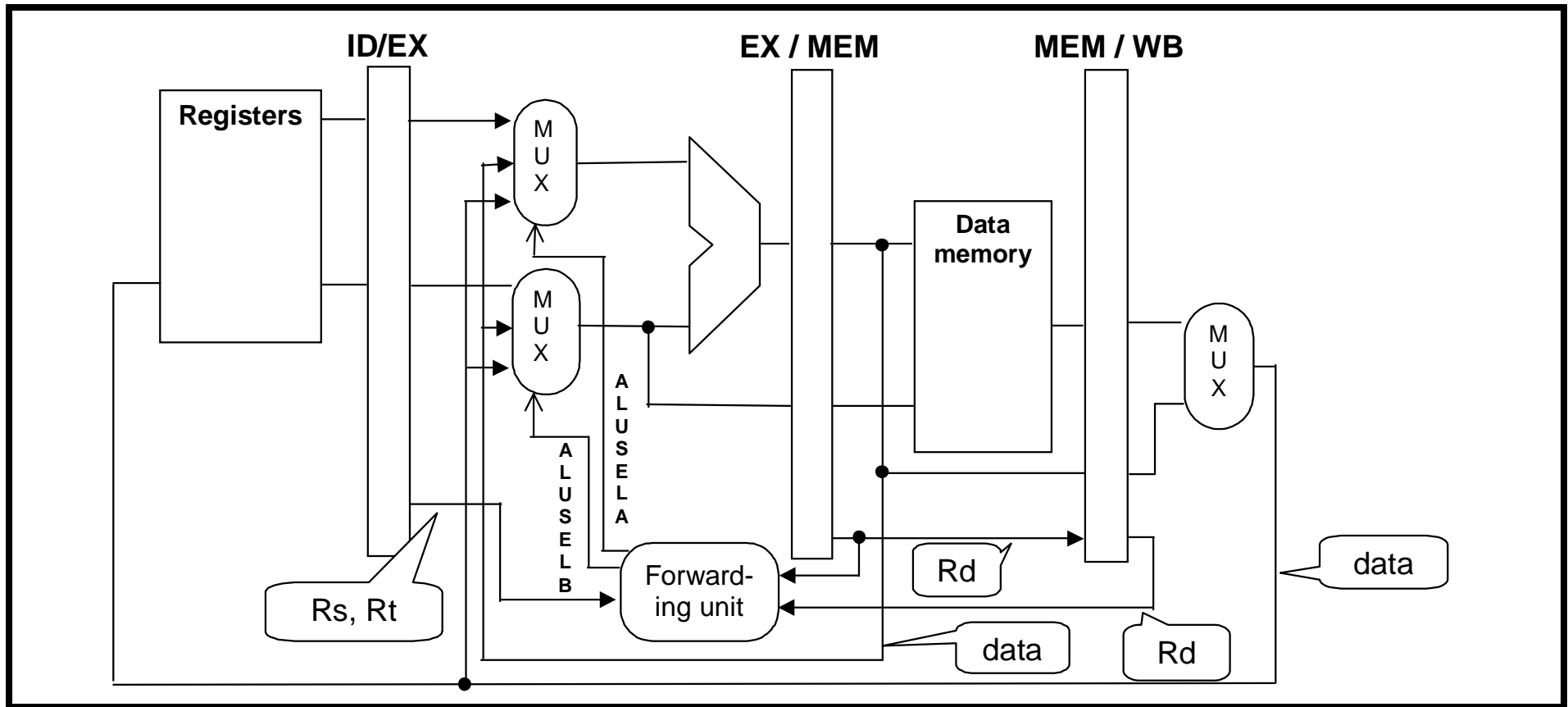
Figure 6.1.

b) The pipelined data path stages for some MIPS instructions are given in the table Q8. The table contents show at which stage:
- source registers are read from the register file,
- source is needed at the ALU inputs,
- the result is delivered to the register file, and
- the result is forwarded to the ALU input.

Table Q8

Instruction	Stage when source read from register file	Stage when source needed at ALU input	Stage when result written into register file	Stage when result forwarded to ALU input
Add	2	3	5	4
Sub	2	3	5	4
Lw	2	3	5	5

Consider the following code:

add $5, $6, $7
lw $6, 100($7)
sub $7, $6, $8

Suppose: The ALU needs a source at the start of the stage, and a result is forwarded at the end of the stage.

I. [5 marks] Identify all of the data dependencies in the code given, insert no operations into the appropriate locations, and indicate how many of nops are required to clear hazards.

ANSWER

II. Assuming that registers had the following values before the first instruction:
- $5 = 0,
- $6 = 4,
- $7 = 0,
- $8 = 4

and the memory location with address 100 had value 10,
- **[5 marks]** What would be the content of the register $7 after the third instruction if the data path **could not** detect hazards?

ANSWER

- **[5 marks]** What would be the content of the register $7 after the third instruction if the data path **could** detect hazards?

ANSWER

III. **[5 marks]** Optimize the code given by swapping the instructions, instead of inserting no operations, and show the redesigned code.

ANSWER

SPARE PAGE FOR EXTRA ANSWERS

Cross out the rough working that you do not want marked.
Specify the question number for work you do want marked.

Question 7. Memory Hierarchy [15 marks]

The 4 – way 32 slots set associative cache with one word per block is presented in Figure 7.1.

Slot	V_0	Tag_0	W_0	V_1	Tag_1	W_1	V_2	Tag_2	W_2	V_3	Tag_3	W_3
000	1	11100	A	1	11010	B	0			1	00000	C
001	1	11100	E	0			0			0		
010	0			0			0			0		
011	1	11100	D	1	01100	C	0			0		
100	0			0			0			0		
101	0			0			0			0		
110	0			0			0			0		
111	1	11100	F	0			0			0		

Figure 7.1

Suppose the cache has the contents as in the Figure 7.1, and then the processor issues the following data requests as a sequence of byte addresses:

11 1000 1100
01 1000 0000
11 1000 0100
01 1001 1100
01 1000 0000

a) **[10 marks]** Show the contents of the cache after all these 5 processor requests. (Denote the new words in the cache with capital letters G, H, …)

ANSWER

Slot	V_0	Tag_0	W_0	V_1	Tag_1	W_1	V_2	Tag_2	W_2	V_3	Tag_3	W_3
000												
001												
010												
011												
100												
101												
110												
111												

b) **[5 marks]** Calculate the miss rate from these 5 processor requests.

ANSWER

Question 8. Input/Output   [35 marks]

a) [10 marks] A program performs a three-step process:

- It reads in a 4-KB block from a random location on disk,
- It does some processing on that data, and then
- It writes out the result as another 4-KB block elsewhere on the disk.

Suppose:

- Each block is contiguously located on a single track on the disk.
- The disk drive rotates at 6000 RPM.
- The disk has an average seek time of 7 ms.
- The disk has a transfer rate of 4 MB/sec.
- The controller overhead is 1.5 ms.
- No other program is using the disk or processor, and there is no overlapping of disk operation with processing.
- The processing step takes 200,000 clock cycles, and the processor clock rate is 400MHz.

How long will it take in average to perform the described process?

ANSWER

b) [10 marks] Controlling data transfer between disk and RAM is implemented using a direct memory access (DMA) controller.
Suppose:

- The transfer of one page of data between memory and disk takes 20 msec.
- Processor clock rate is 400MHz.

Compute the processor overhead during transfer of 1 page between disk and RAM, if:

- The DMA controller set up for the transfer of one page takes 1,500 processor clock cycles, and
- Handling of the interrupt at the completion of the page transfer takes 500 processor clock cycles.

(Express the processor overhead as the ratio between the number of clocks needed to execute all necessary operations related to disk I/O control during one disk I/O, and the number of clocks available in the same time interval.)

ANSWER

c) Consider a system consisting of a synchronous bus and a DRAM memory with the following characteristics:

- The memory supports 4 word block access with an 8/3/3/3 burst rate. The burst rate indicates that there are 8 bus cycles needed to read and put on the bus the first 32 bit word of a block, and that for each of the remaining words only 3 cycles are needed.
- The 32 bit synchronous bus is clocked at 200 MHz.
- To transmit the first word of a block the memory-bus system takes 1 bus clock cycle to send an address to memory, during the next 7 bus cycles the memory performs reading, and then 1 bus clock cycle is needed to transfer the data.
- No address is needed to read and transmit each of the remaining 3 successive memory words of the block.
- Two clock cycles are needed between each bus operation and these two cycles can be overlapped by memory operations.

The operation of the described system is represented on the Figure 8.1.

Find:

I. **[5 marks]** The time needed to complete one **bus transaction** consisting of an address transmission followed by 4 words of data.

ANSWER

II. **[5 marks]** The sustained bandwidth (maximal number of **bytes** that can be transferred in a second).

ANSWER

III. **[5 marks]** The throughput of the described system (maximal number of **bus transactions** in a second).
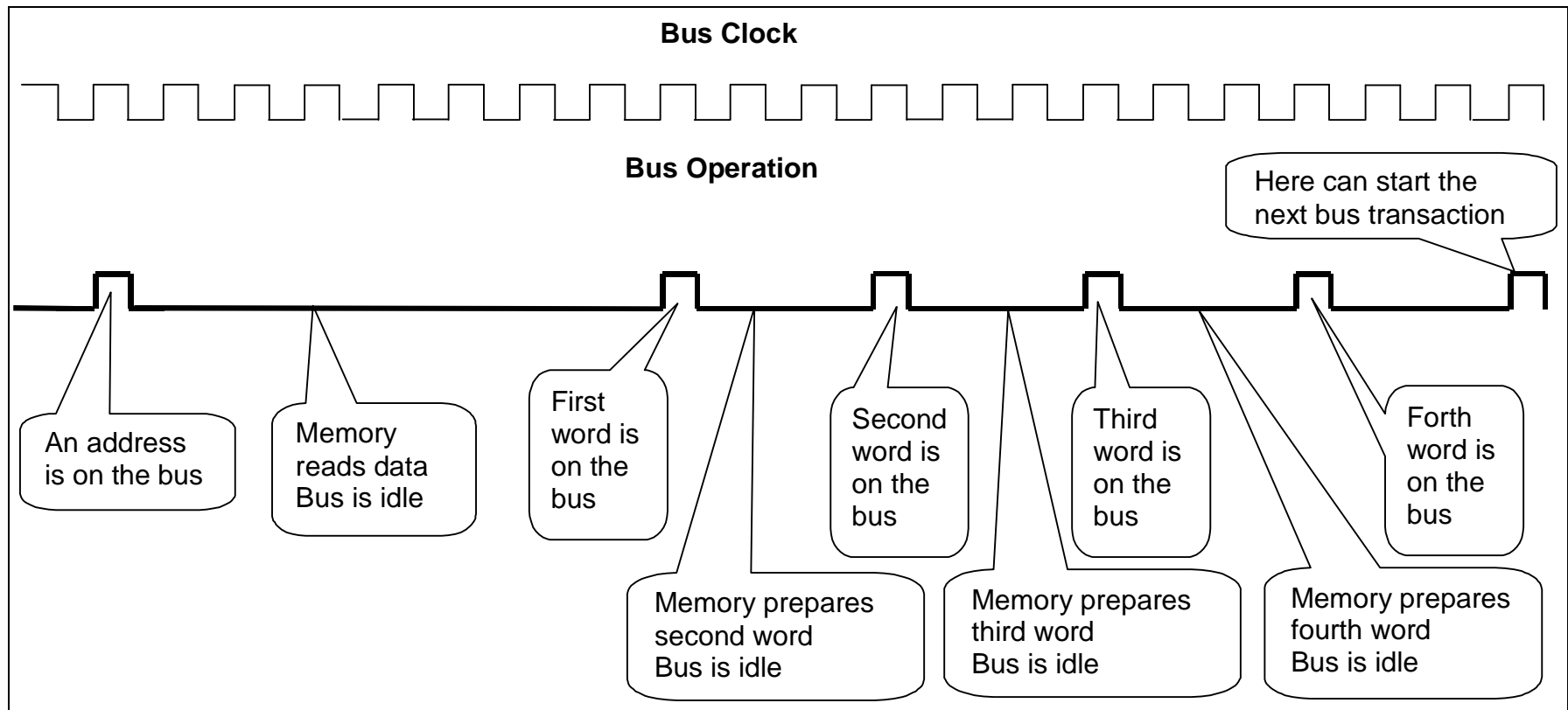
ANSWER

COMP 203   **continued**

Figure 8.1.

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