Digital Electronics - Course Outline

ECEN 202: 2010 Trimester 2

This document sets out the workload and assessment requirements for ECEN202. It also provides contact information for staff involved in the course. If the contents of this document are altered during the course, you will be advised of the change by an announcement in lectures and/or on the course web site. A printed copy of this document is held in the School Office.

Course Lecturer(s)

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The names and contact details of lab tutors for the different sessions will be published at a later stage.

Course Description

The aim of this course is to introduce students, in a practically-oriented way, to a number of topics in analogue electronics, including circuit theorems, transducers, power supplies, semiconductor devices, transistor amplifiers, operational amplifiers and circuits. It builds on the basic circuit theory developed in PHYS 115 and is an integral part of the Electronic and Computer Systems Engineering major. At the end of the course students do a design project which includes designing, laying out and populating a printed circuit board. ECEN 203 is a prerequisite for further courses in analogue electronics.

Prerequisites

ENGR101, MATH 142 or with permission MATH151

Restrictions: PHYS234, ELEN202

Objectives

By the end of the course, students should be able to:

1. Describe the properties, construction and operating characteristics of digital integrated circuits from the most important CMOS and TTL logic families. (BE graduate attribute 3(a))

2. Describe the basic logic operations using Boolean algebra, truth tables and logic circuits and be able to simplify complex logic circuits via Boolean algebra and the K map method. ((BE graduate attribute 3(a))

3. Understand the use of various types of flip-flops in creating sequential circuits and their uses in synchronisation, frequency division and counting. (BE graduate attribute 3(a,b))

4. Design synchronous sequential circuits using the state machine method. ((BE graduate attribute 3(b,c))

5. Understand the design and application of a selection special function IC's, including memory devices. ((BE graduate attribute 3(a, b))

6. Understand the principles and application of programmable logic devices, particularly with reference to generic array logic devices. ((BE graduate attribute 3(b,c))

7. Be able to generate clear documentation such as circuit diagrams and reports in order to document your design. ((BE graduate attribute 2(b)).

Course Timetable

Lectures: Tuesday and Thursday from 10 - 10.50 am in AM102.

Labs: One 3-hour lab/week on Wednesday 9 am to 12 pm or Wednesday 2 to 5 pm or Thursday 2-5 pm. Labs will be held in LB217. Allocation of the lab sessions will take place in the first lecture (Tuesday 13 July).

Course materials and texts

A study guide containing the core class notes and laboratory instructions will be available from SCPS reception (ground floor, Laby building). In addition students may be required to take down additional notes in class. No textbook is required, but the book "Digital Systems", by R J Tocci will be valuable as additional reading material. This text is available in the VUW bookshop at a cost of ~ $ 120. The library should also have some copies on closed reserve and on 3 - day loan. Any edition from the 7th or later is suitable.

Assessment

The assessment for ECEN202 involves assignments, two in-term tests, weekly laboratories, and design exercises as detailed below:

Assessed Item	Length/ duration	Date due / exam period	% of final grade	Objectives assessed
Laboratory Work	Weekly report	Weeks 2 - 12	20%	1 - 3, 5, 6
Assignments	tbd	Weeks 2 - 12	10%	1 - 5
Design Report	tbd	Weeks 9 - 11	20%	4
Tests 1	1 hour	Week 6	25%	1 - 3
Test 2	1 hour	Week 12	25%	4 - 6

Laboratory Work

The course has 9 one-session experiments and 1 two-session design exercise associated with it. All experimental work must be started in the scheduled periods (see schedule to be posted in week). If you do not complete the work in this session, arrangements can be made to complete at a later stage (before the next session). However, no laboratory demonstrators will be available out of sessions.

It is strongly advised that you keep detailed experimental notes for all experiments in a logbook. In addition, data acquired/graphs plotted should be electronically stored and kept to the end of the course.

At the end of each laboratory you will be required to submit a short laboratory report. This report will be based on a number of questions asked at the end of each laboratory script. This report must be handed in no later than one week after the experiment had been scheduled.

Your final mark for each laboratory will consist of a mark for your report as well as a mark assigned by the lecturer/lab demonstrator for your contribution in the laboratory.

Assignments

Assignments will be set approximately once every two weeks and should be handed in before the required deadline.

Design Exercise and Report

Full details of the design and reporting requirements will be handed out during the course. Please note the deadline for design demonstration, which is one week after your last design laboratory session, as well as the deadline for the design report.

Handing in of work

Drop boxes on the second floor of the Laby building, opposite to the laboratory, will be marked for your laboratory reports or assignments.

Mandatory Course Requirements and passing ECEN202

Mandatory course requirements are as follows:

- Satisfactory completion of the design exercise.
- Satisfactory completion of at least 7 of the 9 laboratory experiments.
- A minimum of 40% averaged over the two in-term tests.

To pass ECEN202 a student must satisfy mandatory requirements and gain at least a **C** grade overall.

Late Work

All work is due in on the due date. Marks will be deducted at a rate of 10% of the full mark for each working day late. Work will not be marked if more than 1 week late. Extensions must be requested in writing (email) and will only be given

in exceptional circumstances, and if agreed before the due date.

In the event of an aegrotat application, regular submission and performance in assignments and laboratories will contribute substantially to the outcome.

Workload

On average, students should plan to spend a minimum of 10 hours per point i.e. 150 hours for a 15 point course, or 10-12 hours per week, including exam periods, in order to achieve an average grade in this course.

Blackboard

This course uses Blackboard. Course materials and other information will be posted on Blackboard. Students should check Blackboard regularly.

School of Engineering and Computer Science

The School office is located on level three of the Cotton Building (Cotton 358).

Announcements and Communication

The main means of communication outside of lectures will be the ECEN202 Blackboard site as well as email. PLease check that your email address is correct in the VUW system.

Plagiarism

Working Together and Plagiarism

We encourage you to discuss the principles of the course and assignments with other students, to help and seek help with programming details, problems involving the lab machines. However, any work you hand in must be your own work.

The School policy on Plagiarism (claiming other people's work as your own) is available from the course home page. Please read it. We will penalise anyone we find plagiarising, whether from students currently doing the course, or from other sources. Students who knowingly allow other students to copy their work may also be penalised. If you have had help from someone else (other than a tutor), it is always safe to state the help that you got. For example, if you had help from someone else in writing a component of your code, it is not plagiarism as long as you state (eg, as a comment in the code) who helped you in writing the method.

Withdrawal

The last date for withdrawal from ECEN201 with entitlement to a refund of tuition fees is Friday, 23 July 2010 (the end of week 2 of trimester). The last date for withdrawal without being regarded as having failed the course is Friday, 24 September 2010 (the end of week 9) -- though later withdrawals may be approved by the Dean in special circumstances.

Rules & Policies

Find key dates, explanations of grades and other useful information at http://www.victoria.ac.nz/home/study.

Find out about academic progress and restricted enrolment at http://www.victoria.ac.nz/home/study/academic-progress.

The University's statutes and policies are available at http://www.victoria.ac.nz/home/about/policy, except qualification statutes, which are available via the Calendar webpage at http://www.victoria.ac.nz/home/study/calendar (See Section C).

Further information about the University's academic processes can be found on the website of the Assistant Vice-Chancellor (Academic) at http://www.victoria.ac.nz/home/about/avcacademic

All students are expected to be familiar with the following regulations and policies, which are available from the school web site:

Grievances
Student and Staff Conduct
Meeting the Needs of Students with Disabilities
Student Support
Academic Integrity and Plagiarism
Dates and Deadlines including Withdrawal dates
School Laboratory Hours and Rules
Printing Allocations
Expectations of Students in ECS courses

The School of Engineering and Computer Science strives to anticipate all problems associated with its courses, laboratories and equipment. We hope you will find that your courses meet your expectations of a quality learning experience.

If you think we have overlooked something or would like to make a suggestion feel free to talk to your course organiser or lecturer.