Power Electronics - Course Outline

ECEN 405: 2016 Trimester 1

ECEN 405 covers theory, design and application of power electronic circuits and the transformation and control of electrical energy. Topics include switching devices and their properties, power quality indices, Designing switching poles, Switch mode converter design, Magnetics design, Power factor correction, Feedback control of converters, Rectification and Inversion.

This document sets out the workload and assessment requirements for ECEN 405. It also provides contact information for staff involved in the course. If the contents of this document are altered during the course, you will be advised of the change by an announcement in lectures and/or on the course web site. A printed copy of this document is held in the School Office.

Objectives

By the end of the course, students should be able to:

1. Explain the terminology inherent in Power Electronics and be able to calculate figures of merit such as Total Harmonic Distortion (THD) (both voltage and current), Form Factor, Crest Factor, ripple, etc.(BE graduate attribute 3(a))
2. Interpret and be able to implement and analyse different rectification, switch-mode and inversion techniques (BE graduate attribute 3(a, b)).
3. Design decision on different power electronic converters for a wide variety of electronic applications. (BE graduate attribute 3(a, b))
4. Design, construct, and demonstrate the operation of a power electronic system. (BE graduate attribute 1(b), 2(a), 3(b, d, e, f))
5. Practically inspect power converter topologies in an industrial environment and recognise the safety issues of working in an industrial environment. (BE graduate attribute 1(b), 2(b), 3(b,d,e))

Prerequisites

The prerequisites for ECEN 405 are:

- ECEN 303 or PHYS 340

Course Materials and Textbook

For all lectures students will be provided with a comprehensive study guide which contains the entire lecture slides and additional lecture material. A complete PDF of these slides is available via the ECS Wiki for students. An effort will also be made to provide lecture notes during the lectures.

The recommended textbook for ECEN 405 is: *Mohan,* “Power Electronics – A first Course”, 3rd (2012) edition, Wiley.

Outline of Course Content

1. Power Electronics Indices
2. Design of Switching Power Ploes
3. Power Inversion
4. DC-DC Conversion/SMPS
5. Rectification
6. Feedback Control
7. Power Factor Control

Lectures, Tutorials, Laboratories, and Practical work

- **Lectures:** Tuesday, Wednesday (AMLT105) and Friday (AM104) from 900 – 950 hrs.
- **Labs**: One 3-hour lab/week will be held in Co250 on Monday 9-12 hrs. The allocated lab times should also be used towards the design assignment.

Assignments and Projects

The assessment for ECEN405 involves assignments, two in-term tests, weekly laboratories, and a design report as detailed below:

Assessed Item	Length/ duration	Date due / exam period	% of final grade	Objectives assessed
Laboratory Work	Weekly report	Weeks 2 - 12	15%	1 - 3
Assignments	Weekly	Weeks 2 - 10	30%	1 - 3
Design Project	12 Weeks	June 13	30%	4 - 5
Test	1 hour	April 15	10%	1 - 3
Field Trip Report		May 23	5%	1 - 5
Test	1 Hour	May 27	10%	1 - 3

Workload

On average, students should plan to spend a minimum of 10 hours per point i.e. 150 hours for a 15 point course, or *10-12* hours per week, including exam periods, in order to achieve an average grade in this course.

School of Engineering and Computer Science

The School office is located on level three of the Cotton Building (Cotton 358).

Staff

The course organiser for ECEN 405 is Ramesh Rayudu. His contact details are:

- AM421
- +64 4 463 5733 Ext 8068
- Ramesh.Rayudu@ecs.vuw.ac.nz

The Lab Demonstrator is Daniel Burmester and will be available during lab timings on Lab days for two hours .

Some lectures on HVDC will be delivered by Transpower HVDC Manager, Mr. Michael Dalzell.

The Class Rep for this course is Andrew Ang.

Announcements and Communication

This course uses ECSWiki. Course materials and other information will be posted on ECSWiki. Students should check ECSWiki regularly.

Assessment

Your grade for ECEN 405 will be determined based on the below assessment weightings:

Assessed Item	Weight
Laboratory Work	15%
Assignments	30%
Design Report	30%
Field Trip report	5%
Test 1	10%
Test 2	10%

Tests and Exams

There is NO final exam for this course and there will be two term tests in week 6 and 11.

Practical Work

There will be a field trip to HAYWARDS substation as part of this course. The date of the trip will be notified in the class. Remember you need to write a report on your trip and submit. Your report is worth 5%.

Laboratory Work

The course has FIVE experiments and a design assignment for 6 weeks associated with it. All experimental work must be started in the scheduled lab time. If you do not complete the work in this session, arrangements can be made to complete at a later stage (before the next session). However, no laboratory demonstrators will be available out of sessions.

It is required that you keep detailed experimental notes for all experiments in a logbook. In addition, data acquired/graphs plotted should be electronically stored and kept to the end of the course. A log book will be provided to keep a log of your research activities for your design assignment. The log book will be marked and will contribute towards your project mark.

At the end of each laboratory you will be required to submit the provided laboratory report. The report marking will be based on a number of questions asked in the laboratory script. This report must be handed in no later than one week after the experiment had been scheduled.

Assignments

Assignments will be given weekly every Tuesday from Weeks 2 to Week 10 and should be handed in at or before the following Wednesday lecture.

Design Exercise and Report

Full details of the design and reporting requirements will be handed out during the course. In general, the assessment schedule for the project is as follows:

1. **The quality of the report (7.5%)**
2. **The performance of the amplifier (efficiency, bandwidth, distortion) (5%)**
3. **The design process (10%)**
4. **PCB layout and construction (5%)**
5. **Presentation (2.5%)**

Policies and penalties for late submission

Late assessment will be penalised at the rate of 10% for every working day the assessment is late. The lecturer may refuse to mark work that has been handed in over a week late, and may also refuse if the assessment has been marked and returned to the class. In such instances, a zero grade for that assessment shall result.

In the event of an aegrotat application, regular submission and performance in assignments and laboratories will contribute substantially to the outcome.

Plagiarism

Working Together and Plagiarism

We encourage you to discuss the principles of the course and assignments with other students, to help and seek help with programming details, problems involving the lab machines. However, any work you hand in must be your own work.

The School policy on Plagiarism (claiming other people's work as your own) is available from the course home page. Please read it. We will penalise anyone we find plagiarising, whether from students currently doing the course, or from other sources. Students who knowingly allow other students to copy their work may also be penalised. If you have had help from someone else (other than a tutor), it is always safe to state the help that you got. For example, if you had help from someone else in writing a component of your code, it is not plagiarism as long as you state (eg, as a comment in the code) who helped you in writing the method.

Mandatory Requirements

It is expected that ALL work will be completed and handed in for marking. An incomplete or fail grade (K) will be issued to any student who does not satisfy ANY of the below requirements

1. Satisfactorily completes all assigned labs (a demonstrator must verify all lab work).
2. Reasonable attempt to complete the design aspect of the project and submit a design report.
3. Scores more than 40% (average) in the internal tests

Passing ECEN 405

To pass ECEN 405, a student must satisfy mandatory requirements and gain at least a **C-** grade overall.

Withdrawal

The last date for withdrawal from ECEN 405 with entitlement to a refund of tuition fees is Friday 11 March 2016. The last date for withdrawal without being regarded as having failed the course is Friday 13 May 2016 -- though later withdrawals may be approved by the Dean in special circumstances.

Rules & Policies

Find key dates, explanations of grades and other useful information at http://www.victoria.ac.nz/home/study.

Find out about academic progress and restricted enrolment at http://www.victoria.ac.nz/home/study/academic-progress.

The University's statutes and policies are available at http://www.victoria.ac.nz/home/about/policy, except qualification statutes, which are available via the Calendar webpage at http://www.victoria.ac.nz/home/study/calendar (See Section C).

Further information about the University's academic processes can be found on the website of the Assistant Vice-Chancellor (Academic) at http://www.victoria.ac.nz/home/about/avcacademic

All students are expected to be familiar with the following regulations and policies, which are available from the school web site:

Grievances
Student and Staff Conduct
Meeting the Needs of Students with Disabilities
Student Support
Academic Integrity and Plagiarism
Dates and Deadlines including Withdrawal dates
School Laboratory Hours and Rules
Printing Allocations
Expectations of Students in ECS courses

The School of Engineering and Computer Science strives to anticipate all problems associated with its courses, laboratories and equipment. We hope you will find that your courses meet your expectations of a quality learning experience.

If you think we have overlooked something or would like to make a suggestion feel free to talk to your course organiser or lecturer.

Course Outline as PDF