ENGR 101
Engineering Technology

Dr. Kerese Manueli

School of Engineering and Computer Science
Victoria University of Wellington

Victoria
UNIVERSITY OF WELLINGTON
Te Whare Wānanga
o te Ūpoko o te Ika a Māui
CAPITAL CITY UNIVERSITY

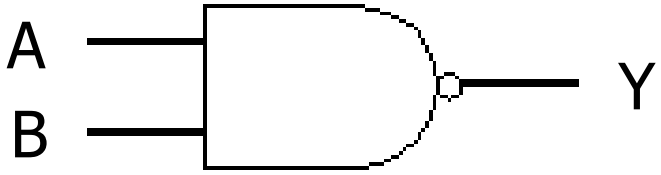
Week 5 Lecture 9a

- NAND, NOR, XOR, XNOR gates and truth tables

- Course web page:
  https://ecs.wgtn.ac.nz/Courses/XMUT101_2021T1/

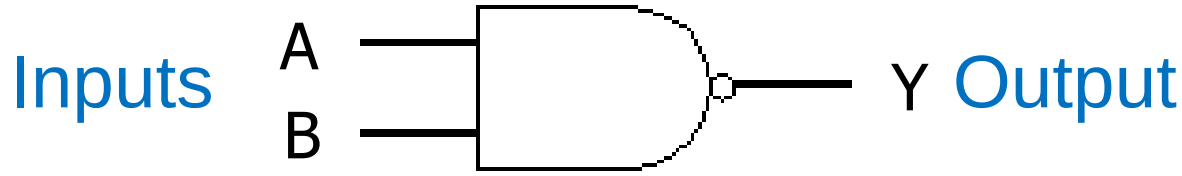
- kerese@ecs.vuw.ac.nz

NAND Gate



- The NAND gate is a combination of an AND gate followed by an INVERTER.

NAND Gate

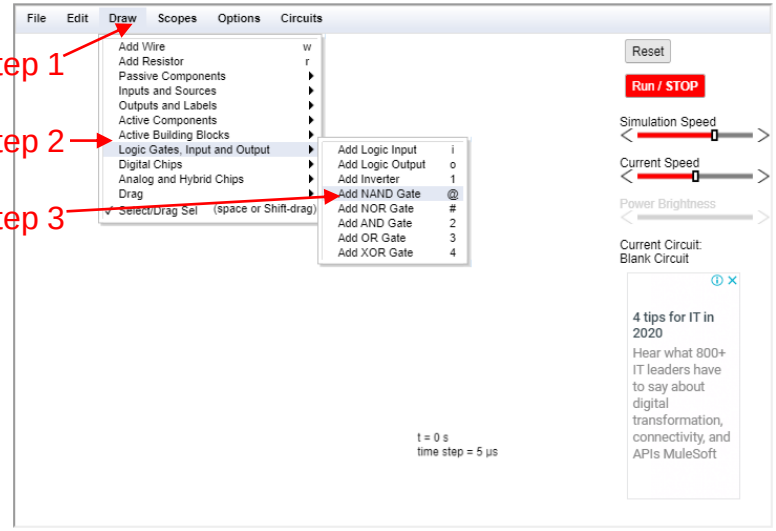


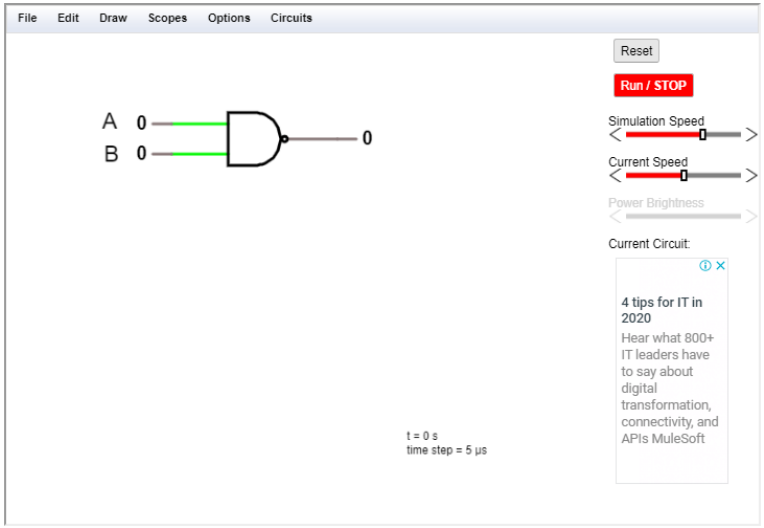
- The NAND gate is a combination of an AND gate followed by an INVERTER.
- Truth Table shows this…

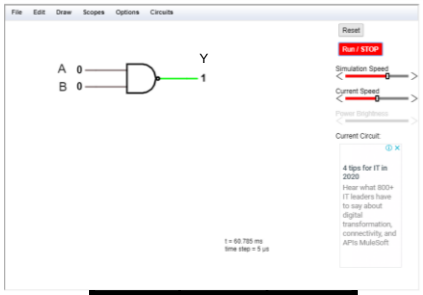
Inputs

A	B	Y (Output)
0	0	1
0	1	1
1	0	1
1	1	0

NAND Gate



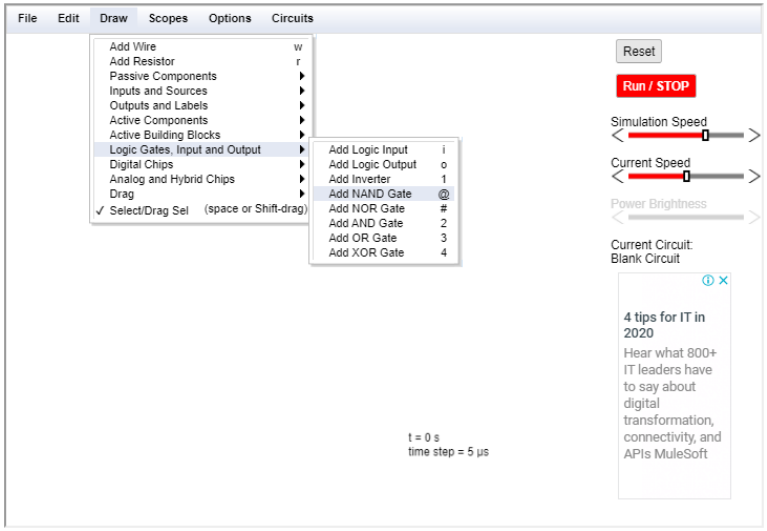


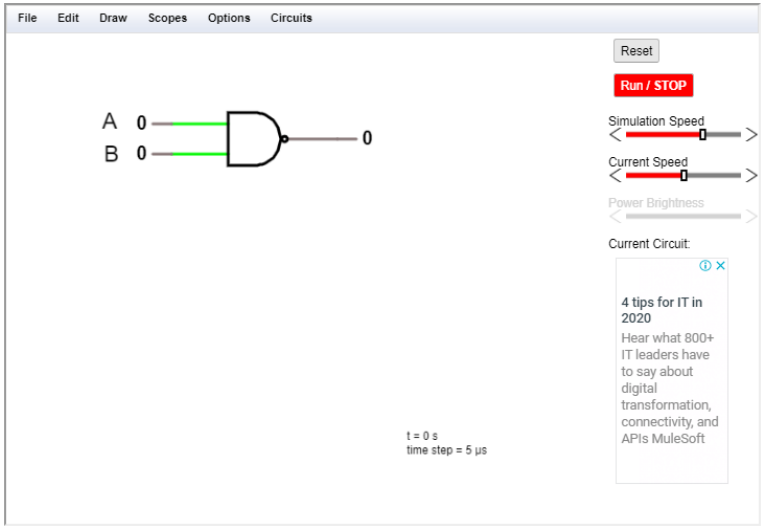


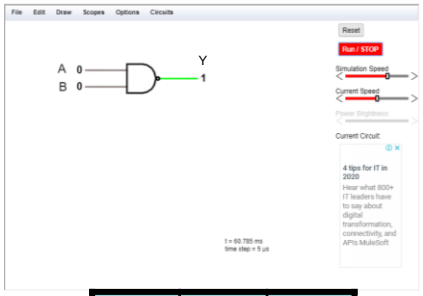
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

2nd row

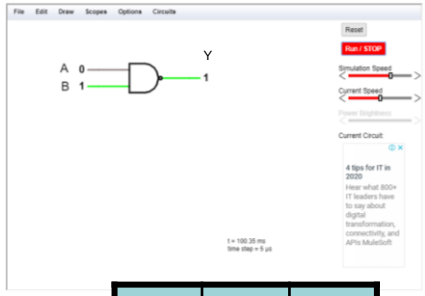
NAND Gate







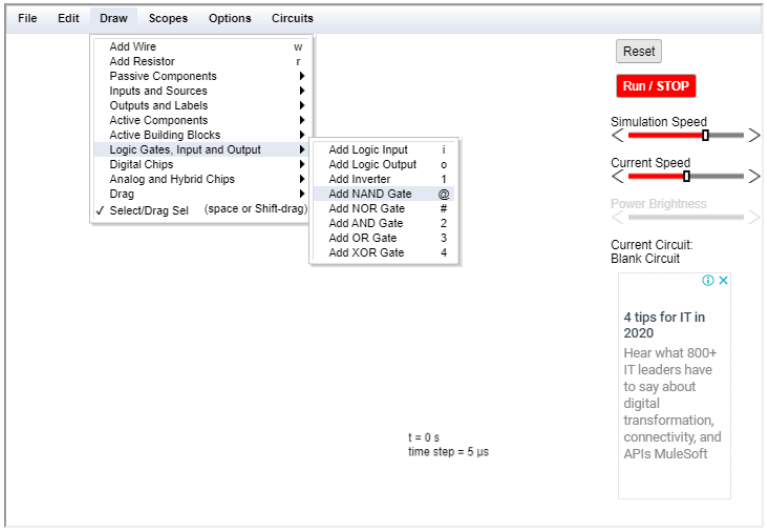
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

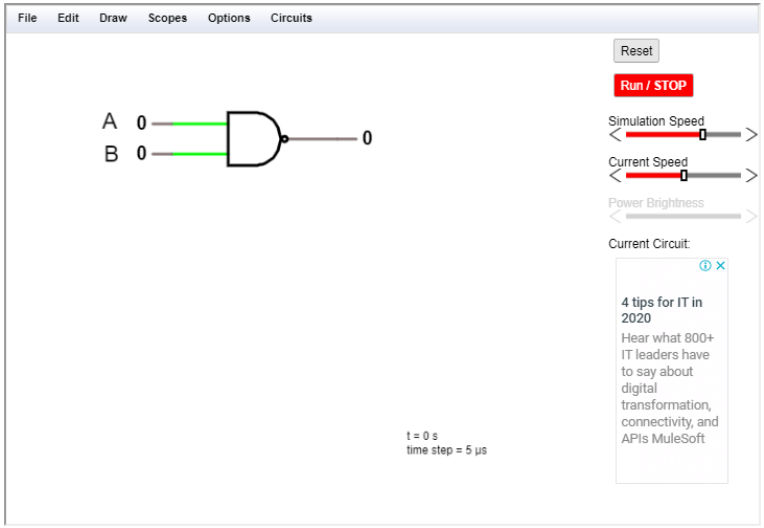


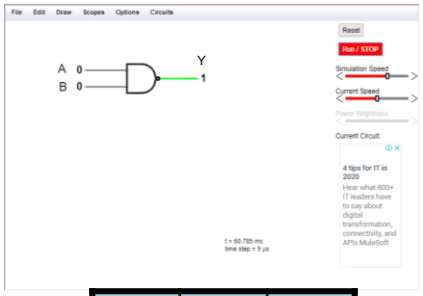
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

3rd row

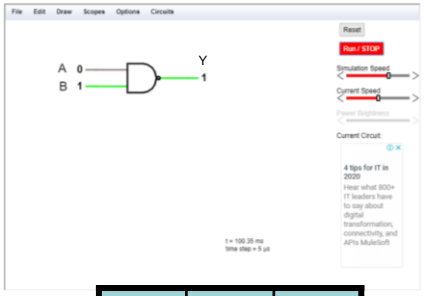
NAND Gate



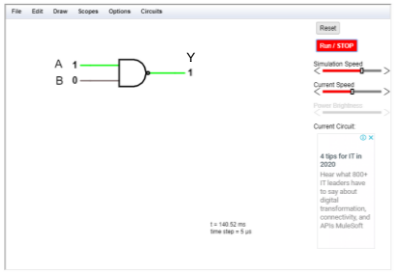




A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0



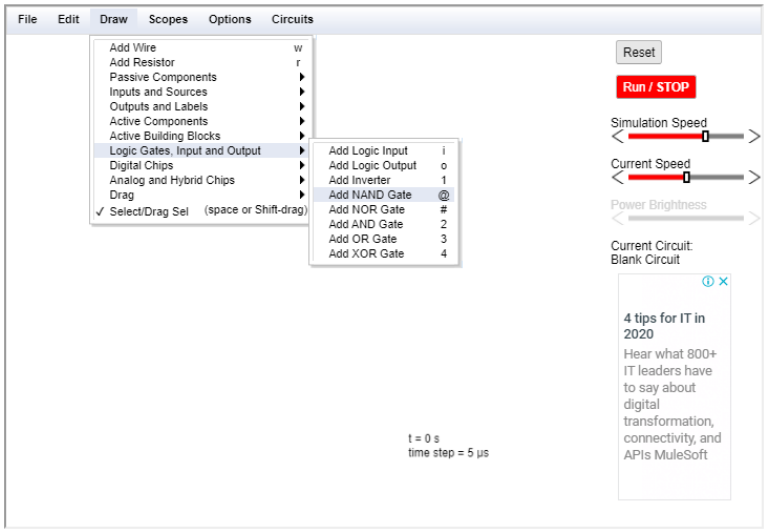
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

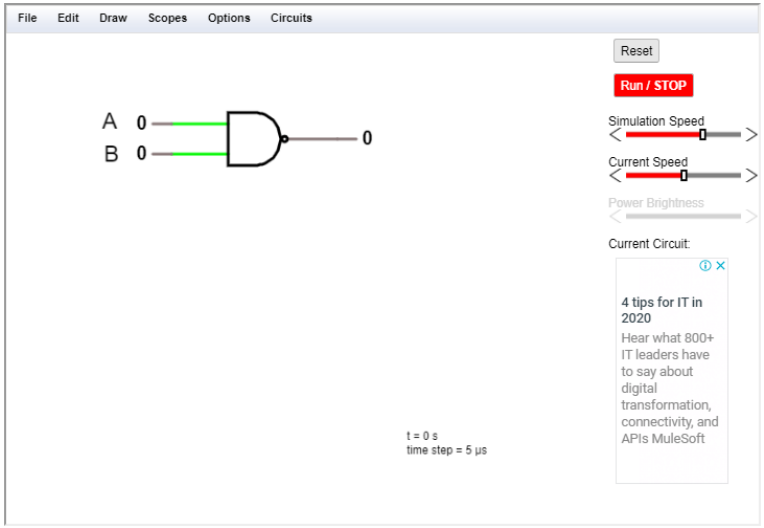


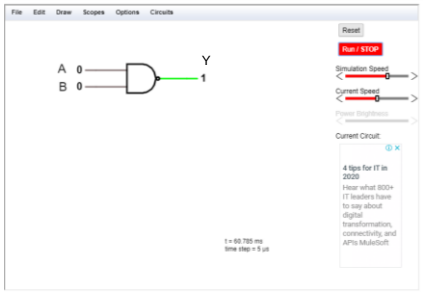
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

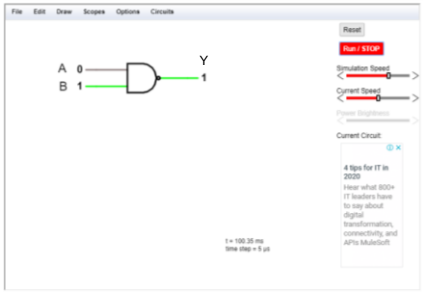
4th row

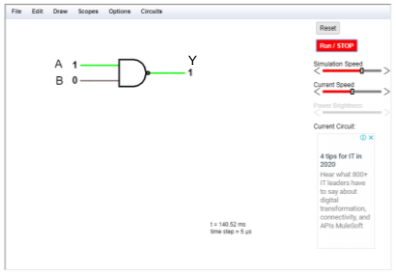
NAND Gate

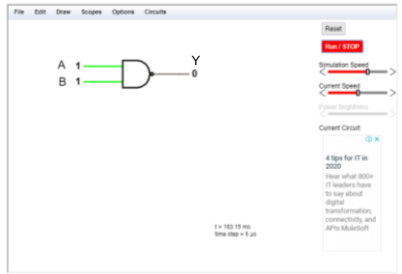












A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

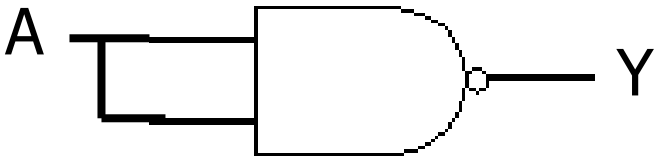
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

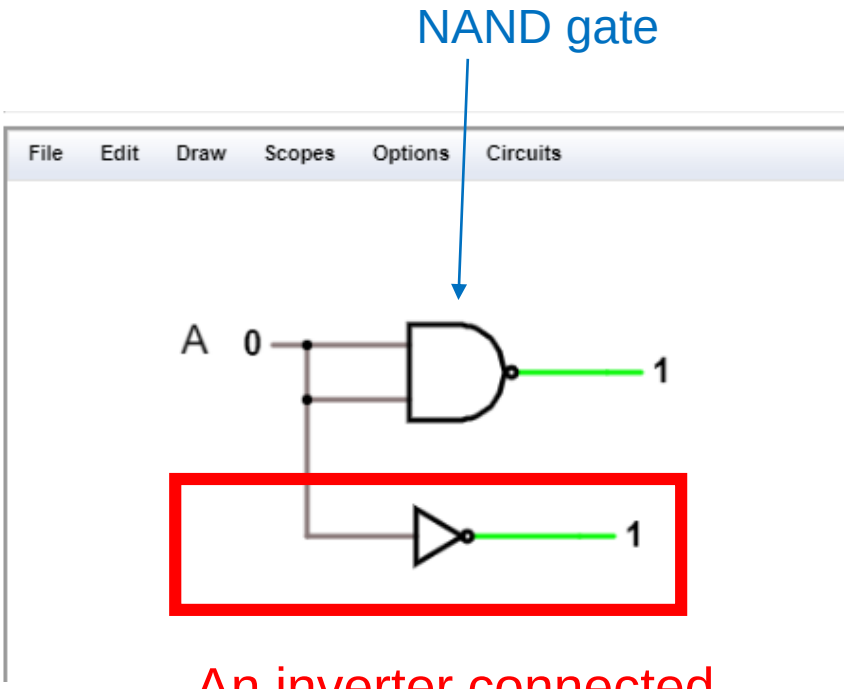
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

5th row

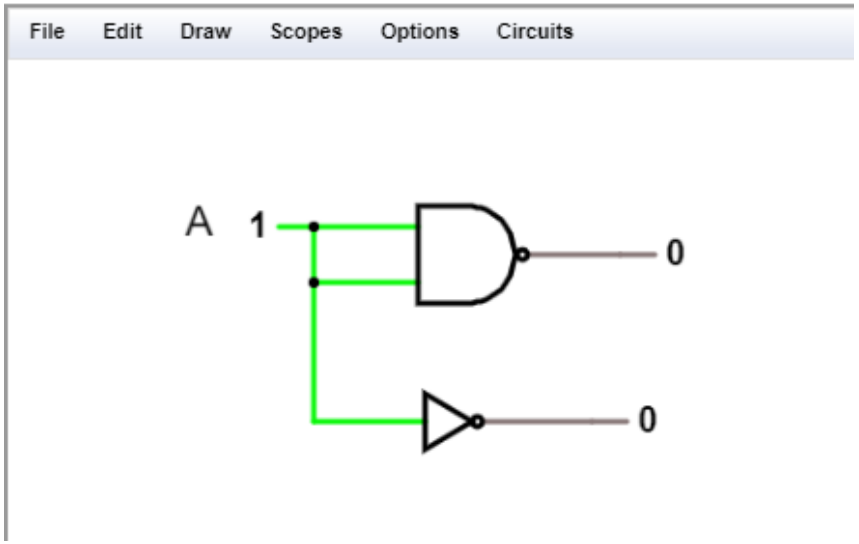
NAND gate used as another gate



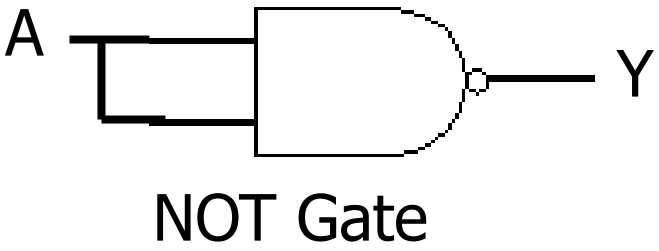
NAND gate with same input → NOT Gate



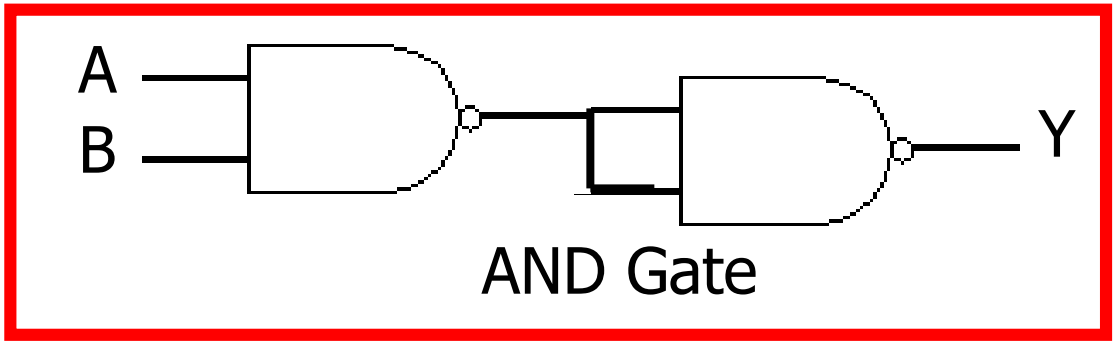
An inverter connected to the same input A



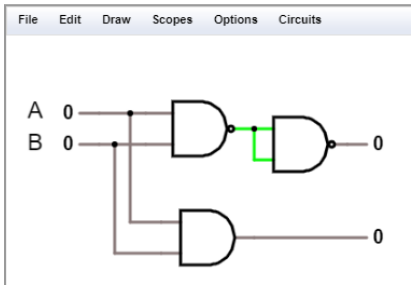
NAND gates used as other gate

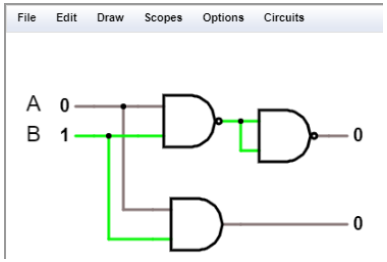


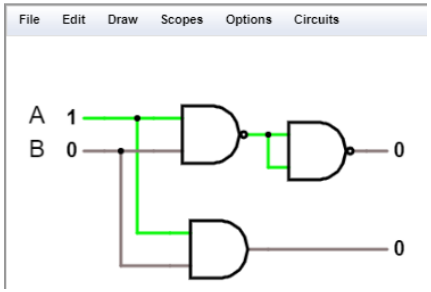
NOT Gate

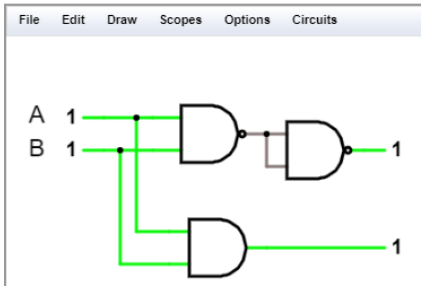


AND Gate

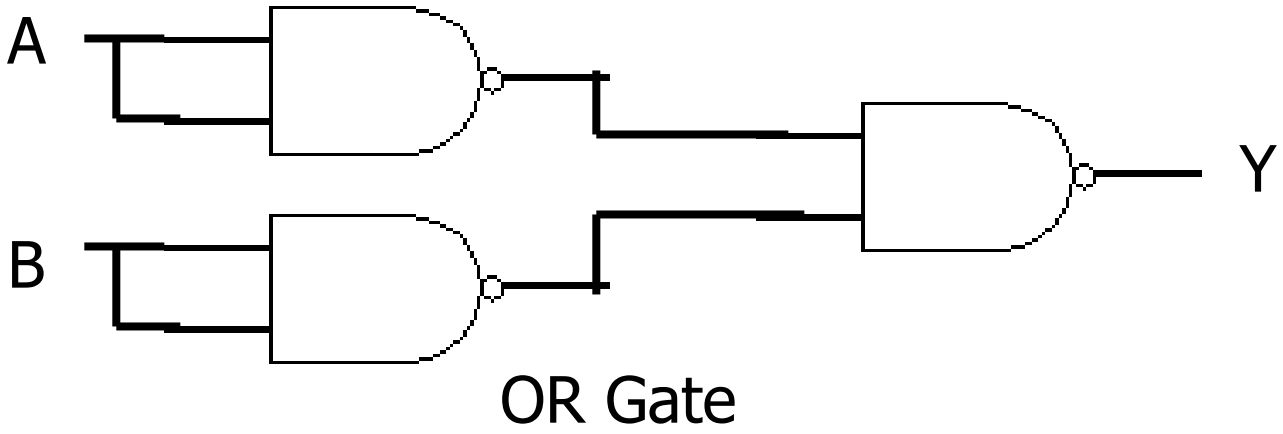


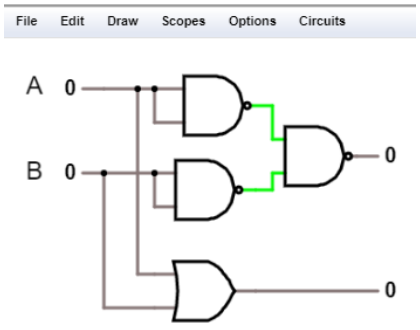


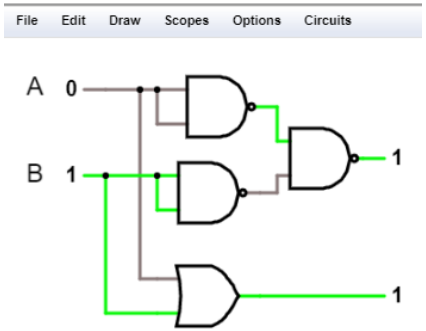


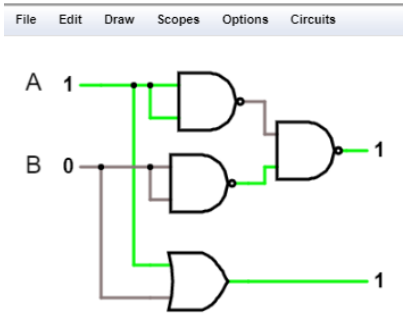


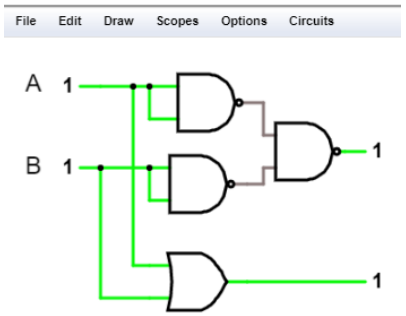
NAND gates into other gates



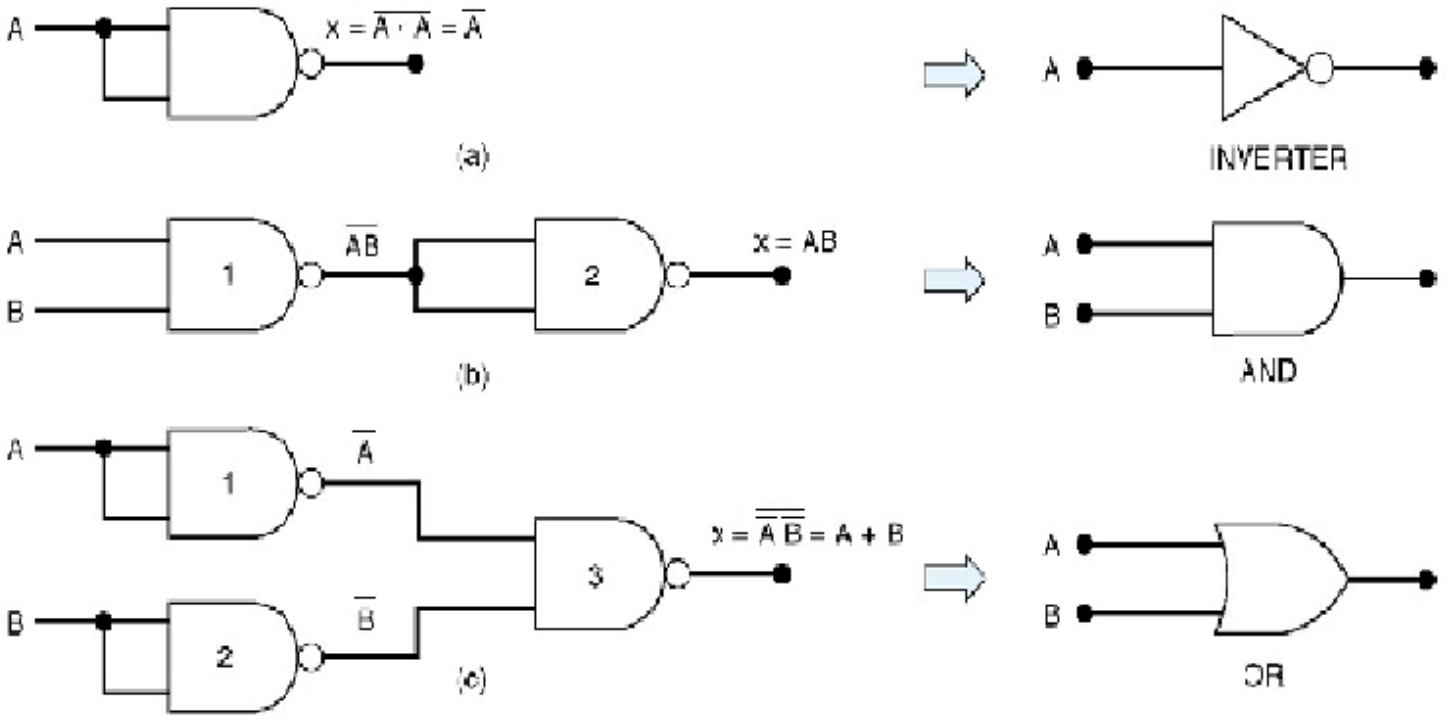




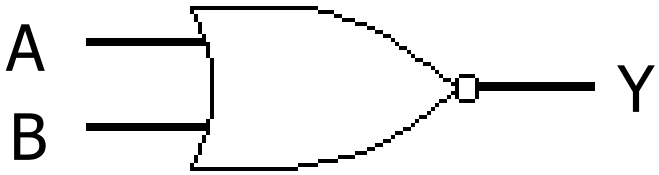




Universality of NAND gates



NOR Gate



- A NOR gate is a combination of an OR gate followed by an inverter. It's truth table shows this…

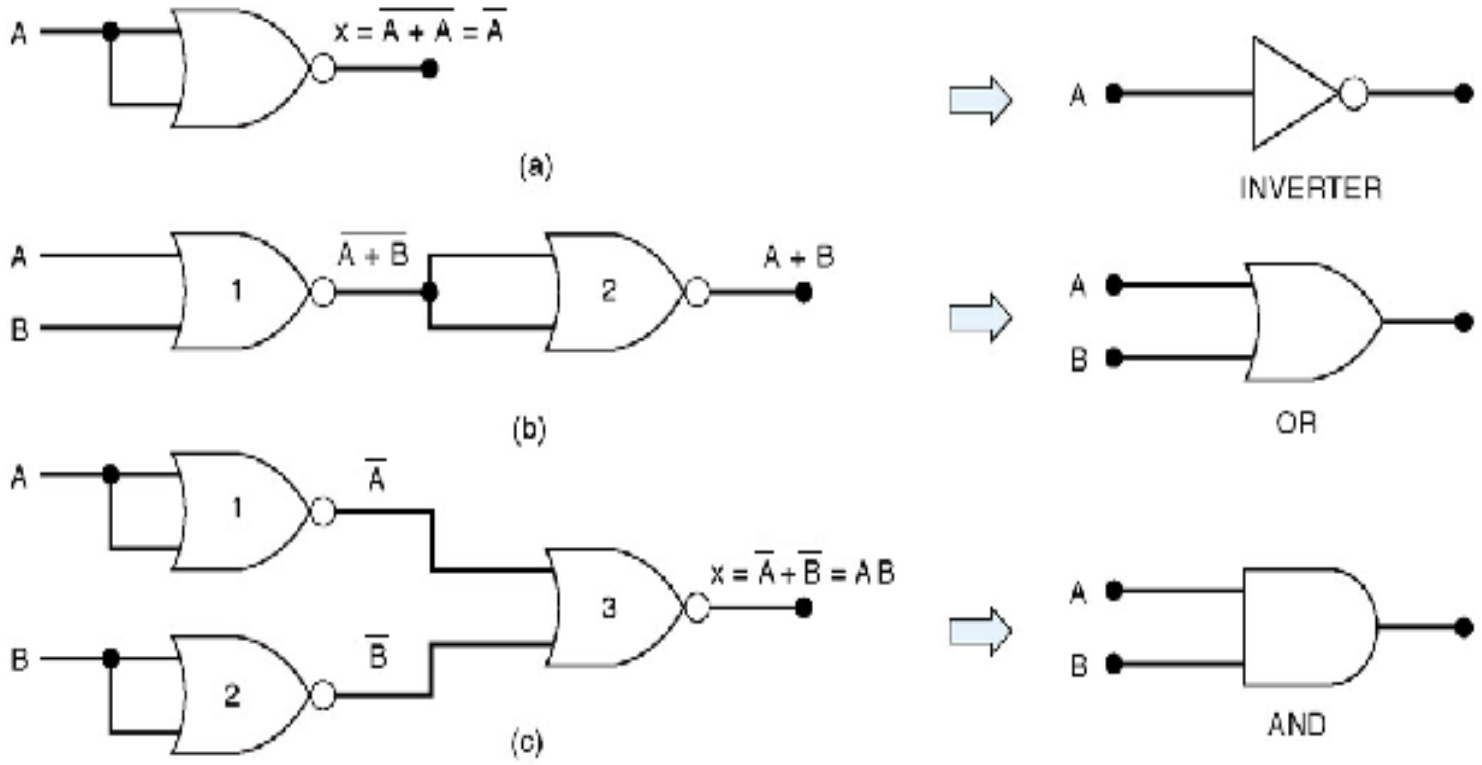
A	B	Y
0	**0**	**1**
0	**1**	**0**
1	**0**	**0**
1	**1**	**0**

Functionally Complete Gates

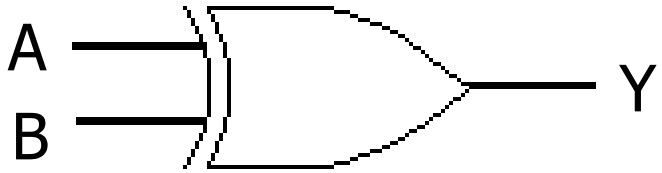
- Just like the NAND gate, the NOR gate is functionally complete (ie any logic function can be implemented using just NOR gates).
- Both NAND and NOR gates are very valuable as any design can be realized using either one.
- It is easier to build an IC chip using all NAND or NOR gates than to combine AND,OR, and NOT gates.
- NAND/NOR gates are typically faster at switching and cheaper to produce.

Universality of NOR gate

Equivalent representations of the AND, OR, and NOT gates



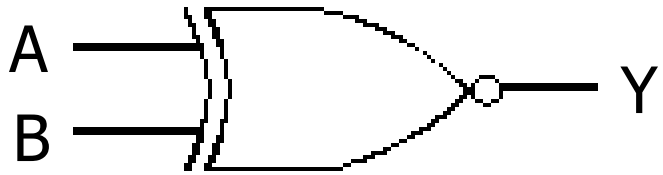
XOR Gate (Exclusive-OR)



- The symbol for the XOR gate is shown above.
- XOR gates assert their output when exactly one of the inputs is asserted, hence the name.
- The switching algebra symbol for this operation is $\oplus$, i.e. $1 \oplus 1 = 0$ and $1 \oplus 0 = 1$.

A	B	Y
0	**0**	**0**
0	**1**	**1**
1	**0**	**1**
1	**1**	**0**

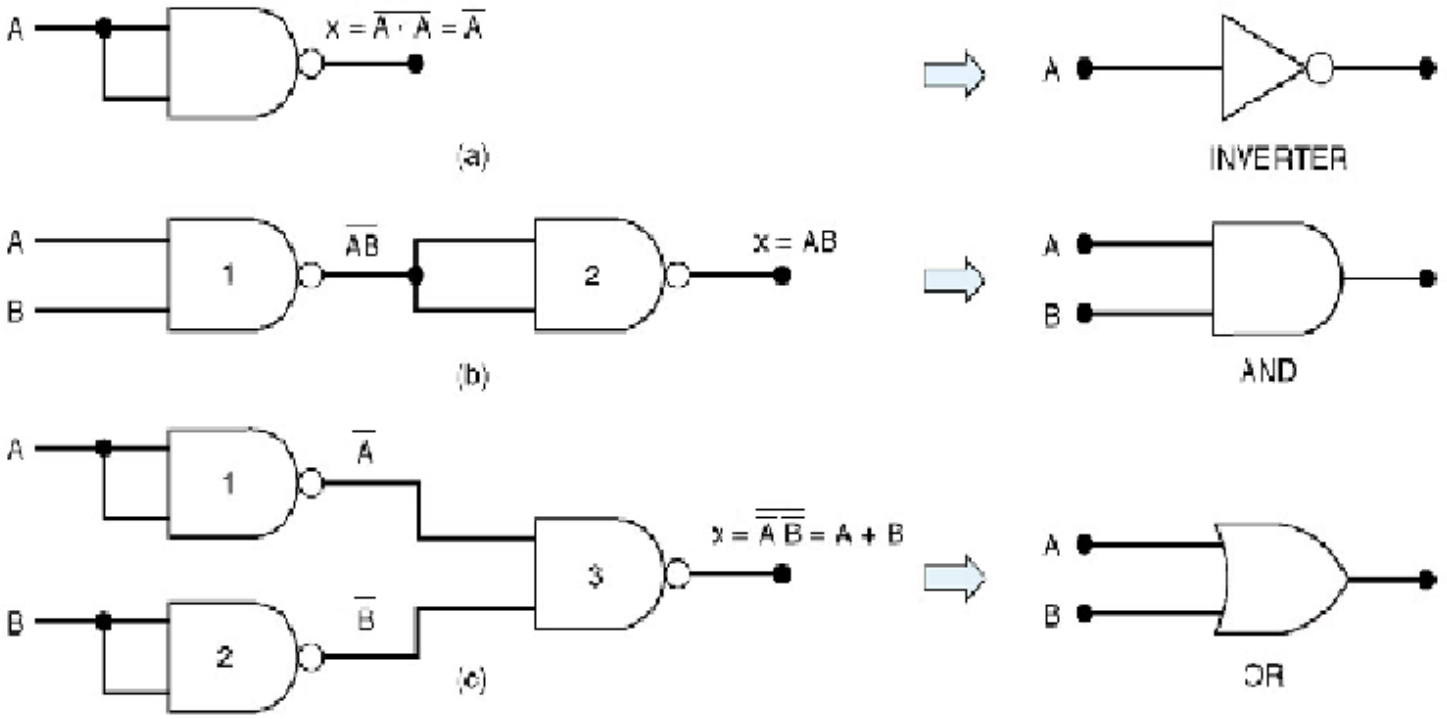
XNOR Gate



- This is a XNOR gate.
- This functions as an exclusive-NOR gate, or simply the complement of the XOR gate.
- The switching algebra symbol for this operation is ⊙, i.e. $1 \odot 1 = 1$ and $1 \odot 0 = 0$.

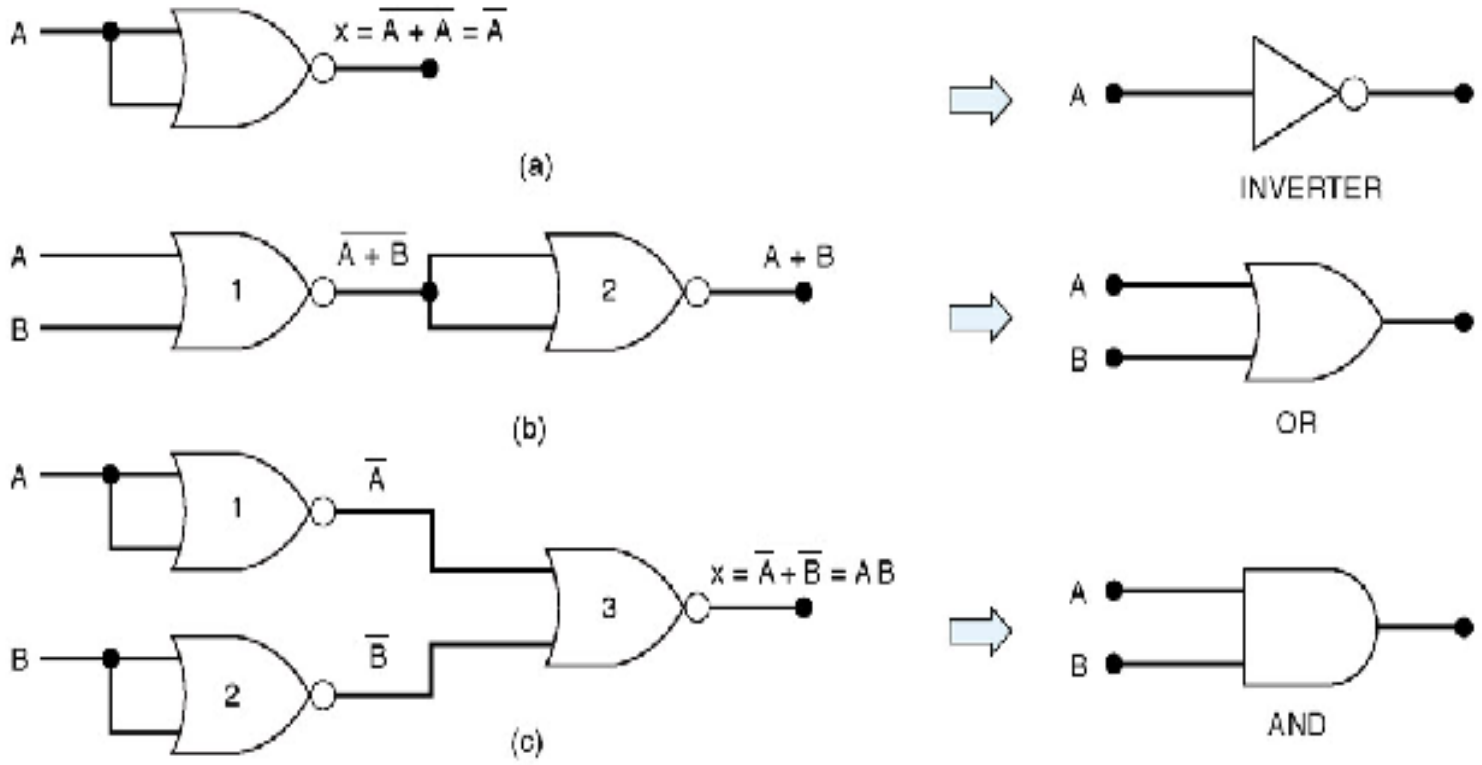
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

Universality of NAND gates



Universality of NOR gate

Equivalent representations of the AND, OR, and NOT gates



Week 5 Lecture 9a

- NAND, NOR, XOR and XNOR gates

- Course web page:

  https://ecs.wgtn.ac.nz/Courses/XMUT101_2021T1/

- kerese@ecs.vuw.ac.nz