

ENGR 101

Engineering Technology

Dr. [Kerese Manueli](#)

School of Engineering and Computer Science
Victoria University of Wellington

Victoria
UNIVERSITY OF WELLINGTON

*Te Whare Wānanga
o te Ūpoko o te Ika a Māui*



CAPITAL CITY UNIVERSITY

Week 5 Lecture 9a

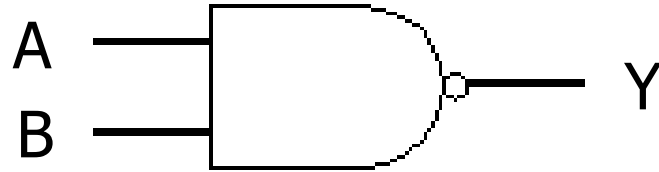
- NAND, NOR, XOR, XNOR gates and truth tables

- Course web page:

https://ecs.wgtn.ac.nz/Courses/XMUT101_2021T1/

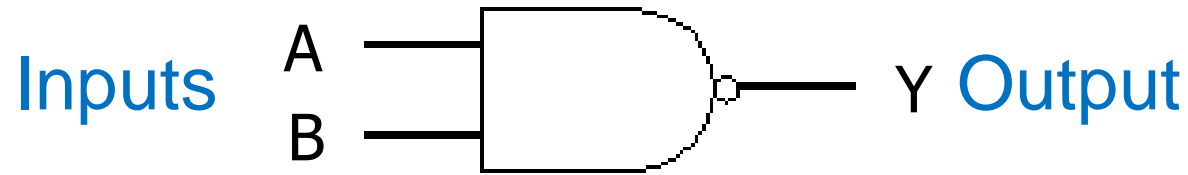
- kerese@ecs.vuw.ac.nz

NAND Gate



- The **NAND** gate is a combination of an AND gate followed by an INVERTER.

NAND Gate



- The **NAND** gate is a combination of an AND gate followed by an INVERTER.
- **Truth Table** shows this...

Inputs

A	B	Y (Output)
0	0	1
0	1	1
1	0	1
1	1	0

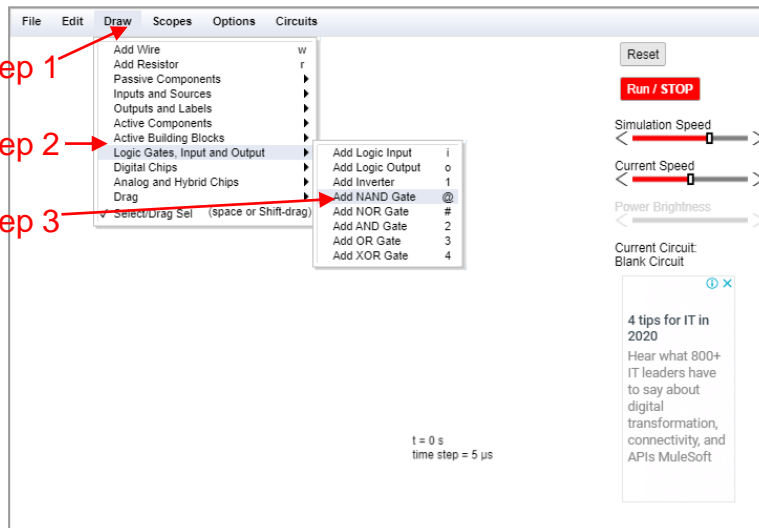
The truth table is a 4x3 grid. The first two columns are labeled 'A' and 'B' under the heading 'Inputs'. The third column is labeled 'Y (Output)'. The rows represent the four possible combinations of binary inputs: (0,0), (0,1), (1,0), and (1,1). The output values are 1 for the first three rows and 0 for the last row.

NAND Gate

Step 1 →

Step 2 →

Step 3 →



File Edit Draw Scopes Options Circuits

- Add Wire w
- Add Resistor r
- Passive Components
- Inputs and Sources
- Outputs and Labels
- Active Components
- Active Building Blocks
- Logic Gates, Input and Output
 - Digital Chips
 - Analog and Hybrid Chips
 - Drag
 - Select/Draw Sel (space or Shift-drag)
 - Add Logic Input i
 - Add Logic Output o
 - Add Inverter 1
 - Add NAND Gate @
 - Add NOR Gate #
 - Add AND Gate 2
 - Add OR Gate 3
 - Add XOR Gate 4

Reset

Run / STOP

Simulation Speed

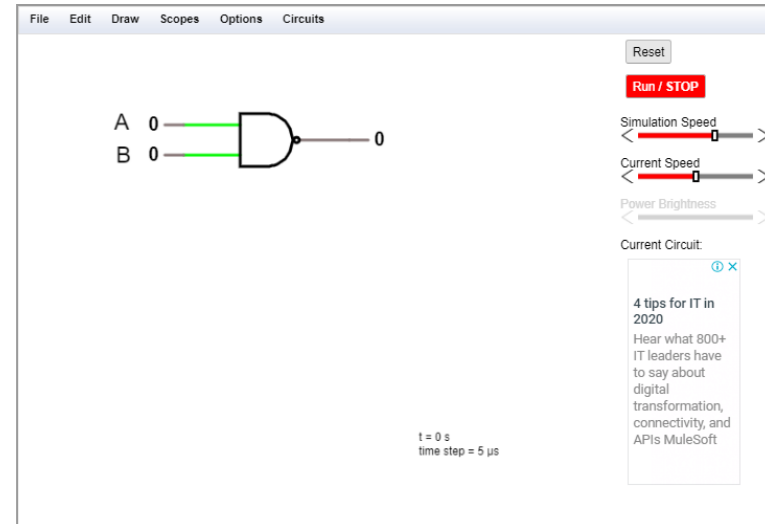
Current Speed

Power Brightness

Current Circuit:
Blank Circuit

4 tips for IT in 2020
Hear what 800+ IT leaders have to say about digital transformation, connectivity, and APIs MuleSoft

t = 0 s
time step = 5 μs



File Edit Draw Scopes Options Circuits

Reset

Run / STOP

Simulation Speed

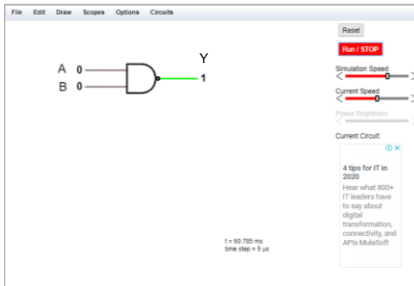
Current Speed

Power Brightness

Current Circuit:
Blank Circuit

4 tips for IT in 2020
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t = 0 s
time step = 5 μs



File Edit Draw Scopes Options Circuits

Reset

Run / STOP

Simulation Speed

Current Speed

Power Brightness

Current Circuit:
Blank Circuit

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t = 69.785 ms
time step = 1 μs

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

← 2nd row

NAND Gate

File Edit Draw Scopes Options Circuits

- Add Wire w
- Add Resistor r
- Passive Components
- Inputs and Sources
- Outputs and Labels
- Active Components
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- Logic Gates, Input and Output
 - Add Logic Input i
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 - Add Inverter 1
 - Add NAND Gate @
 - Add NOR Gate #
 - Add AND Gate 2
 - Add OR Gate 3
 - Add XOR Gate 4
- Digital Chips
- Analog and Hybrid Chips
- Drag
- Select/Drag Sel (space or Shift-drag)

Reset

Run / STOP

Simulation Speed

Current Speed

Power Brightness

Current Circuit:
Blank Circuit

4 tips for IT in 2020
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t = 0 s
time step = 5 μs

File Edit Draw Scopes Options Circuits

Reset

Run / STOP

Simulation Speed

Current Speed

Power Brightness

Current Circuit:
Blank Circuit

4 tips for IT in 2020
Hear what 800+ IT leaders have to say about digital transformation, connectivity, and APIs MuleSoft

t = 0 s
time step = 5 μs

File Edit Draw Scopes Options Circuits

Reset

Run / STOP

Simulation Speed

Current Speed

Power Brightness

Current Circuit:
Blank Circuit

4 tips for IT in 2020
Hear what 800+ IT leaders have to say about digital transformation, connectivity, and APIs MuleSoft

t = 65.705 ns
time step = 1 μs

File Edit Draw Scopes Options Circuits

Reset

Run / STOP

Simulation Speed

Current Speed

Power Brightness

Current Circuit:
Blank Circuit

4 tips for IT in 2020
Hear what 800+ IT leaders have to say about digital transformation, connectivity, and APIs MuleSoft

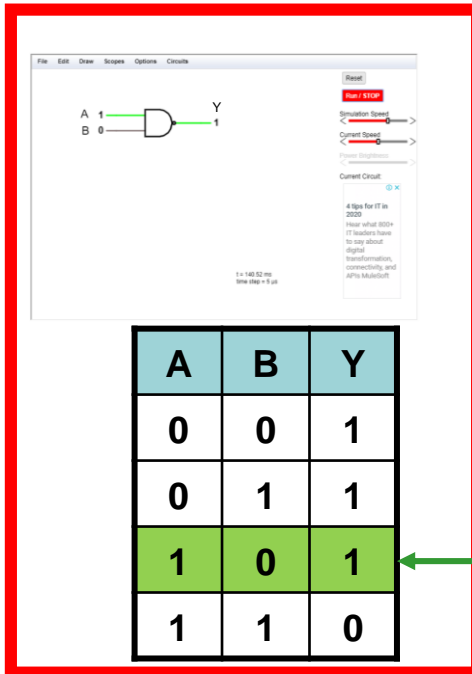
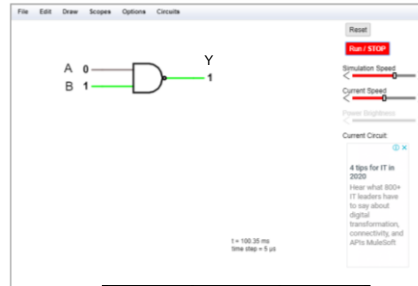
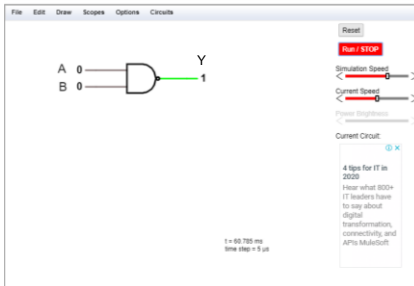
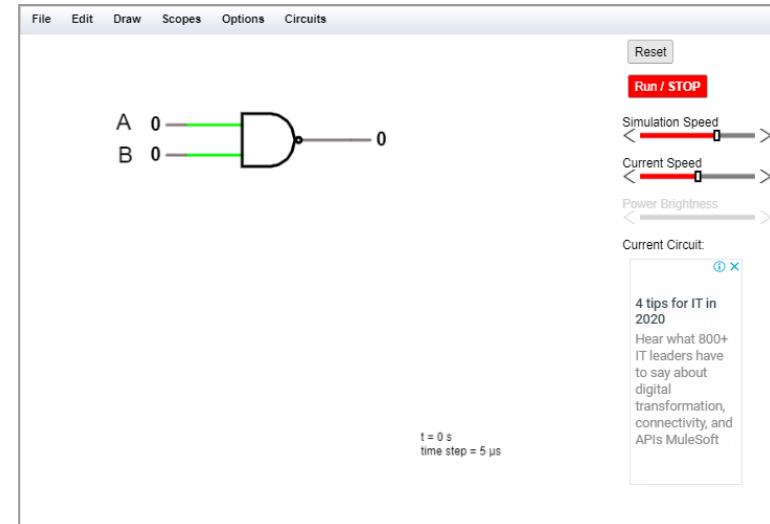
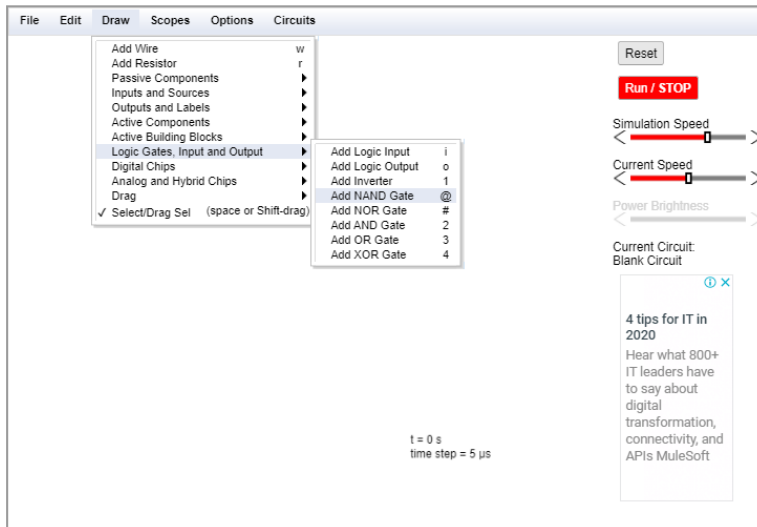
t = 100.35 ns
time step = 1 μs

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

3rd row

NAND Gate



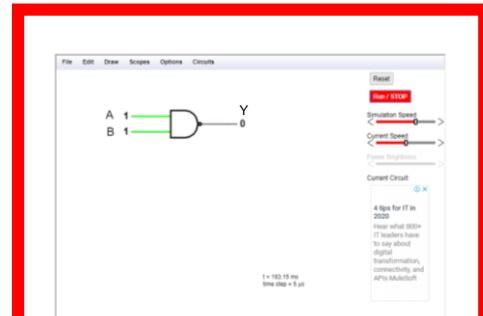
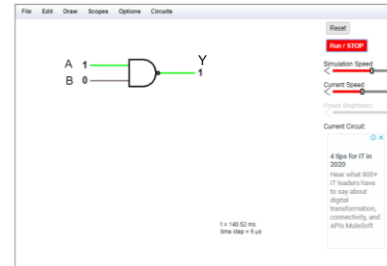
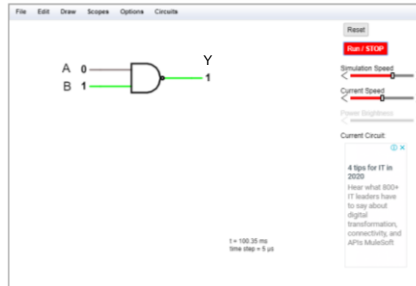
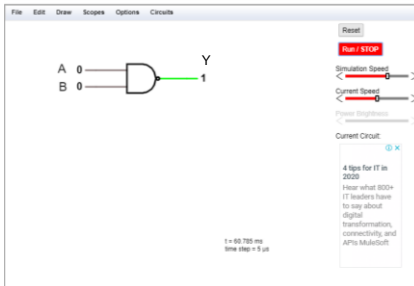
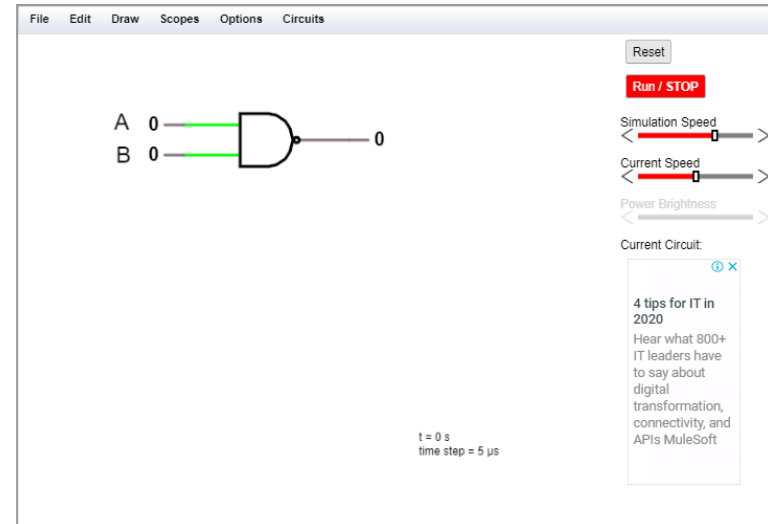
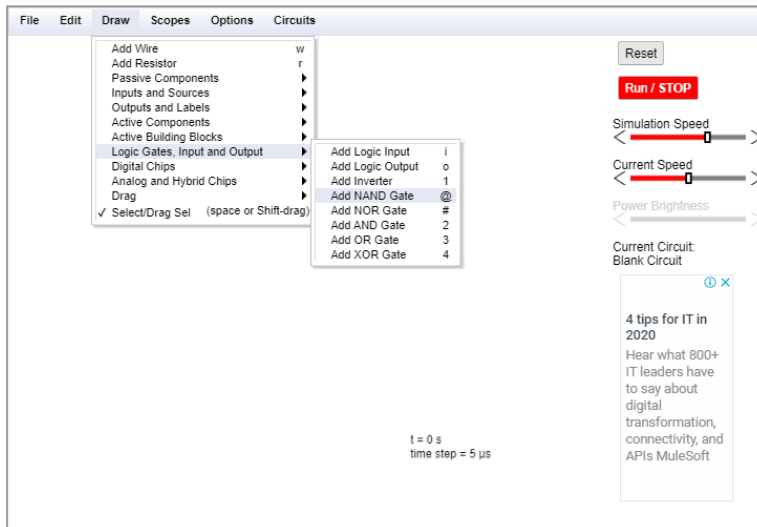
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

4th row

NAND Gate



A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

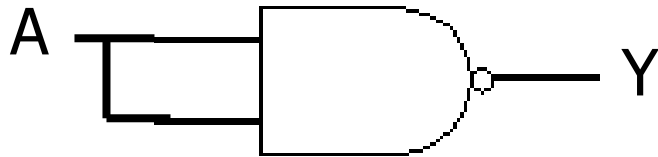
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

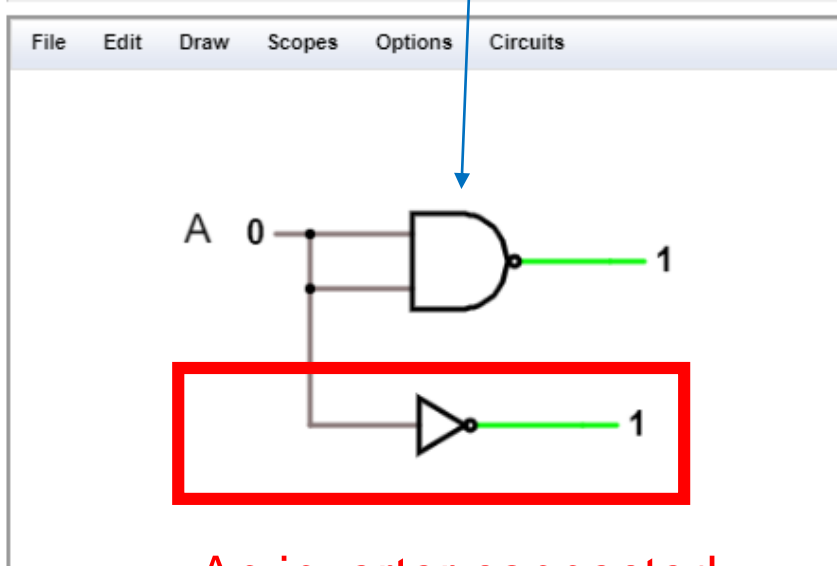
5th row

NAND gate used as another gate

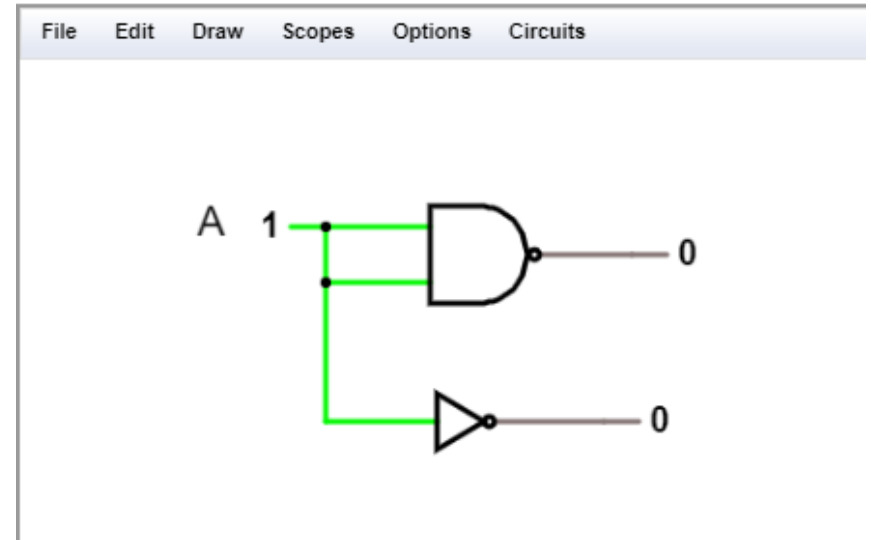


NAND gate with same input \rightarrow NOT Gate

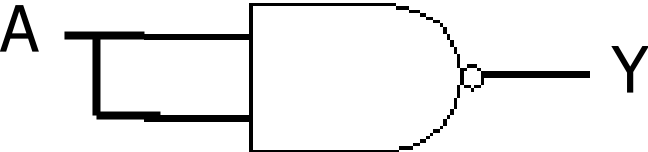
NAND gate



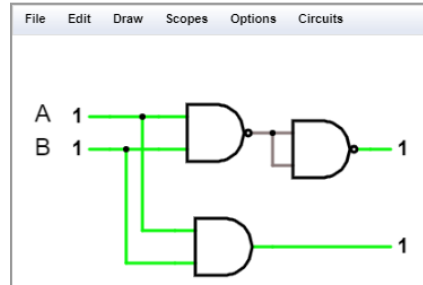
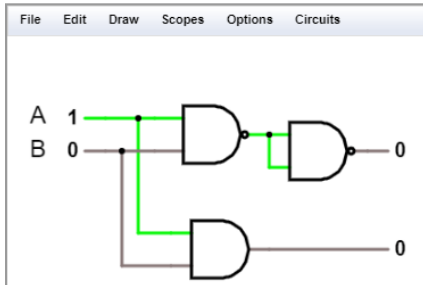
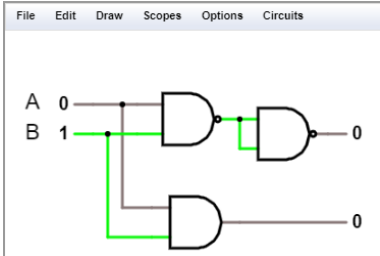
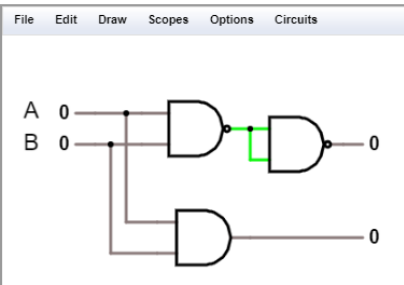
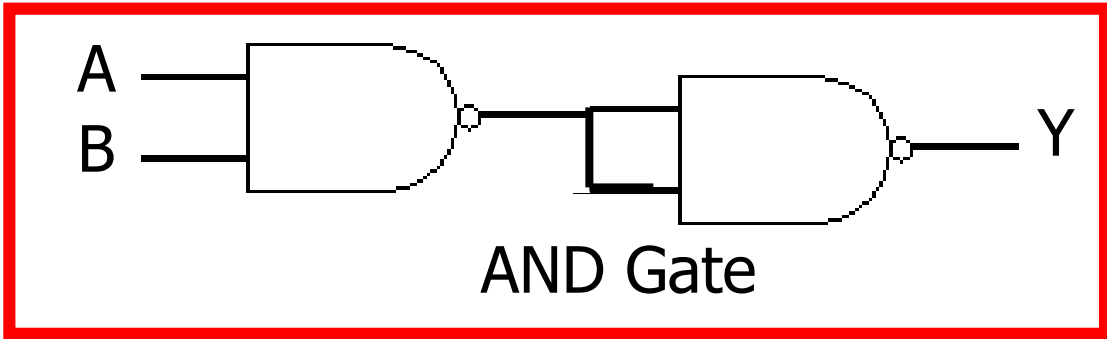
An inverter connected to the same input A



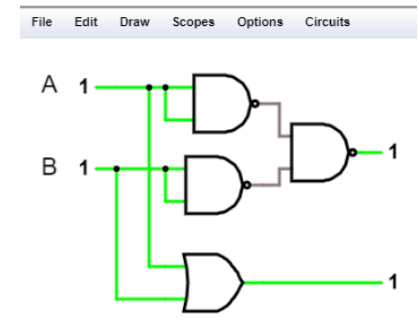
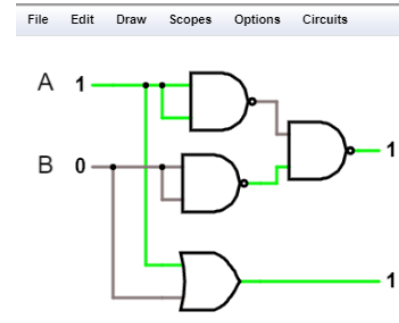
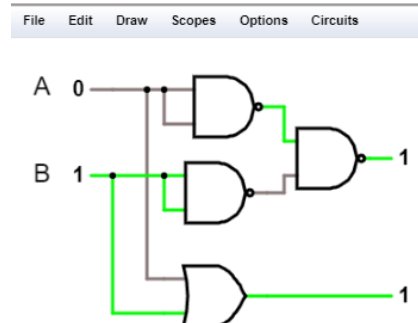
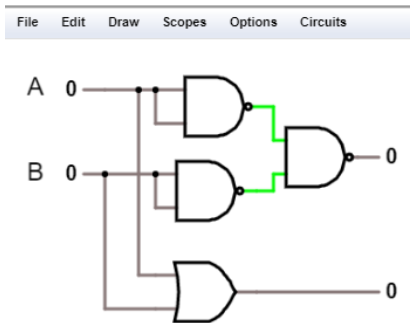
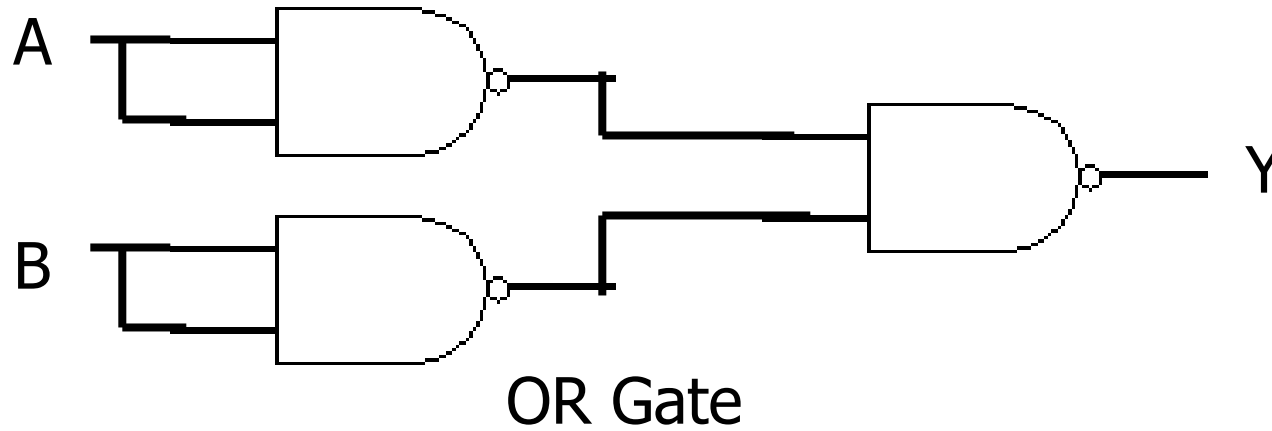
NAND gates used as other gate



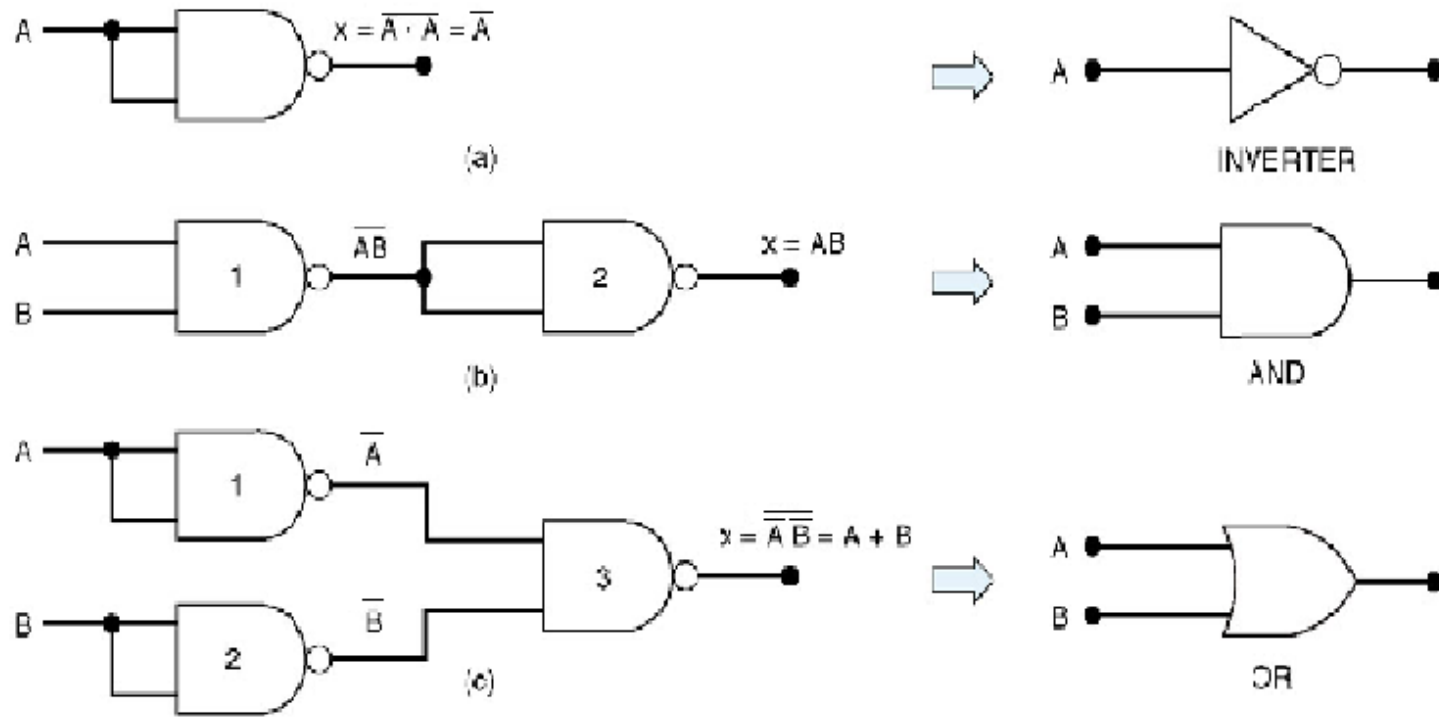
NOT Gate



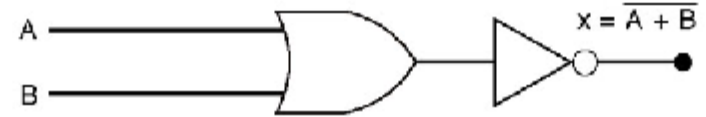
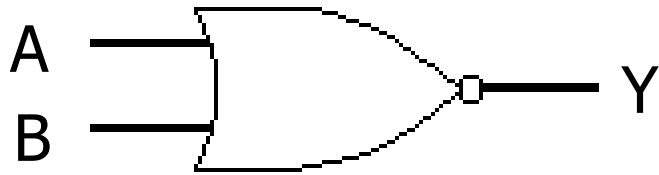
NAND gates into other gates



Universality of NAND gates



NOR Gate



- A **NOR** gate is a combination of an OR gate followed by an inverter. It's truth table shows this...

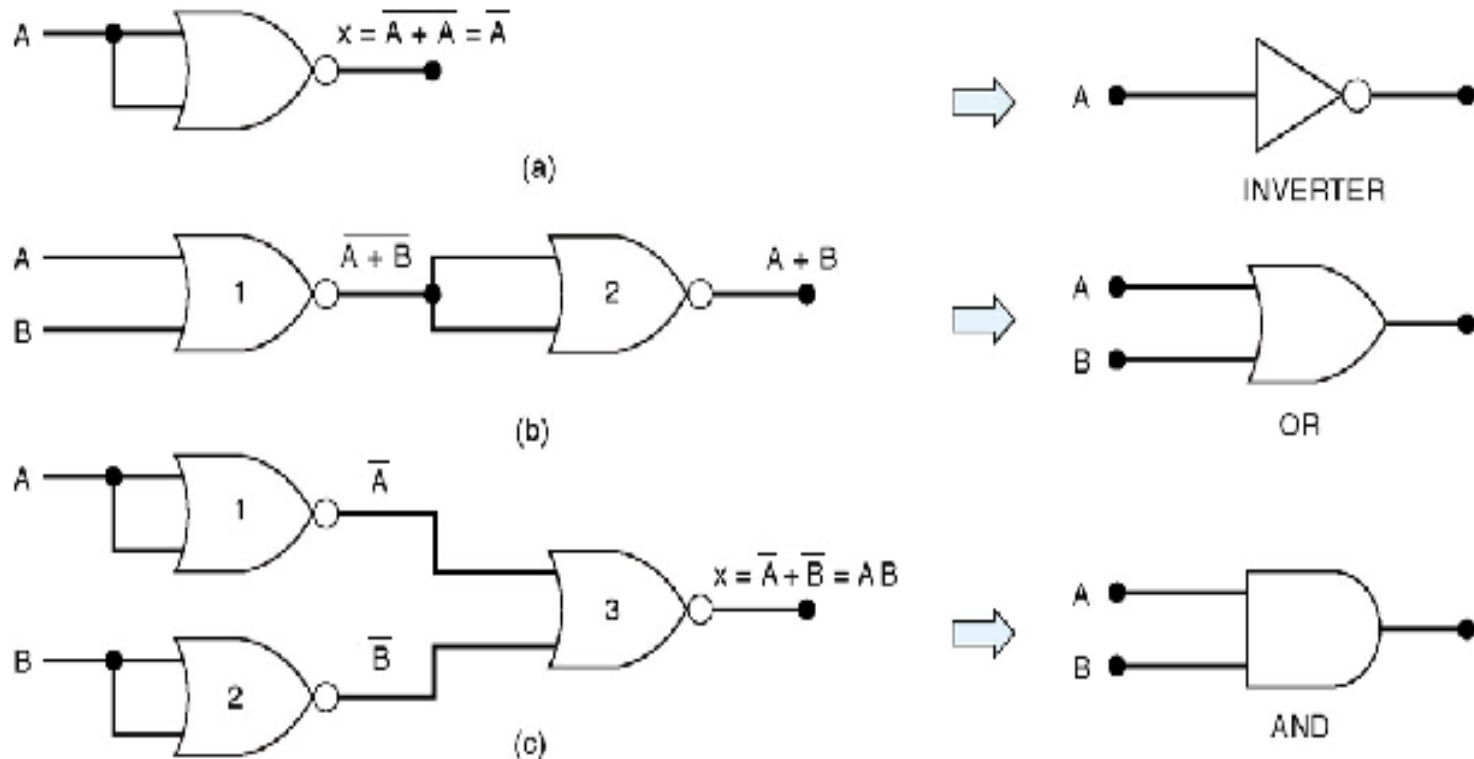
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Functionally Complete Gates

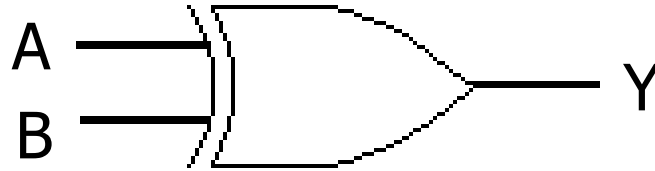
- Just like the NAND gate, the **NOR** gate is functionally complete (ie any logic function can be implemented using just NOR gates).
- Both NAND and **NOR** gates are very valuable as any design can be realized using either one.
- It is easier to build an IC chip using all NAND or NOR gates than to combine AND, OR, and NOT gates.
- NAND/NOR gates are typically faster at switching and cheaper to produce.

Universality of NOR gate

Equivalent representations of the AND, OR, and NOT gates



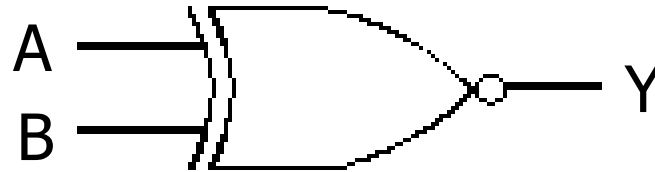
XOR Gate (Exclusive-OR)



- The symbol for the **XOR** gate is shown above.
- XOR gates assert their output when exactly one of the inputs is asserted, hence the name.
- The switching algebra symbol for this operation is \oplus , i.e.
 $1 \oplus 1 = 0$ and $1 \oplus 0 = 1$.

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

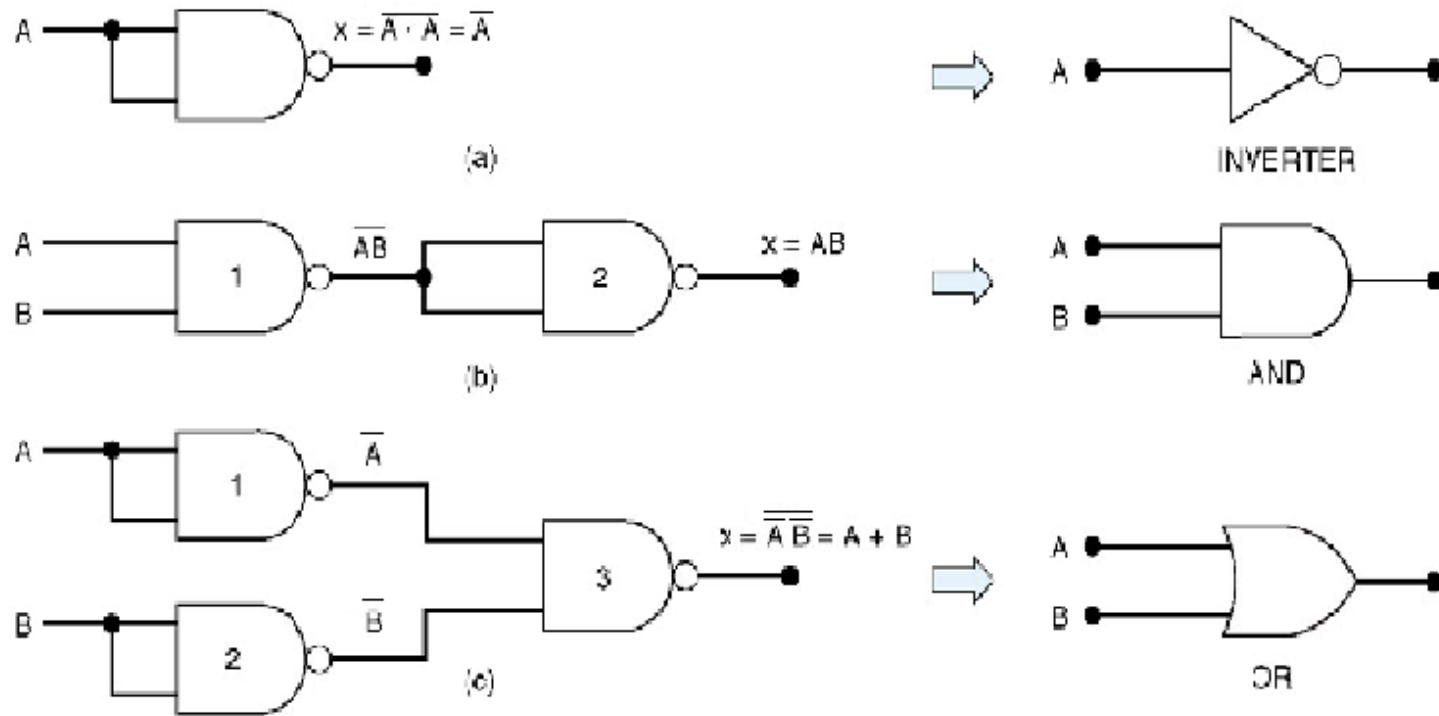
XNOR Gate



- This is a XNOR gate.
- This functions as an exclusive-NOR gate, or simply the complement of the XOR gate.
- The switching algebra symbol for this operation is \odot , i.e. $1 \odot 1 = 1$ and $1 \odot 0 = 0$.

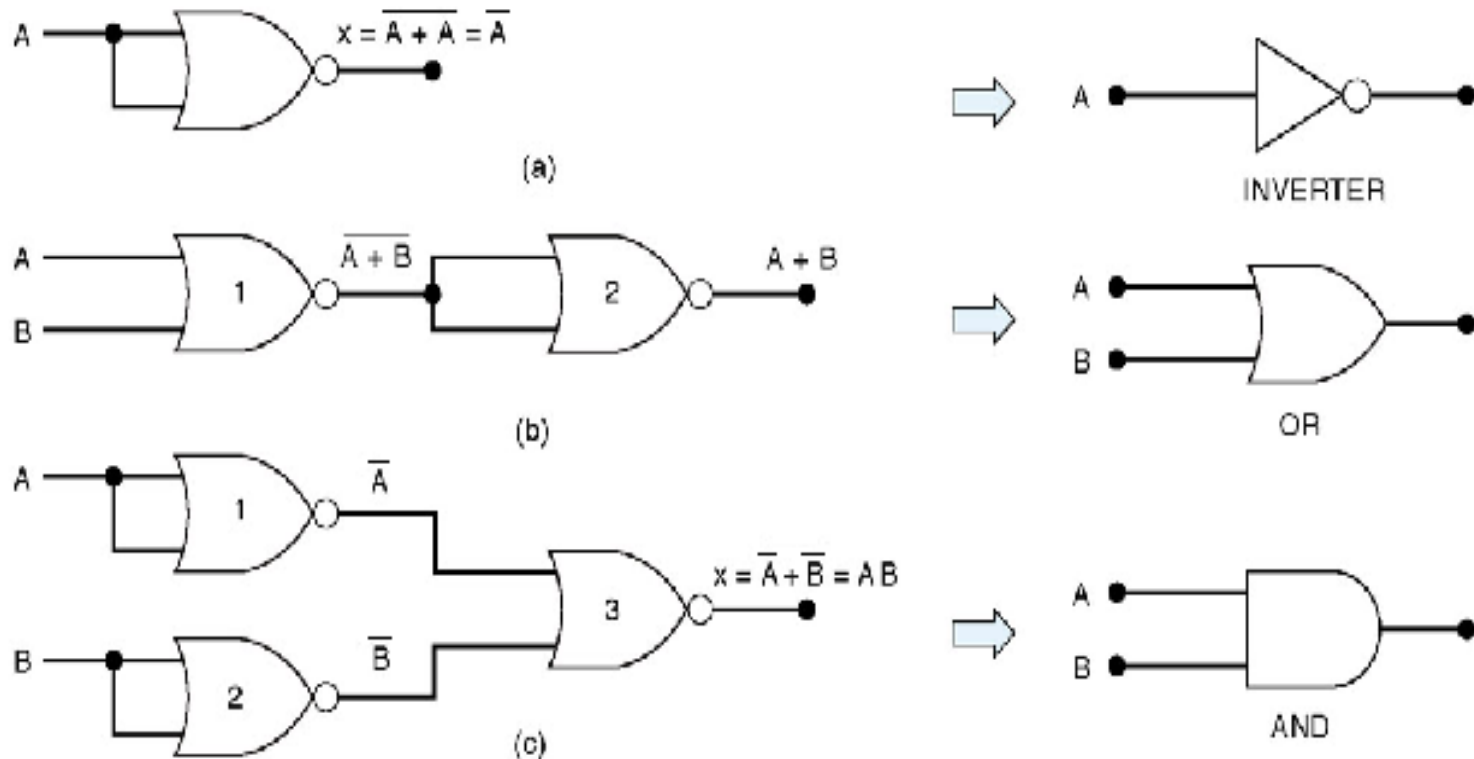
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

Universality of NAND gates



Universality of NOR gate

Equivalent representations of the AND, OR, and NOT gates



Week 5 Lecture 9a

- NAND, NOR, XOR and XNOR gates

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- `kerese@ecs.vuw.ac.nz`